EICROC and HGCROC/CALOROC status and plans

ePIC AC-LGAD TOF DSC meeting
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Organization for Micro-Electronics desiGn and Applications

EICROC0 update

- Firmware update (old version @ Omega)
  - New version implemented ✓
  - Scripts corrected to work with new firmware ✓
- Code development for new firmware
  - Config files, test scripts, data processing scripts ✓
  - Code that allows to plot S-Curves, TDC, ADC, Hit automatically
  - Uploaded on GitLab
- Documentation write-up (updated over time)
  - User guide ✓
  - Code guide ✓
  - Datasheet
  - Uploaded on GitLab
- Tests on ASIC with new firmware and scripts
  - S-Curves ✓
- New boards have been produced and assembled
  - Tests started this week (need rework as I2C translator soldered upside down)

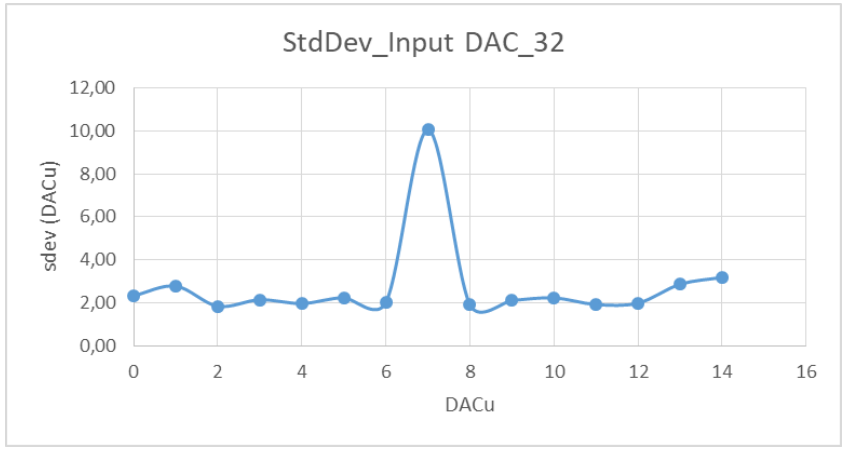
Ex : S-curves on 16 channels with threshold trimming

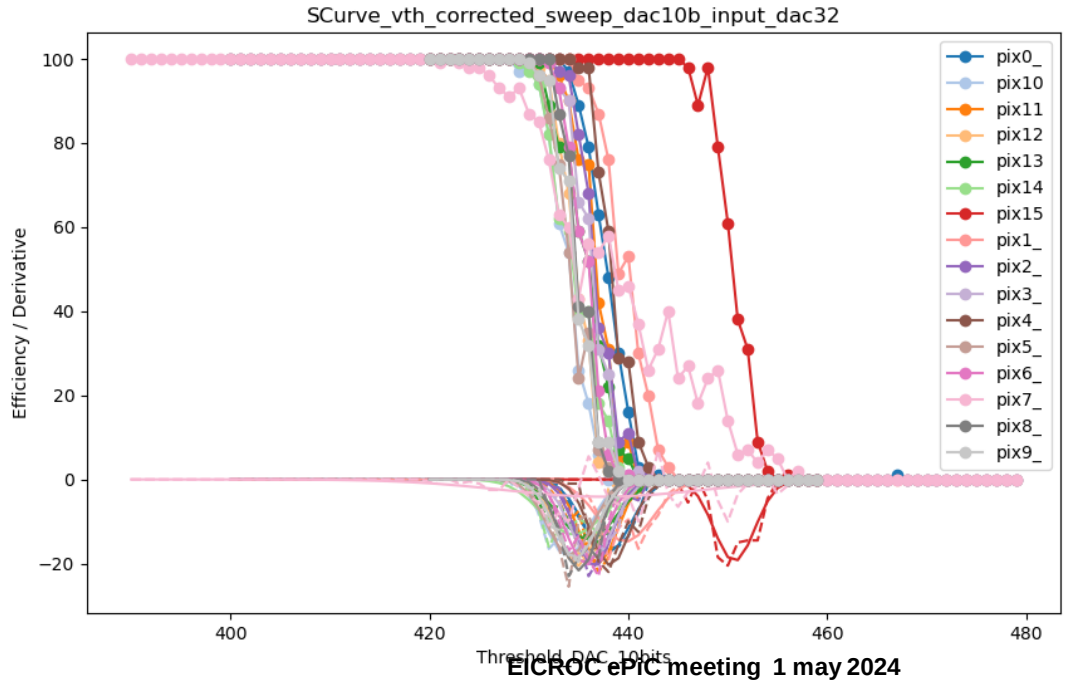
Input DAC_pulse 32: ~ 14 fC

Vth_correction fixed for each channel at the measured value

0,11 fC / DACu

Input DAC_32_vth_corrected_chbych		
	50% trigger efficiency	StdDev
Mean	437,1840275	2,778044388
min	433,8969726	1,848503507
max	450,6570696	10,04795084
delta	16,76	



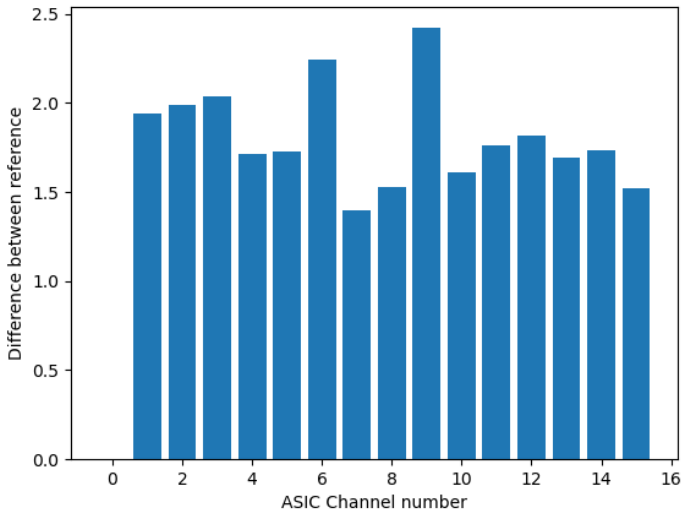


Crosstalk:

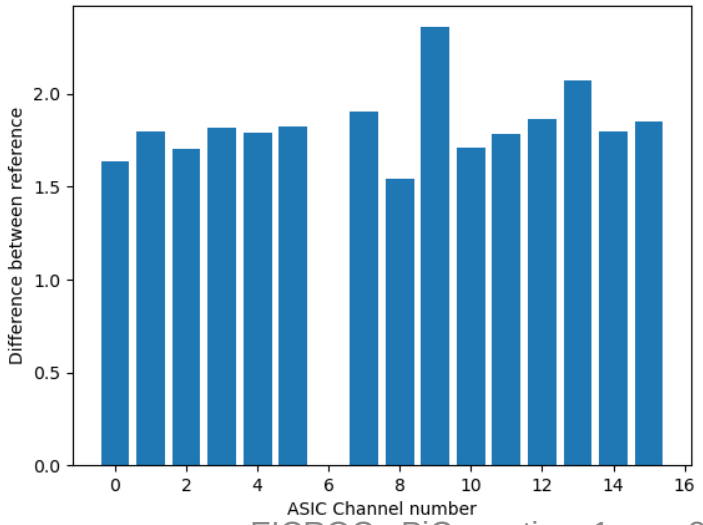
A large signal is injected into one channel through the internal DAC pulser (DAC code = 63 → 250 mV in 100 fF → ~ 26 fC). The threshold is scanned across all channels to count the number of triggers generated by the internal signal. Theoretically, when we scan the threshold without injecting a signal, the discriminator triggers on the noise present on the preamplifier DC level (the pedestal). If there is a coupling signal in nearby channels due to the signal injected into one channel, the pedestal of the nearby channel could shift.

In the figure, we plotted the difference in the 50% trigger efficiency when no signal is injected and when a signal is injected into only one channel. The measurement is repeated by injecting the signal into the first pixel, in the middle of the ASIC and in the last pixel. The pedestal shits of around 2 DACu that corresponds to 0.22 fC. This value is within the range of measurement error. This low value indicates that there is no coupling signal present in the trigger path.

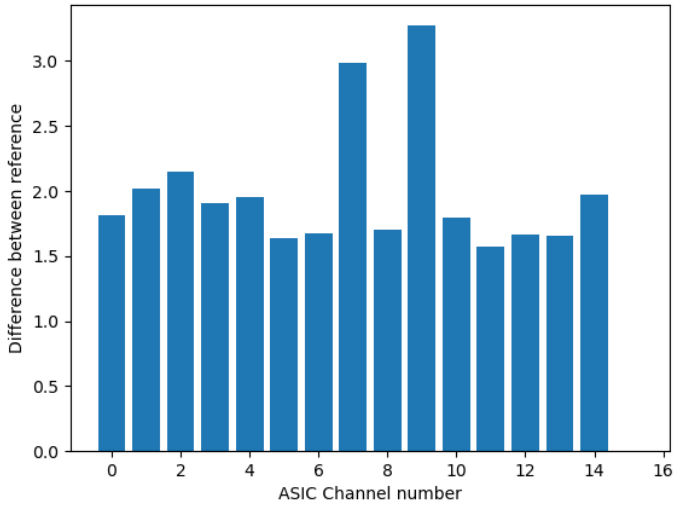
50 % trigger efficiency pedestal – 50 % trigger eff pedestal (with a large signal (dac_pulse_63) injected in pixel 0)



50 % trigger efficiency pedestal – 50 % trigger eff pedestal (with a large signal (dac_pulse_63) injected in pixel 6)

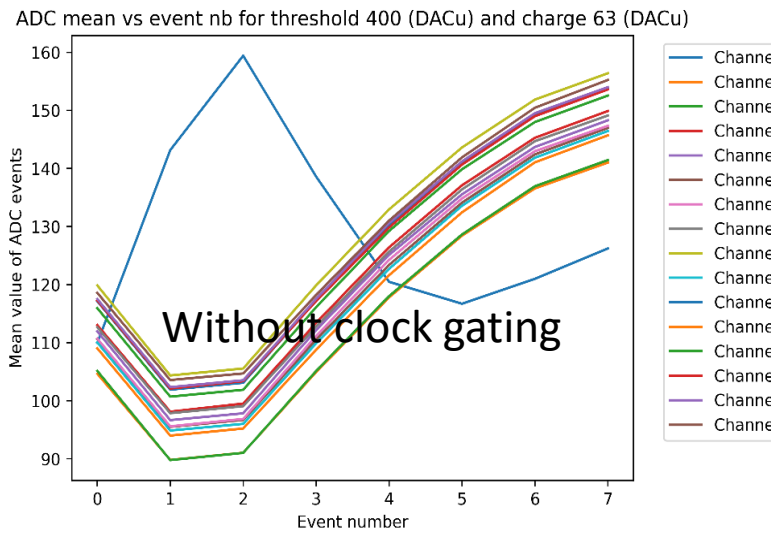


50 % trigger efficiency pedestal – 50 % trigger eff pedestal (with a large signal (dac_pulse_63) injected in pixel 15)

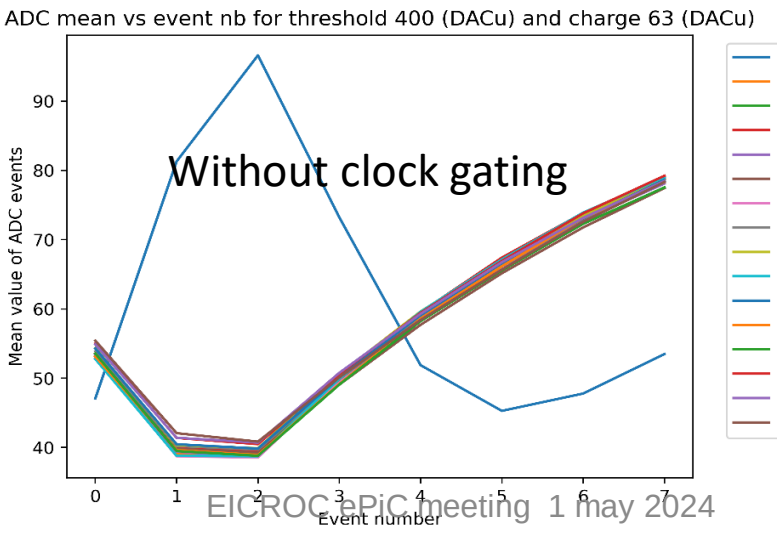


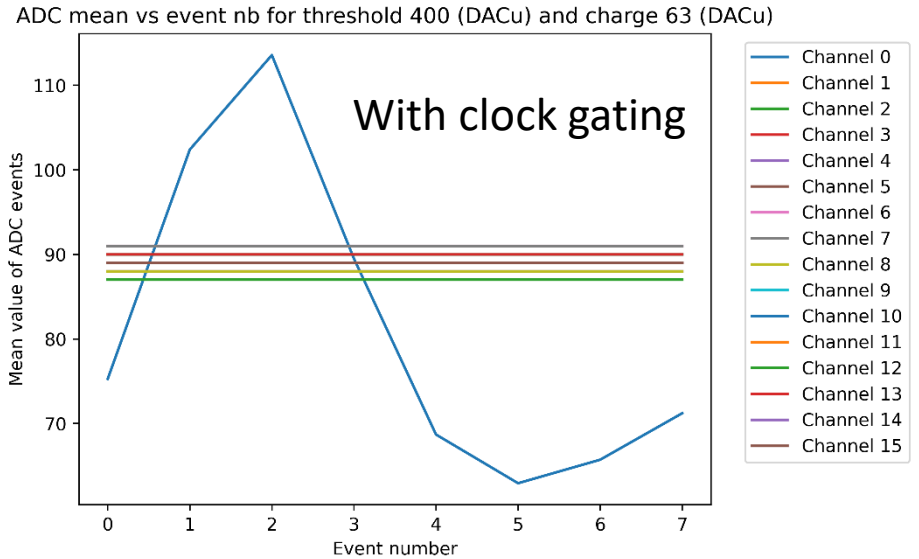
ADC (CHARGE): A large signal is injected into one channel through the internal DAC pulser (DAC code = 63 → 250 mV in 100 fF → ~ 26 fC). The charge ADC values are measured for all channels. To measure the ADC pedestal, clock gating is deactivated to continuously measure the shaper output value and estimate the ADC pedestal. The first picture shows the pedestal before adjusting the shaper output DC level using a DAC named Vref_correction, which allows adjusting the DC level on each channel. The second picture corresponds to the pedestal after DC correction. The pedestal is evidently more uniform after the correction. The third picture shows the charge measurement in the channel where the signal is injected (with clock gating activated). The strange shape of the pedestal indicates coupling at the charge pedestal level, which is under investigation. The shaper signal is also observed on the oscilloscope thanks to the analog probe, and the coupling is evident even in the analog part. A preliminary observation of these signals on the oscilloscope suggests that the coupling is between the CMD pulse and the shaper output. This is under investigation

Pedestal uniformity
Before pedestal trimming



Pedestal uniformity
After pedestal trimming



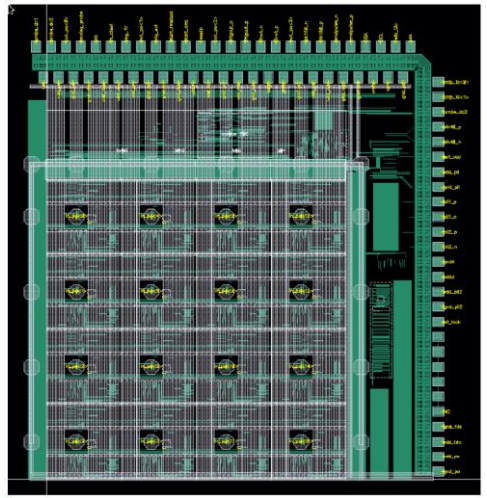


Status of EICROC

- EICROC0 is a testbeam prototype => sensor characterization
  - Triggered readout, all data shipped out : 16 ch * 8 samples ADC + TDC
  - Present power ~2 mW/ch + 4*20 mW « analog probe preamp »
  - Status : measurements in progress
  - ADC power + shaper/driver to be reduced from ~1 mW to 100 µW/ch => EICROC0A
  - EICROC0A : simulations in progress

- EICROC1 will address larger dimensions 4x16 or 8x16 or 4x32 or 8x32
  - Address floor planning and power distribution
  - Selective readout : hit + 9 neighbouring channels
  - Status : layout started based on EICROC0, adding more testability
  - Still EICROC0-like readout

- EICROC2 final size : 32x32

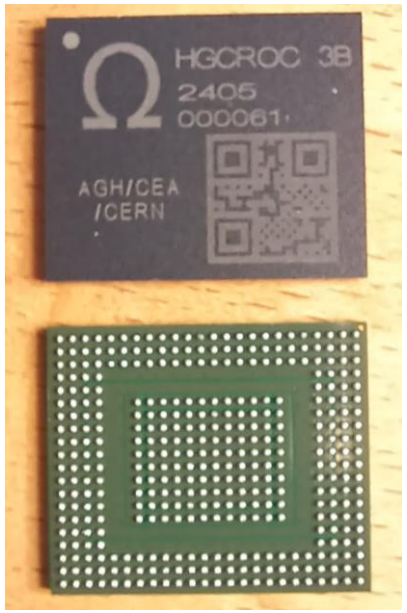


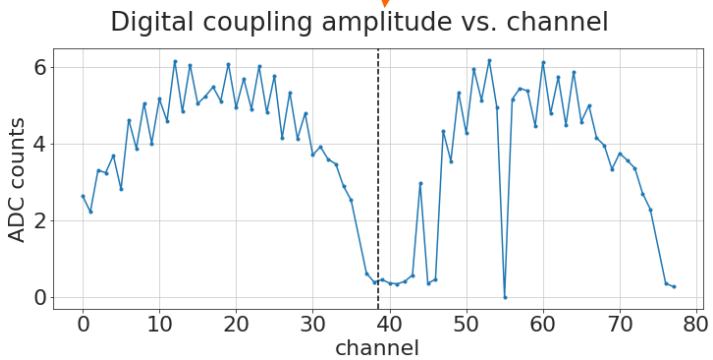
HGCROC3B overview

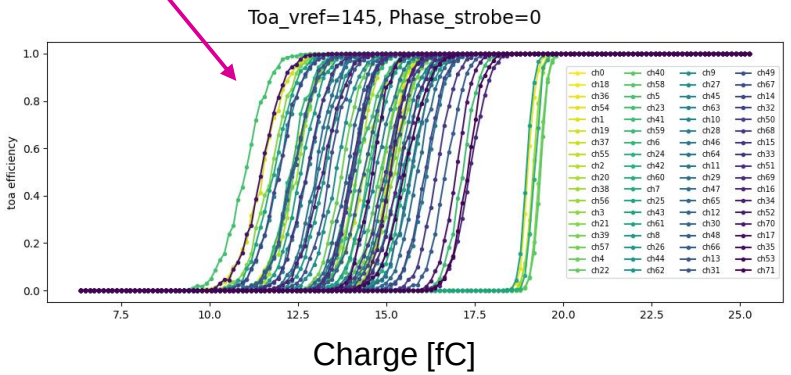
- Fabrication 20 wafers HGCROC3B launched may 23.
  - Fixed missing ADCs, RAM2 bitflips, SETs in PLL
  - But issue with missing C4 bumps (IMEC) : chips received only beg. Feb 24
- Substrate studies : common ground vs separate ground
  - Digital noise, pedestal shift, minimum ToA threshold
  - HGCROC3A mounted on different substrates and tested on mezzanines
- Robot commissioning
  - 600 chips already tested, 2000 more to go
- SEE tests
  - 3 campaigns at Arronax (69 MeV p+)

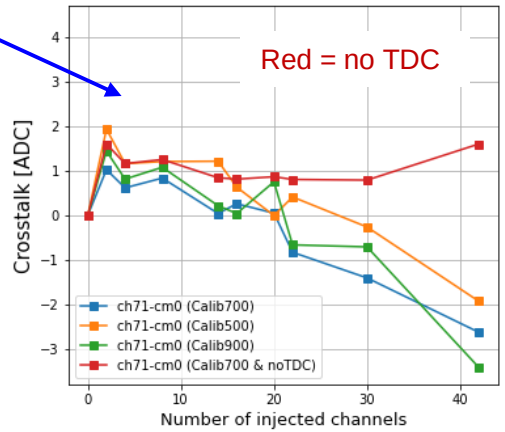
LD substrate studies

- 2 variants of LD substrates
  - SU02 : common ground, analog power domains of ADC and TDC are connected to the analog region
  - SU04: separated grounds, all power domains of ADC and TDC are connected to the digital region
- So far, only HGCROC3 tested on mezzanine
- Optimization/minimization of the digital coupling
  - results below from LD common ground from SERMA
- Min. delta pedestal, Min. ToA threshold, TDC-induced pedestal shift





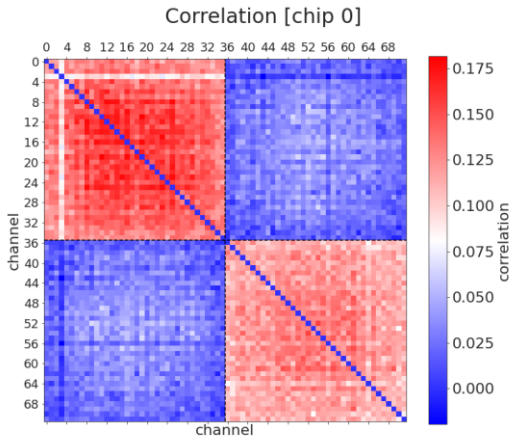


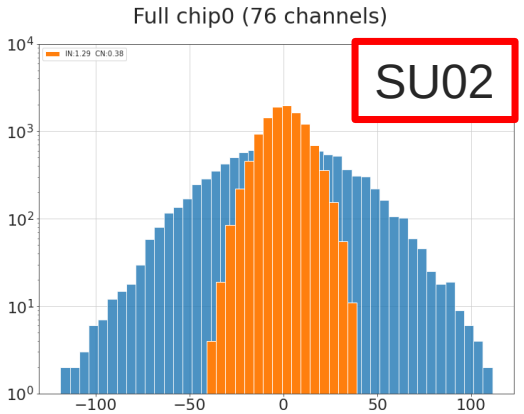


Negative crosstalk due to number of fired TDCs

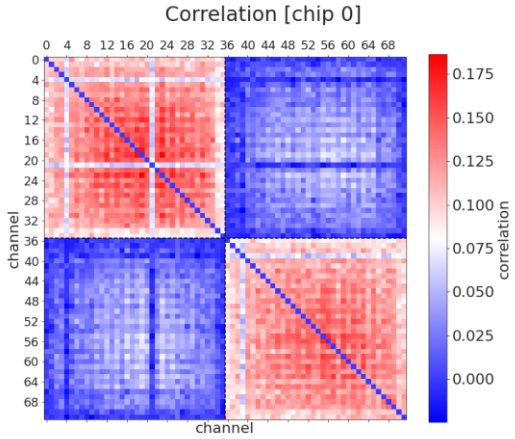
Pedestal and noise

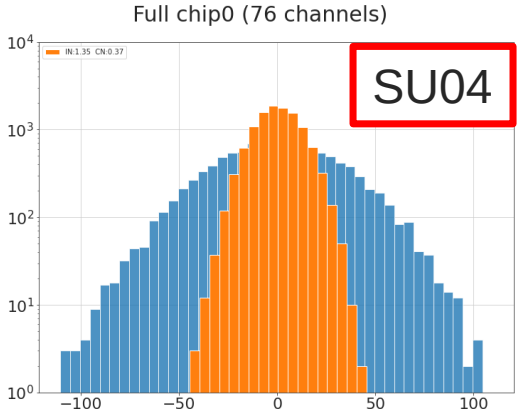
- **SU-02 on mezzanine** with 47 pF capacitor
- Incoherent (1.3) vs. coherent noise (0.5) as usual
- Digital noise ~15 UADC

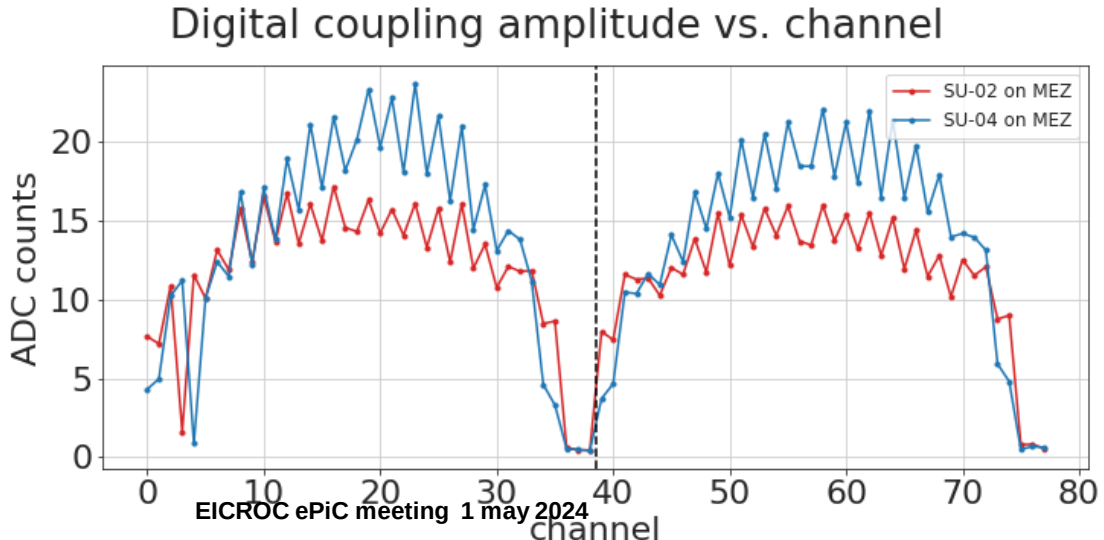




- **SU-04 on mezzanine** with 47 pF capacitor
- Incoherent vs. coherent noise similar
- Digital noise ~20 UADC



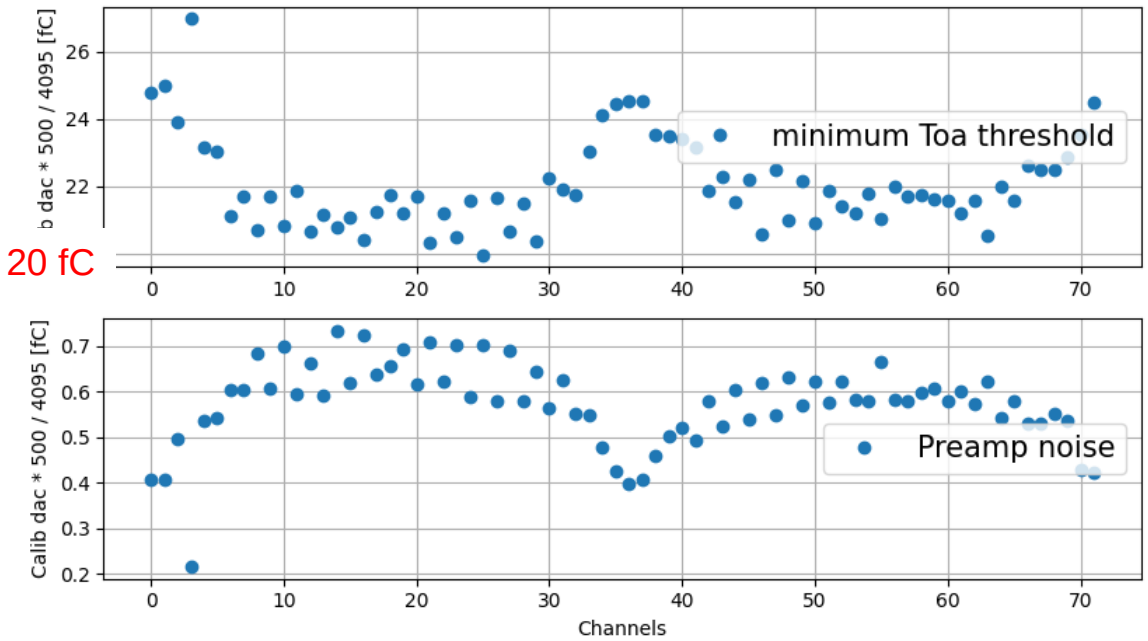




Digital modulation on minimum ToA threshold

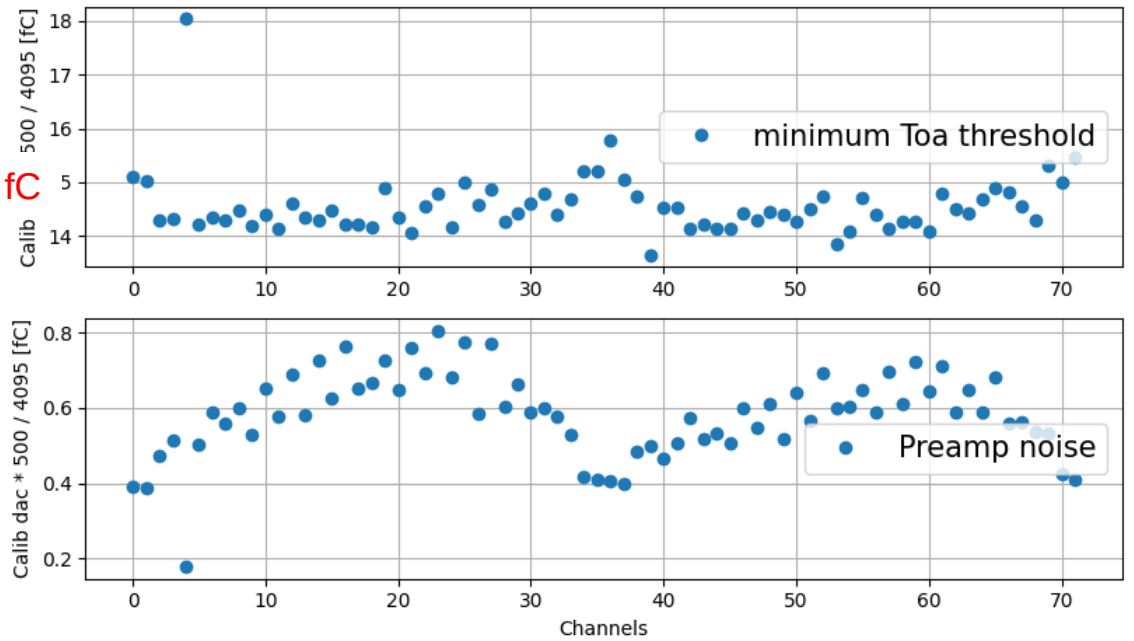
- 47 pF cap. on normal channels
- SU-04 (~ 14,5 fC) better than SU-02 (~ 21 fC)
- Digital coupling effects are not exactly the same after preamp and after shaper (= filter)

SU-02 on mezzanine



20 fC

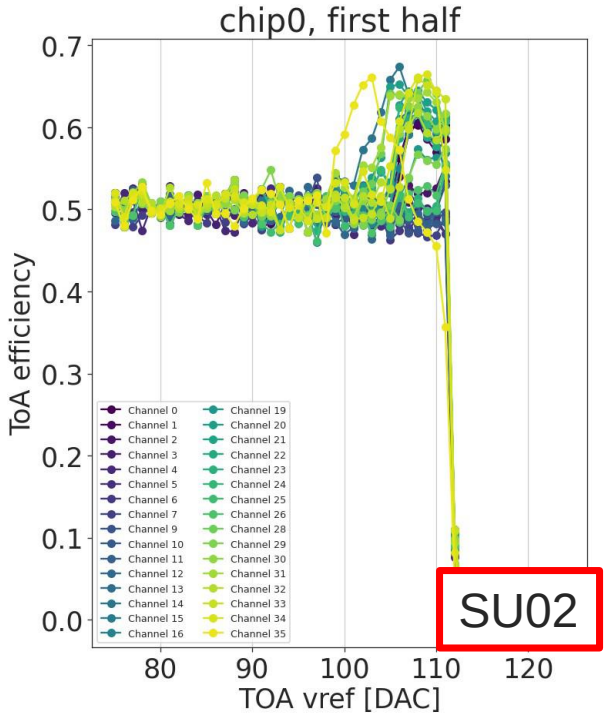
SU-04 on mezzanine

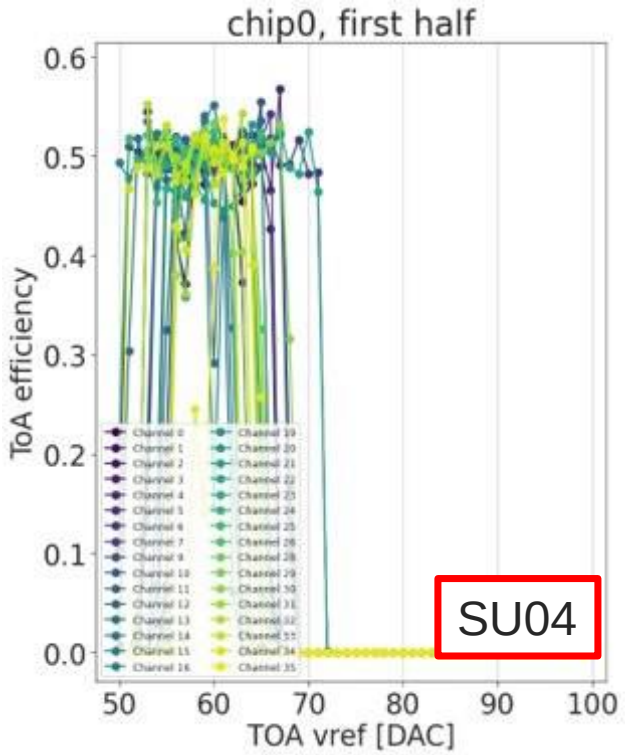


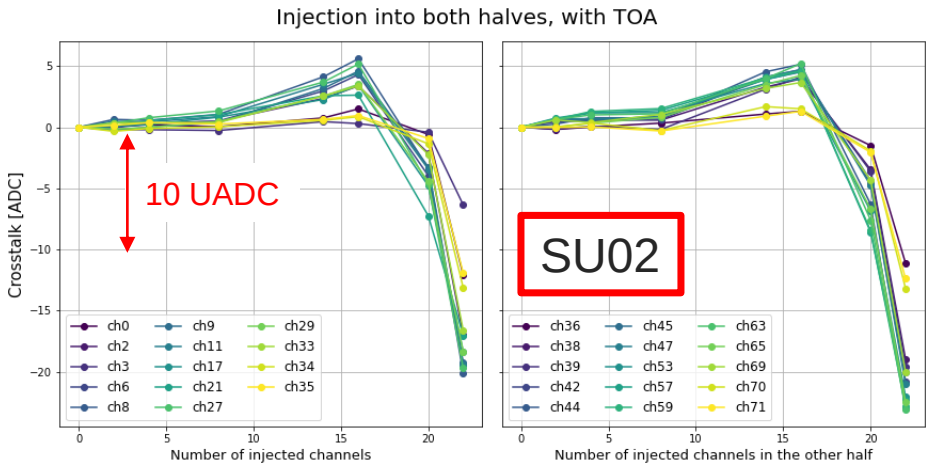
15 fC

TOA threshold trimming and crosstalk [Arnaud et al.]

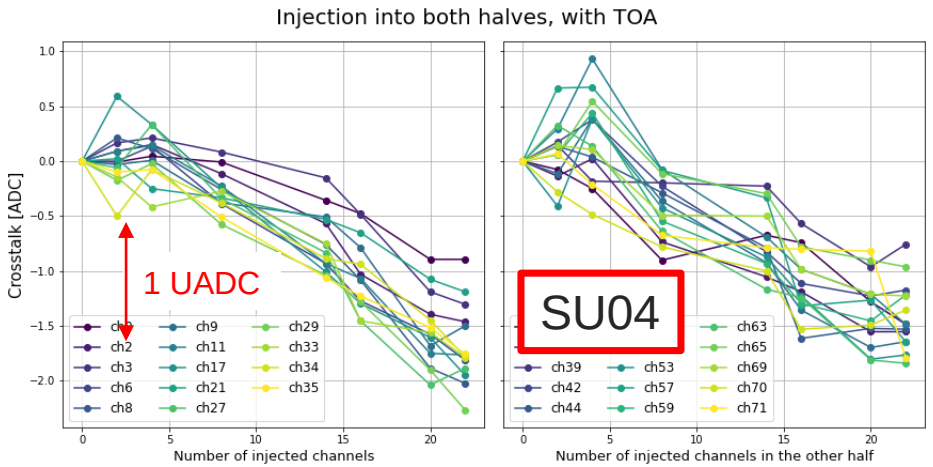
- Cleaner thresholds with SU04
- Better crosstalk and pedestal stability with SU04







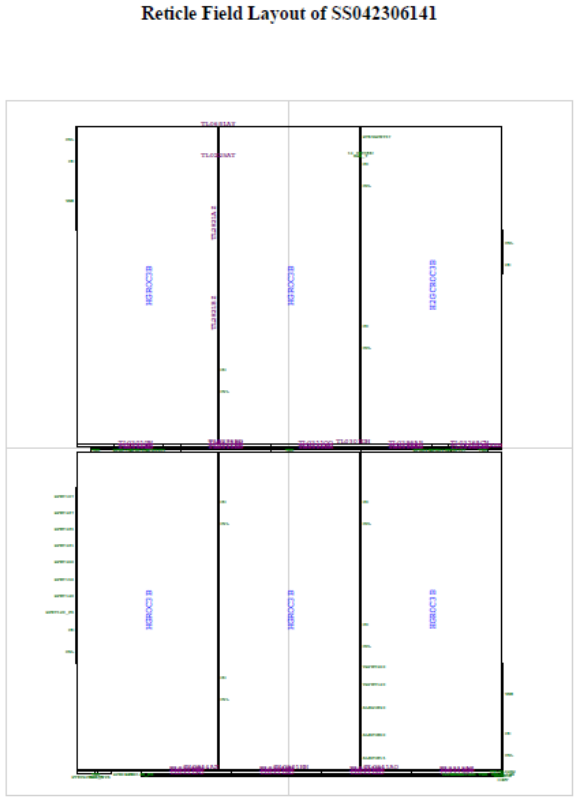
~200 MIPS



~200 MIPS

HGCROC3B fabrication (long) timeline

- May 24 th : gds files sent to IMEC
  - Reticle with 6 dies and 2 dies types (5 x HGCROC3b and 1 x H2GCROC3b).
  - 20 wafers ordered (12 on hold)
- June 12th : Dry run completed at IMEC/TSMC
  - But issue with reticle fill factor too small, finally waived (thanks Kostas)
- July 15th : Fabrication finally launched
- Sept 28th : first 8 wafers received at CERN
- Oct 6th : sent to NCAP for LD packaging
- Oct 17th : NCAP informs us that the C4 bumps are missing…
  - Not ordered by IMEC…
  - 7 wafers sent back to TSMC for bumping, got stuck at customs…
  - 10 wafers on hold at IMEC released, received 31 jan 24, sent to NCAP
  - 1 wafer processed at NCAP for bumping then packaging
    => provided the first chips
- Feb 5th : First 600 packaged HGCROC3Bs received at OMEGA
  - 2 substrates : mostly SU02 but some 04 for tests
- March 22nd : second batch of 2000 3Bs



Reminder: From HGCROC3 to HGCROC3b: issues and fixes

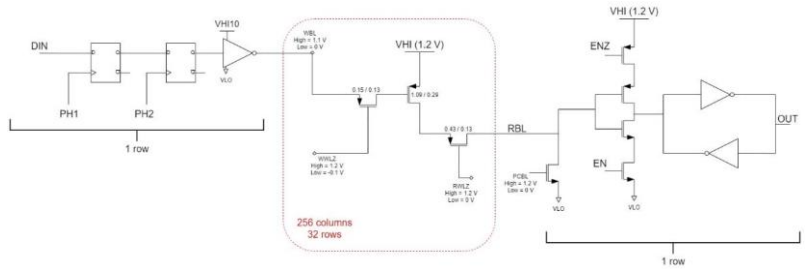
Before PRR

- **(1) RAM2:** 1 to 0 bitflips
  - Fixed with cap on RBL node
  - Availability to short VHI10 to vddd by SC
  - Good results from HKROC1 (sister chip for tests)
- **(2) ADC:** flat or “ghost” ADC, 5% of the channels
  - Fixed with longer conversion pulses
  - Good results from HKROC1
- **(3) TDC:** TOA in wrong BX, bad startup condition (504 code)
  - New startup sequence
  - Good results from HKROC1
  - With fix to avoid events in BX+2
    - Simulation only

After PRR

- **(4) TOA occupancy:** outliers in ToA data when several channels trigger at the same time (retriggering)
  - Adding hysteresis and deglitcher

(1)



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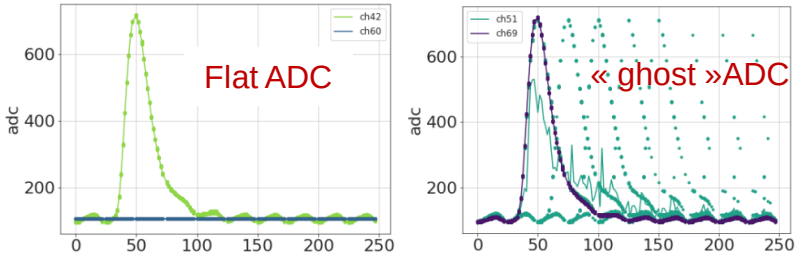

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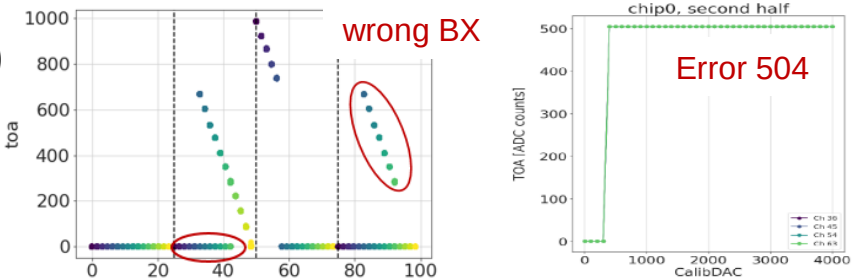

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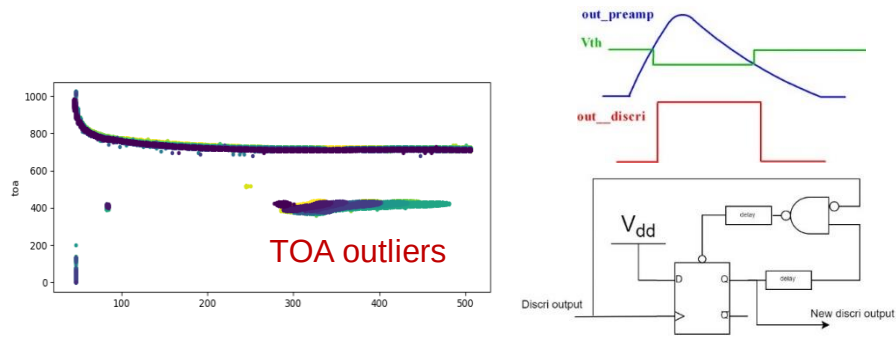
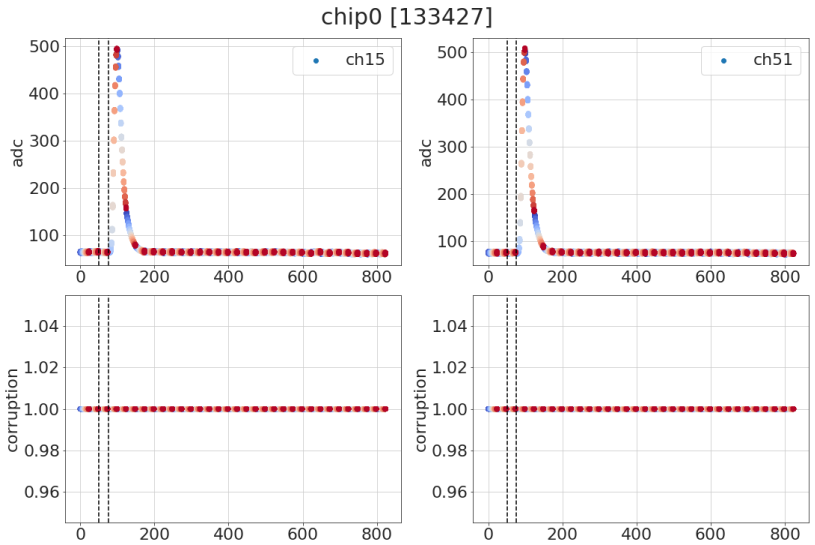
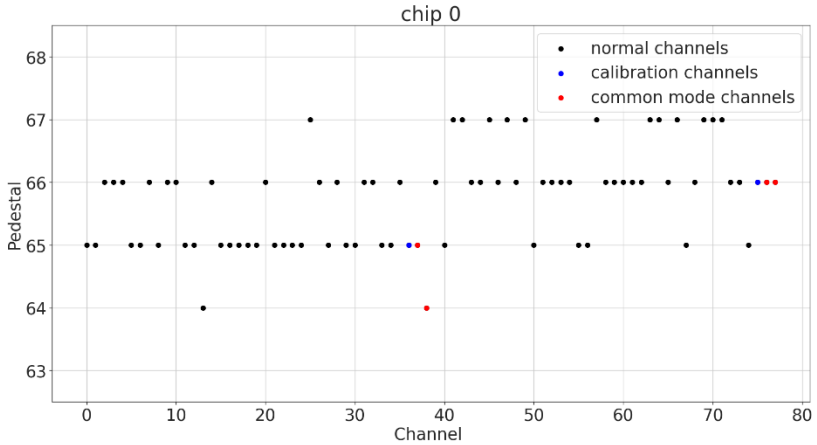
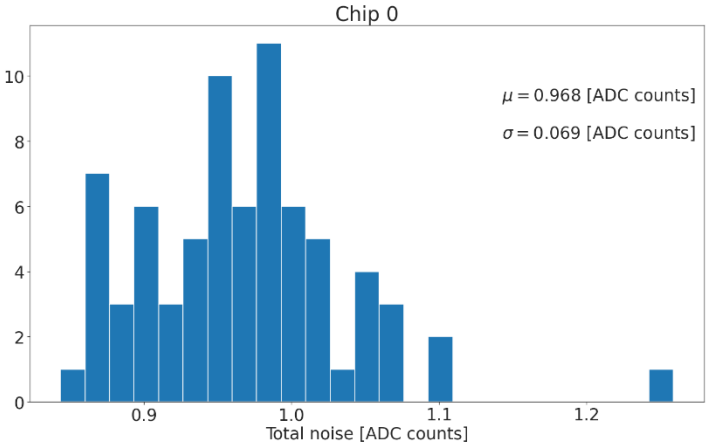


RAM2 bitflips and bad ADC

- VHI10 connection to vddd has been removed
  - No hamming error detected in all tested chips
  - Even with 32 consecutive L1A
    - worst case as the last event is kept in RAM2 for more than 30 µs
- Without any trimming on ADC delays
  - No bad ADC in all tested chips
  - Noise around 1 ADC count (Cdet=0)

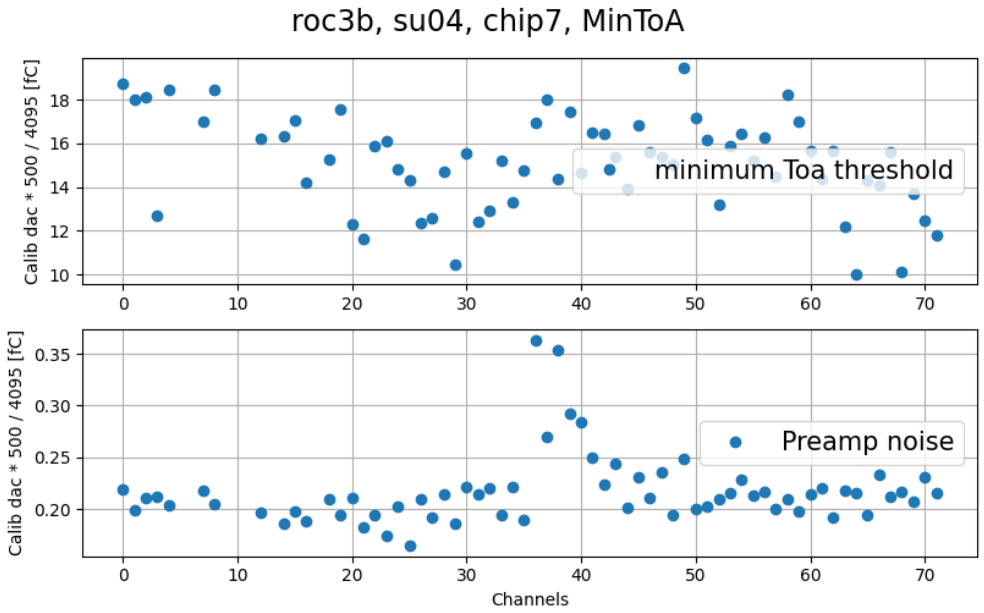


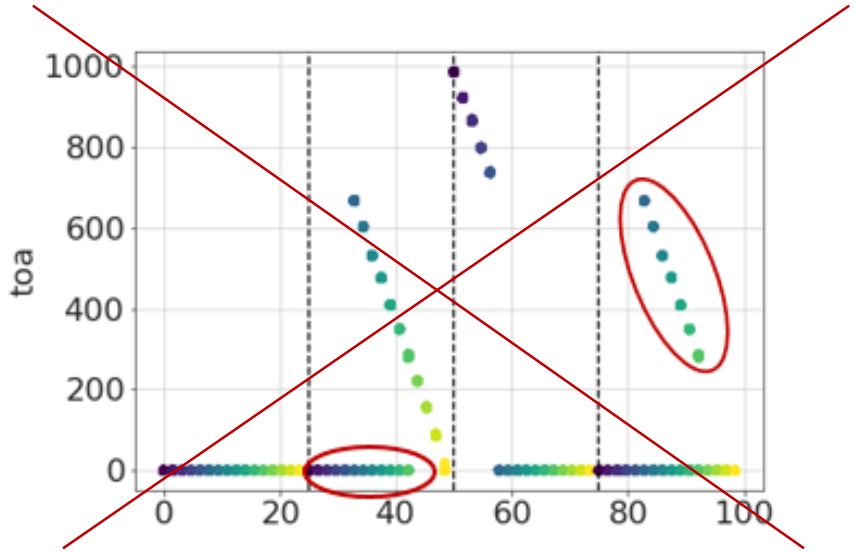




Minimum TOA threshold

- Test on the socket board (without input capacitor)
- Minimum Toa_vref very low: ~15 fC
- There is no TOA data at BX+2



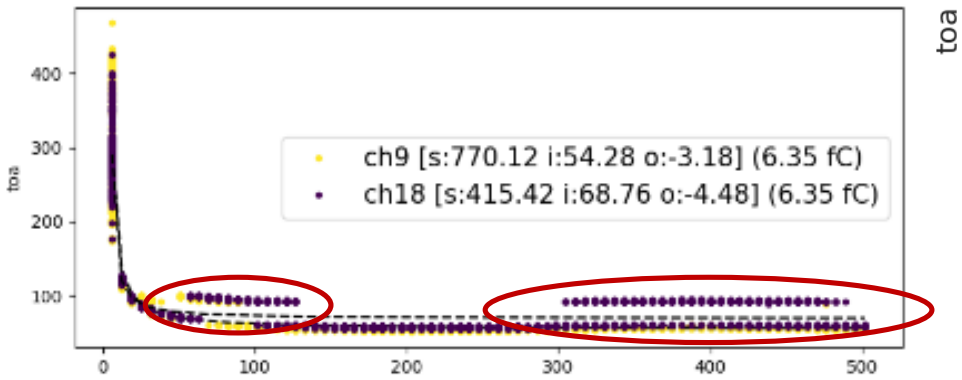


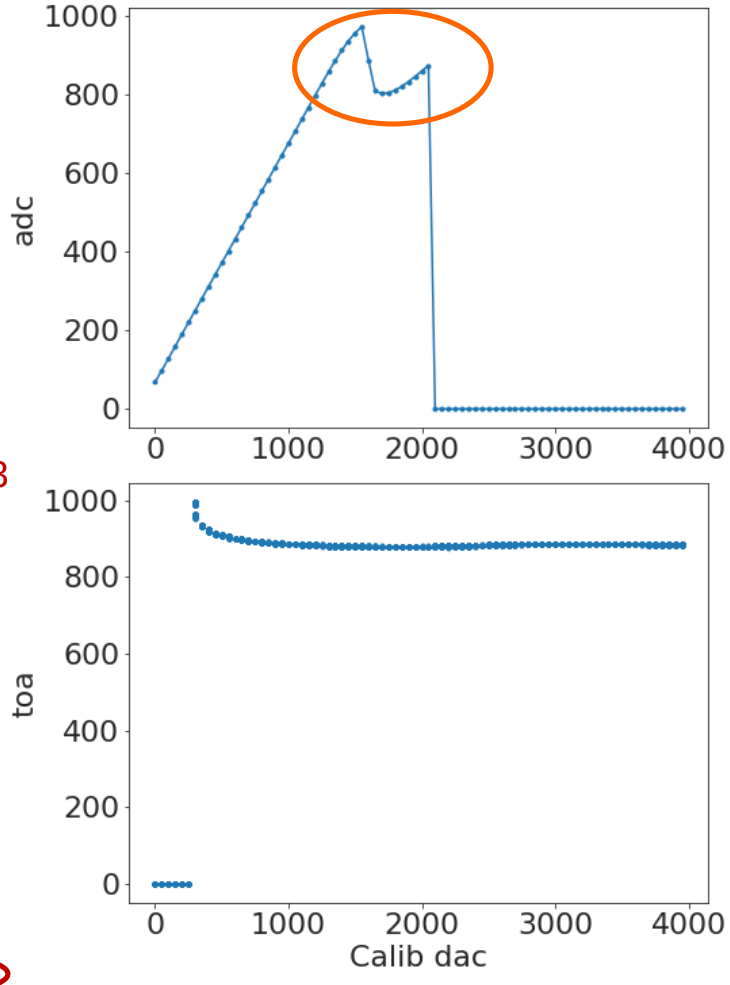
Unexpected TOT effect: sampling_scan

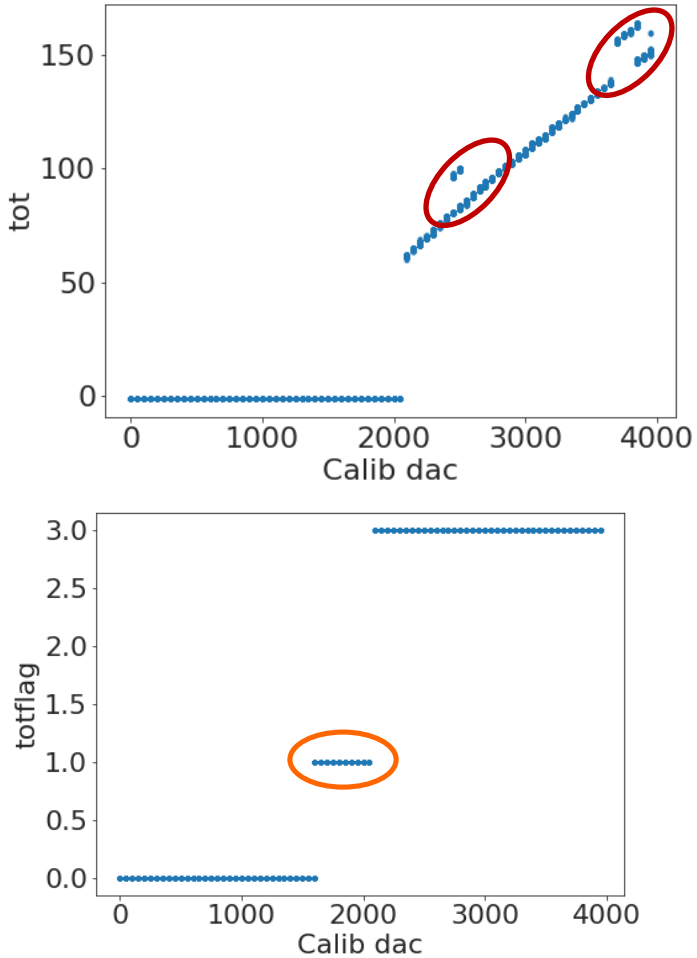
- During a sampling scan, injecting a charge triggering a TOT, data appear only on some phases but not all

- ToT gap
  - For short ToT, TDC converts but provide 0
  - Mistigate with Cdet as larger ToT

- ToA and ToT outliers
  - Positive outliers on the coarse TDC (+8, +16, +3
  - ToA and ToT

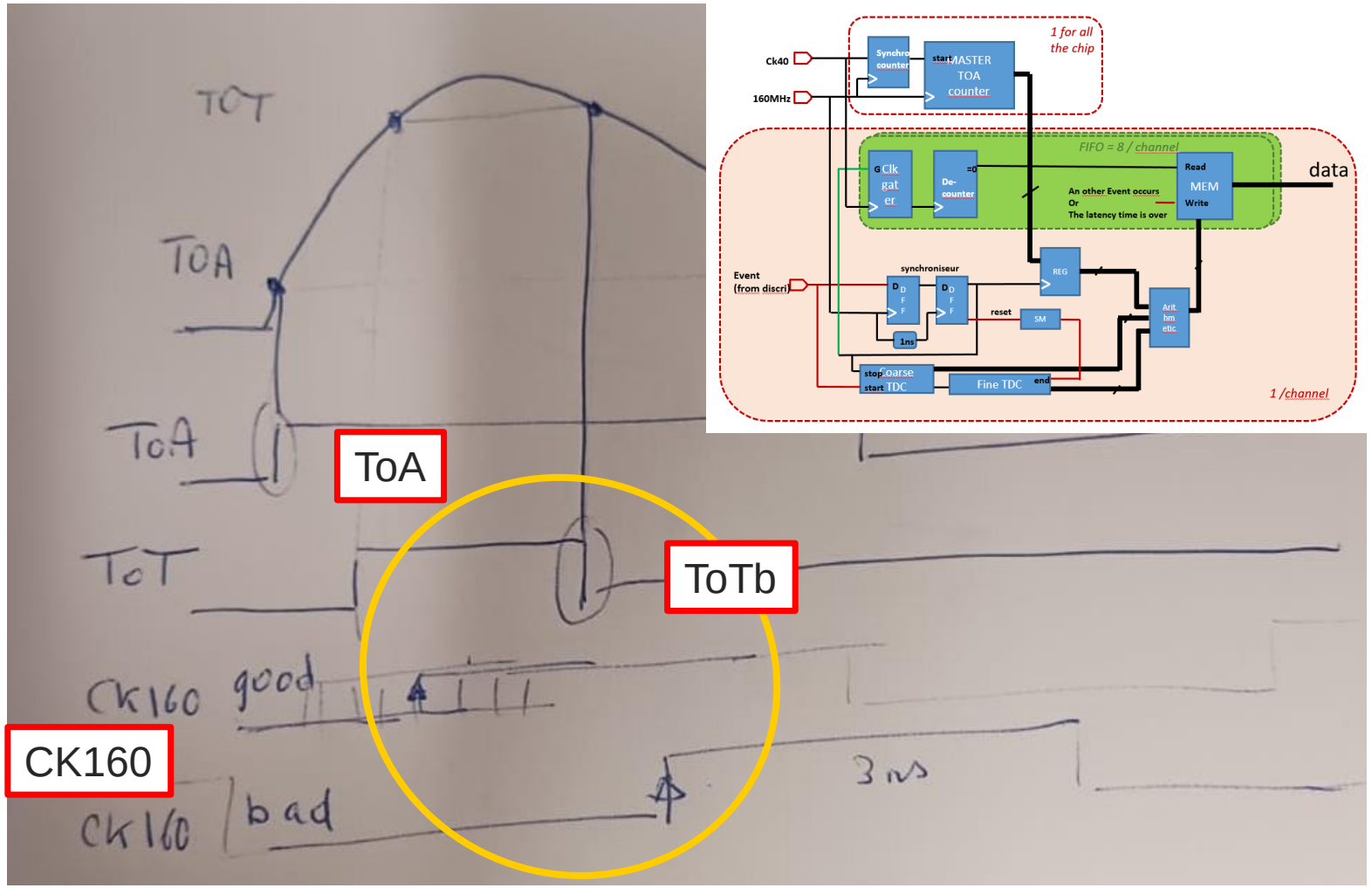




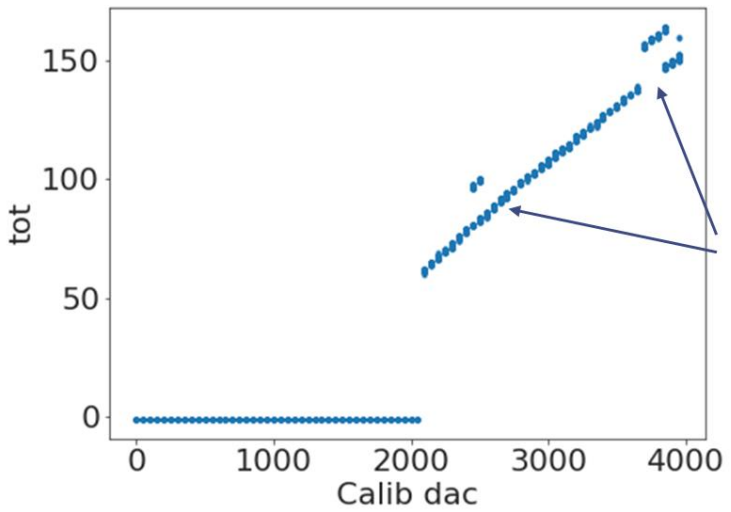


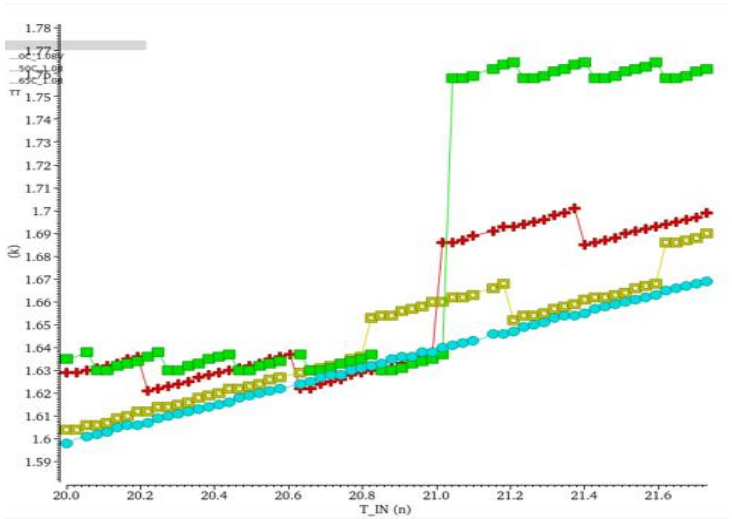
ToT gap

- ToA and ToTb are resynchronized by 160 MHz clock
- If ToA and ToTb happen both before CK160, they produce the same synchronized signal, but ToA slightly later (because more loaded) and thus rejected by the logic => ToT = 0
- If ToTb happens after CK160 they produce different outputs correctly handled
  - Easier for larger ToTs
  - Some phases are better
  - Easier with sensor capacitance
- Was not seen on HKROC test vehicle because there is only ToA
- Fix : add 300 ps delay in ToT, possible with only metal change

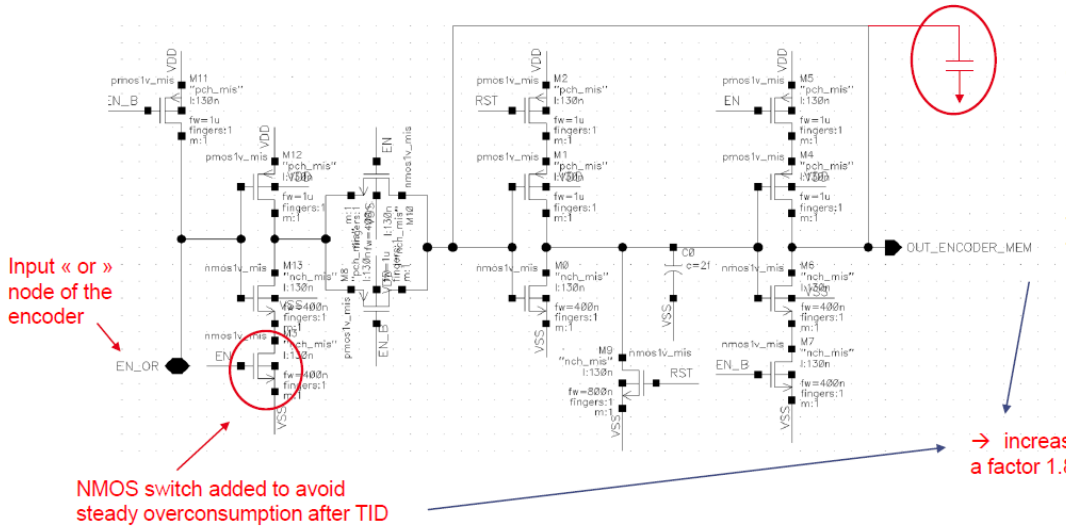


ToT outliers





Source of the problem: the latch of the TDC encoder

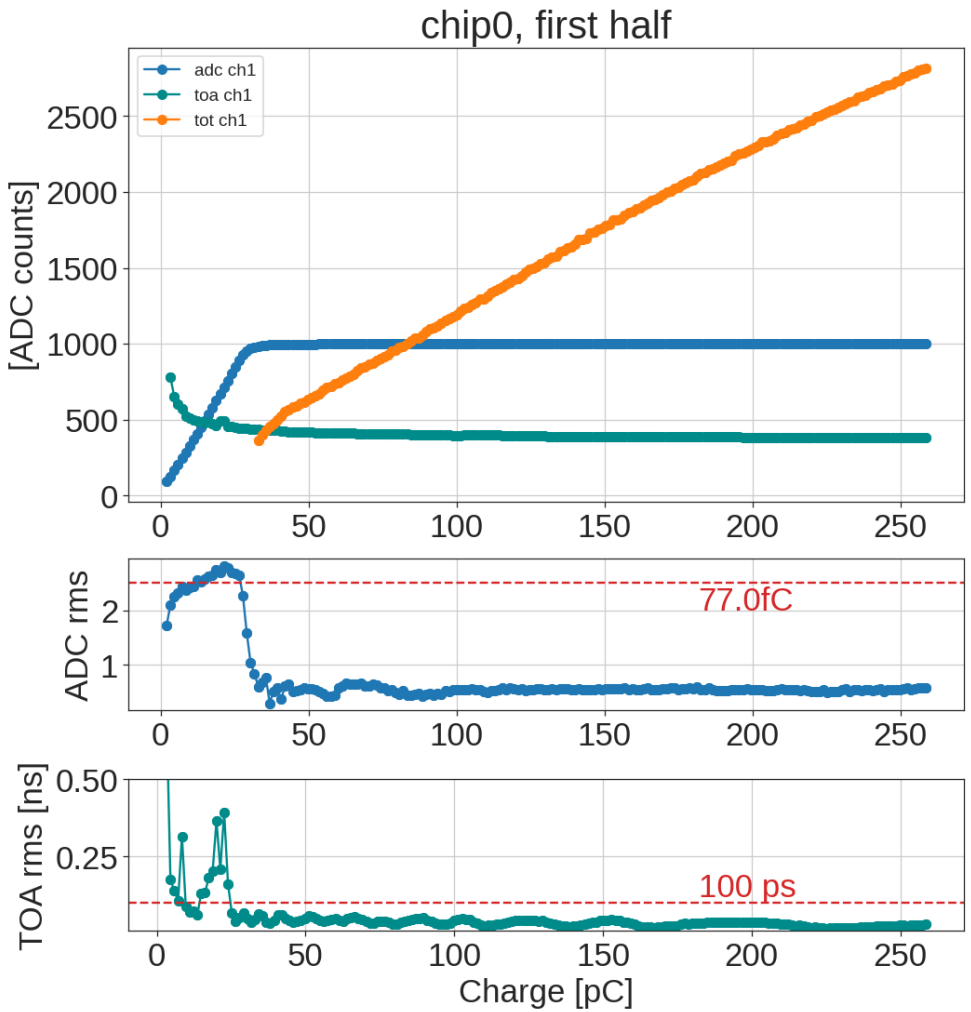


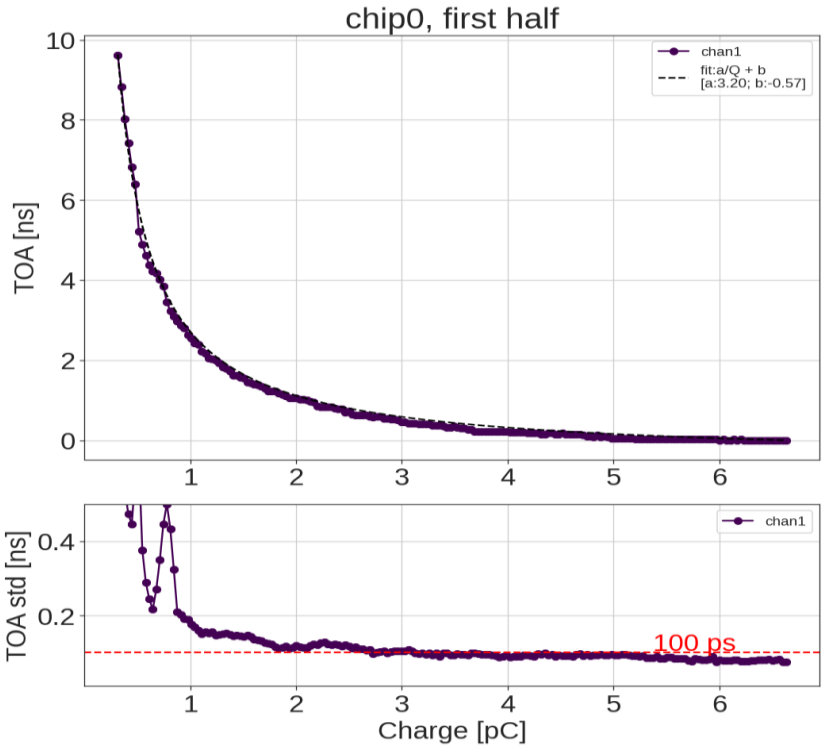
cea Possible design solutions 3

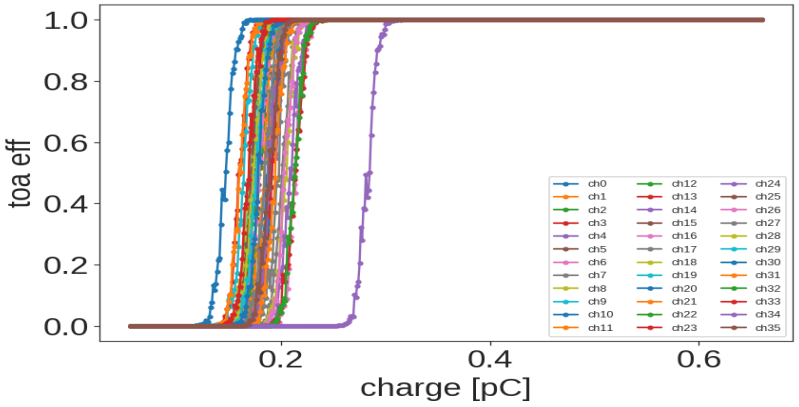
The effect is observed for a lowered supply voltage : extracted CC + C + R with a supply voltage of 1.08V and in the SF -50°C, SF 65°C, SS 65°C and TT corners

SiPM version

- Minor SiPM-specific changes (larger test pulse, Rf range…)
- No specific issue, only ToA/ToT outliers like in Si but no ToT hole







HGCROC3C

- In case metal fix is possible (prefered solution)
  - Process remaining 2 wafers and package them : ~4 months -> oct 24 possible validation of fix
  - In parallel, could launch 75 wafers to feed the MACs : expected dec 24

- In case new engineering run needed (modifying transistors)
  - Minimize modifications to avoid risk
  - Careful simulations and reviews, but complex chip difficult to simulate extensively
  - 20 wafers could be launched in june, packaged chips in ~december

- Important to have CERN support to avoid long delays with IMEC

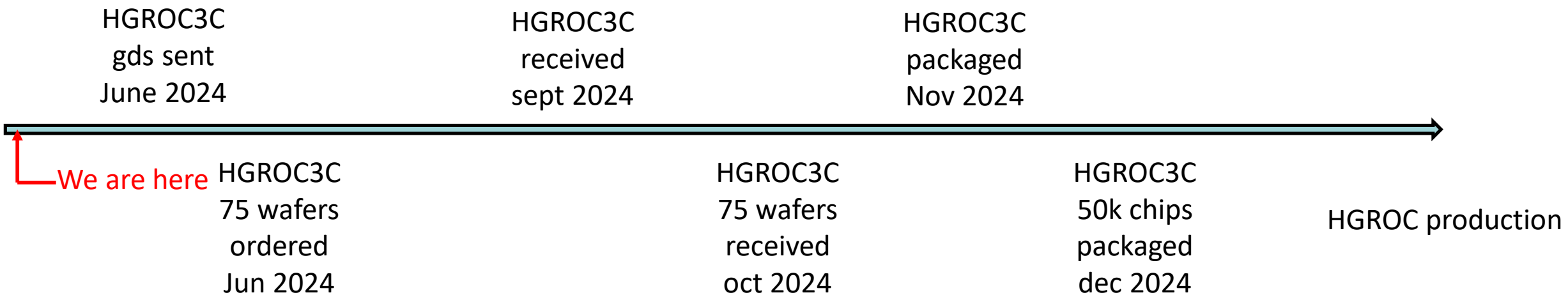
- How to make sure there are no more unseen errors ?
  - Temperature, PS corner measurements
  - 2000 chips measured, bad re-analysed
  - System tests

Schedule 2024

- HGRCO3C ready but verifications still on going
  - Tests with module,
  - Layout being completed mid may 2024

- Tender for packaging in preparation

- Preproduction of HGCROC3C
  - 75 first prod wafers ordered june/july arrive dec 24
  - Remaining 175 wafers ordered jan/feb 25 arrive july 25



HGCROC3B summary

- Substrate now chosen : separated ground. Better TOA threshold and crosstalk

- HGCROC3B has seen unexpected delay and new issues in TDC
  - C4 bumps missing (IMEC)
  - Gap in ToT and ToA outliers (modifications to address TID weakness in 3A)

- HGCROC3C being prepared
  - Metal fix would save 1-2 months and ~200k
  - Submission expected may/june 24

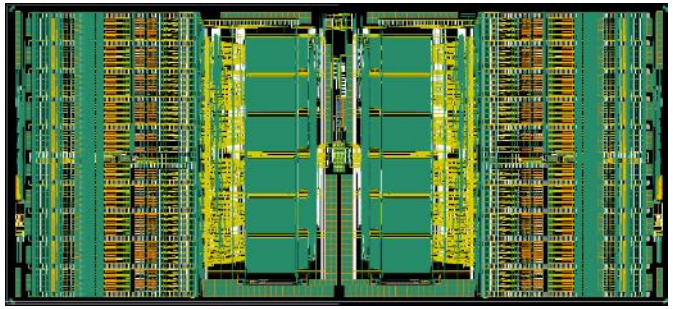
- Measurements continuing
  - Statistics with robots and analysis of bad chips
  - Measurements on modules
  - Irradiations : TID, SEEs, HI

CALOROC1

- SiPM readout calorimetry : CMS H2GCROC with EIC readout (200 MHz clock and fast commands)
  - SiPM from 500 pF to 2.5 nF (or 10 nF)
  - ~5-10 mW/channel

- 2 versions : conservative and exploratory
  - CALOROC1A : Conservative : uses H2GCROC (ADC, TOT) as it is and replaces the backend
  - Status : analog part complete, digital in progress
  - Digital is now « freezing » clock speed and fast commands assignement
  - CALOROC1B : Exploratory : new analog part (dynamic gain switching).
  - Pin to pin compatible
  - Backend « à la HKROC » : auto-triggered, zero-suppressed
  - 40 MHz internal clocking (ADC, TDCs)
  - Status : simulations in progress

HKROC



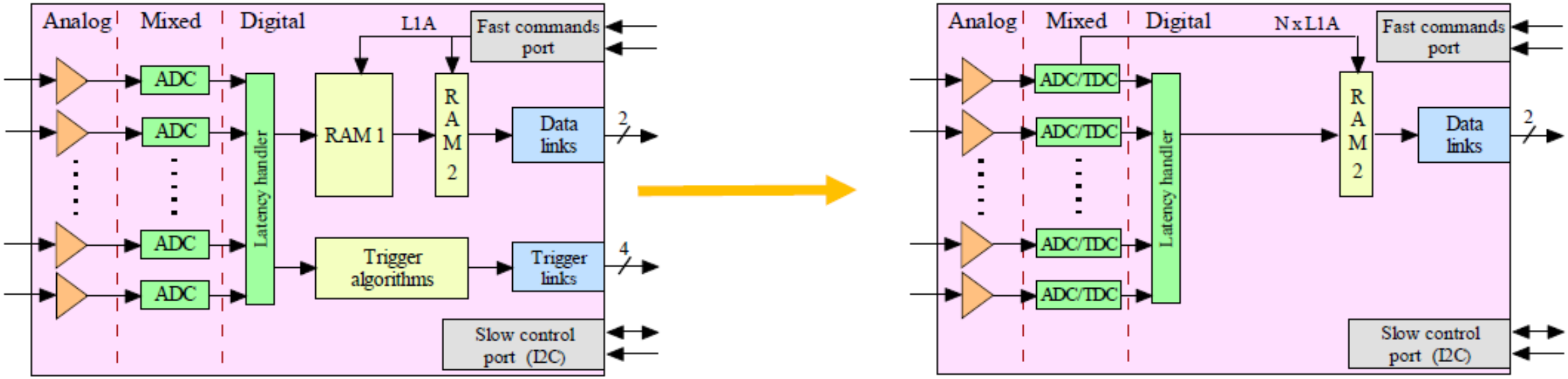
- Channel number tbd : 32 (HKROC) or 64 (HGCROC)
  - Cost issue and pin/pin compatibility with prototypes

- « Si » version considered for HRPPD and/or strips

backup

Evolution for EIC readout [F. Dulucq]

- Data streaming : auto-trigger and zero-suppress



- Each event passing the threshold is readout
- Auto-trigger with N "samples" (1 to 7)
- Can be exercised with present HGCROC (multiple L1A-triggers)