eRD109 progress report
dRICH RDO design @INFN Bologna

P. Antonioli, D. Falchieri, G. Torromeo (INFN – Bologna)

but… a lot of other people contributing in Bologna (L. Rignanese and R. Preghenella among others) and also from INFN-TO (F. Cossio, M. Mignone G. Dellacasa) and INFN-FE (R. Malaguti). Truly a joint project!

Update on dRICH RDO design (April activity)

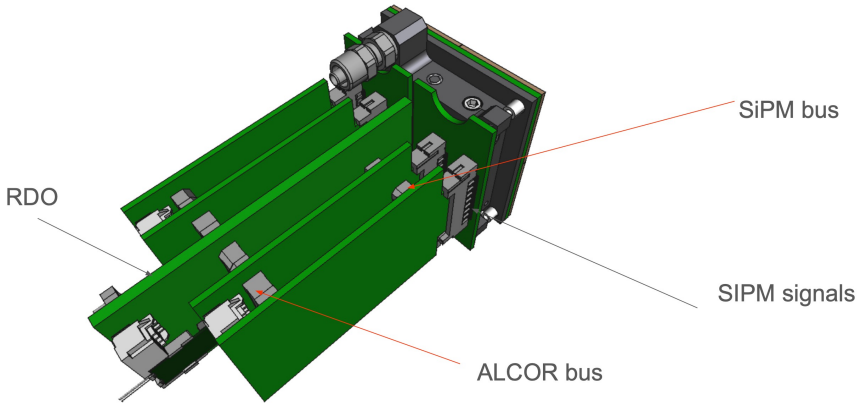
- challenging constraints on dimensions for dRICH (4x9 cm)
- design for schematics/selection of components **in advanced progress**
- Inclusion of VTRX in firmware design just **started**
- delivered 10 AU15P (Artix)
- delivered 10 MPF050T (PolarFire)

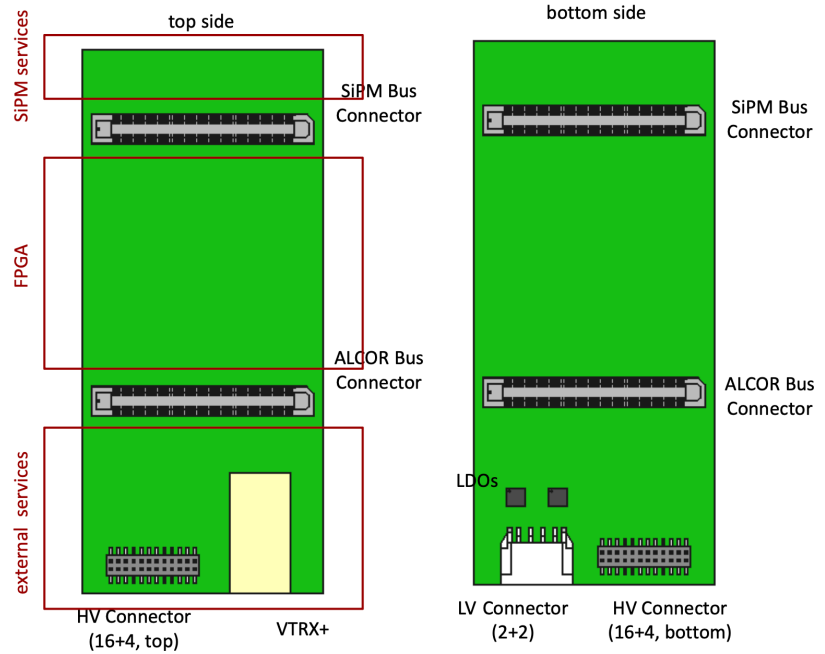
Current components candidates:

- Main FPGA: Xilinx AU15P-SBVB484
- Opt. tranc. VTRx+ + additional oscillator at 125 MHz
- Scrubber FPGA: Microchip MPF050T-FCS9325
- QSPI Flash: MT25QU01
- Samtec connectors (SiPM bus: ERF5-020-05.0-L-DV-TR and AlcorBus: ERF5-050-05.0-L-DV-K-T)
- Clock multiplier/jitter cleaner: SkyWorks SI5326 + additional crystal at 114 MHz
- T sensor: AD7416AR3 (close to LDOs and VTRX+)
- 1 MCU: ATtiny 416
- LDOs and current monitor: LTM4709 + LTC3203
- I2C I/O expander: Microchip MCP23017
- ADC for NTC sensors on SiPM carrier: TMP116NAIDRVT or TMP119

Report highlights on:

- design progress: clock distribution
- review request





And… we are currently very busy for May dRICH test beam firmware these days, sorry if we are a little bit slow on RDO!

Jitter attenuator + clock multiplier selection

Si53xx-RM

Table 1. Product Selection Guide

Part Number	Control	Number of Inputs and Outputs	Input Frequency (MHz)*	Output Frequency (MHz)*	RMS Phase Jitter (12 kHz–20 MHz)	PLL Bandwidth	Hitless Switching	Free Run Mode	Package
Si5315	Pin	1PLL, 2 | 2	0.008–644	0.008–644	0.45 ps	60 Hz to 8 kHz	•		6x6 mm 36-QFN
Si5316	Pin	1PLL, 2 | 1	19–710	19–710	0.3 ps	60 Hz to 8 kHz			6x6 mm 36-QFN
Si5317	Pin	1PLL, 1 | 2	1–710	1–710	0.3 ps	60 Hz to 8 kHz			6x6 mm 36-QFN
Si5319	I²C/SPI	1PLL, 1 | 1	0.002–710	0.002–1417	0.3 ps	60 Hz to 8 kHz		•	6x6 mm 36-QFN
Si5323	Pin	1PLL, 2 | 2	0.008–707	0.008–1050	0.3 ps	60 Hz to 8 kHz	•		6x6 mm 36-QFN
Si5324	I²C/SPI	1PLL, 2 | 2	0.002–710	0.002–1417	0.3 ps	4 Hz to 525 Hz	•	•	6x6 mm 36-QFN
Si5326	I²C/SPI	1PLL, 2 | 2	0.002–710	0.002–1417	0.3 ps	60 Hz to 8 kHz	•	•	6x6 mm 36-QFN
Si5327	I²C/SPI	1PLL, 2 | 2	0.002–710	0.002–808	0.5 ps	4 Hz to 525 Hz	•	•	6x6 mm 36-QFN
Si5328	I²C/SPI	1PLL, 2 | 2	0.008–346	0.002–346	0.35 ps	0.05 Hz to 6 Hz	•	•	6x6 mm 36-QFN
Si5366	Pin	1PLL, 4 | 5	0.008–707	0.008–1050	0.3 ps	60 Hz to 8 kHz	•		14x14 mm 100-TQFP
Si5368	I²C/SPI	1PLL, 4 | 5	0.002–710	0.002–1417	0.3 ps	60 Hz to 8 kHz	•	•	14x14 mm 100-TQFP
Si5369	I²C/SPI	1PLL, 4 | 5	0.002–710	0.002–1417	0.3 ps	4 Hz to 525 Hz	•	•	14x14 mm 100-TQFP
Si5374	I²C	4PLL, 8 | 8	0.002–710	0.002–808	0.4 ps	4 Hz to 525 Hz	•	•	10x10 mm 80-BGA
Si5375	I²C	4PLL, 4 | 4	0.002–710	0.002–808	0.4 ps	60 Hz to 8 kHz	•	•	10x10 mm 80-BGA
Si5376	I²C	4PLL, 8 | 8	0.002–710	0.002–808	0.4 ps	60 Hz to 8 kHz	•	•	10x10 mm 80-BGA

*Note: Maximum input and output rates may be limited by speed rating of device. See each device's data sheet for ordering information.

we need two inputs:

- 98.5 MHz from crystal [per se could be also different.. a 40 MHz and we then we apply factor 9/4…, or 80 MHz …]
- 98.5 MHz from EIC CLK
  - in 2024 version also ext input!!, use jumper to select between quartz and ext. input

2 outputs → 1 to ArtixFPGA → fanout x 4 to FEB via FPGA (as in KC705)

CLK signals in Artix:

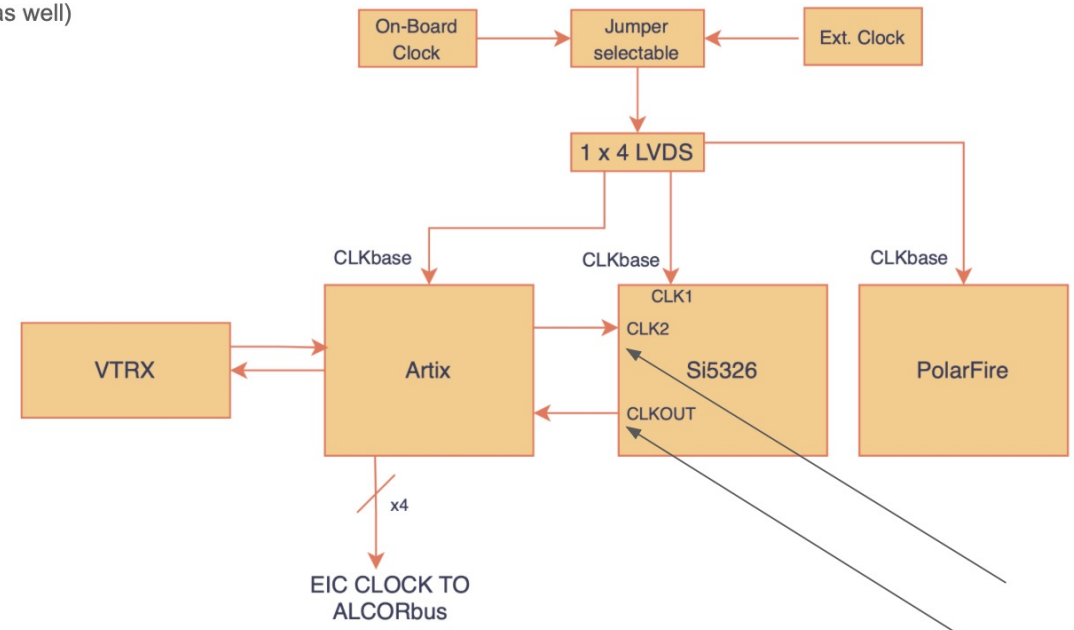
- input from quartz or EXT
- output from Artix to SkyWorks
- input from SkyWorks

Si5326 provides phase adjustments

19

Clock management

On board clock crystal at 98.5 MHz (it could be 80 or 40 MHz as well)



Ext. clock used for sync during test beams when EIC clock not yet available from VTRx link

CLKbase (from on-board clock or ext. clock) is clock source for PolarFire.

Artix-Polarfire-Flash bus works with this clock. This ensures Artix programming at boot, even if VTRx link is down.

reconstructed EIC clock from VTRx @ 98.5 MHz

jitter cleaned + x4 EIC cloc at 398 MHz. Phase can be adjusted via Si5326

All clock signals (single-arrow) are differential pairs

Any feedback/experience on this?

But… : Si5326 (to clean jitter) and Artix (to operate a Gbit link) require additional clocks!

Si5326

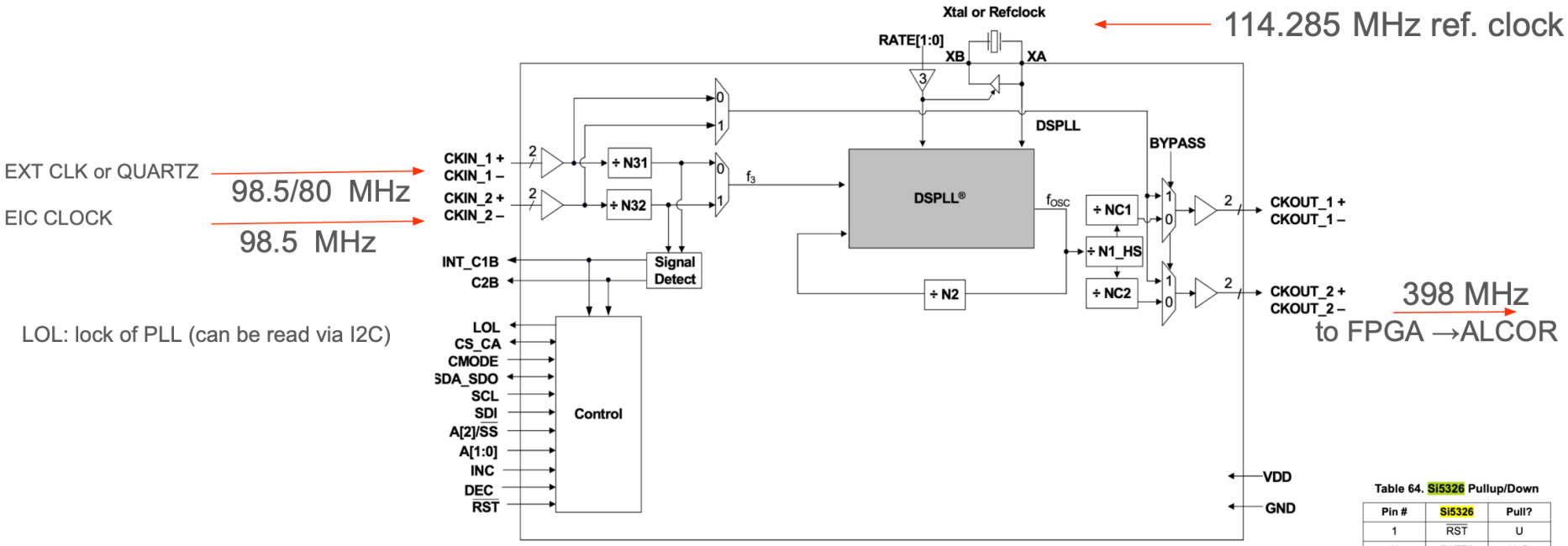


Figure 7. Si5326 Clock Multiplier and Jitter Attenuator Block Diagram

Table 64. Si5326 Pullup/Down

Pin #	Si5326	Pull?
1	$\overline{RST}$	U
11	RATE0	U, D
15	RATE1	U, D
19	DEC	D
20	INC	D
21	CS_CA	U, D
22	SCL	D
24	A0	D
25	A1	D
26	A2_SS	D
27	SDI	D
36	CMODE	U, D

[Si5326 datasheet]

LOS/FOS: lost of signal, frequency offset signal

SI5236 originally suggested by William
Any experience in radiation?

Si5326: reference clock for jitter cleaner

APPENDIX A—NARROWBAND REFERENCES

To provide jitter attenuation, all Si53xx any-frequency jitter attenuating clocks require an external reference. In most cases, this function can be provided by a low cost crystal. The Si5316, Si5317, Si5319, Si5323, Si5324, Si5326, Si5366, Si5368 and Si5369 support two crystal options. For best jitter performance, a 3rd overtone 114.285 MHz crystal is recommended. For relaxed jitter or more cost-sensitive applications, a 37 to 41 MHz fundamental mode crystal may be used. For a current list of qualified crystals, see "Si531x/2x/6x Jitter Attenuating Clock Recommended Crystal List."

Third overtone crystals

Reference Source Selection

The Si53xx reference source is determined by the device RATE[1:0] pin settings as shown in the table below. Use RATE[1:0] = MM for the 3rd overtone 114.285 MHz crystal option. Use RATE[1:0] = LL for the 37 to 41 MHz fundamental mode crystal option.

Table 50. XA/XB Reference Sources and Frequencies

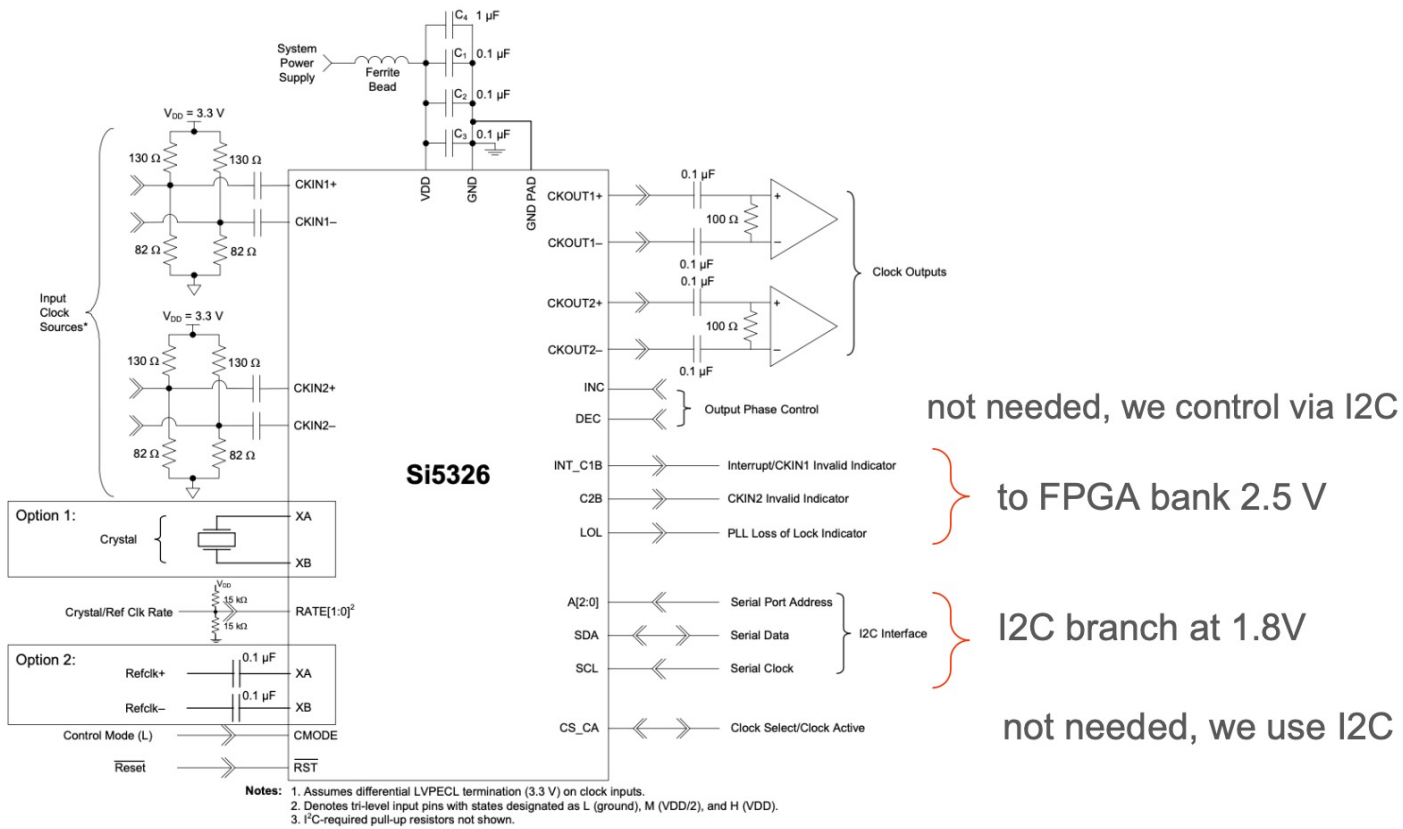
RATE[1:0]	NB/WB	Type	Recommended	Lower limit	Upper limit
HH	WB	No crystal or external clock	—	—	—
HM	NB	Reserved	—	—	—
HL	NB	Reserved	—	—	—
MH	NB	External clock	114.285 MHz	109 MHz	125.5 MHz
MM	NB	Third overtone crystal	114.285 MHz	—	—
ML	NB	External clock	57.1425 MHz	55 MHz	61 MHz
LH	NB	Reserved	—	—	—
LM	NB	External clock	38.88 MHz	37 MHz	41 MHz
LL	NB	Fundamental mode crystal	40 MHz	37 MHz	41 MHz

Dimensions (mm): all 3.2 x 2.5 mm except AVX (which is not 3OT) which is 2x1.6 mm package

Certified crystals by SkyWorks:
https://www.skyworksinc.com/-/media/Skyworks/SL/documents/public/reference-manuals/si531x-2x-6x-reference-manual.pdf

Manufacturer	Part Number (3.2 x 2.5)	Website	Stability (± ppm)	Accuracy (± ppm)
Abracon	ABM8-116-114.285MHZ-T	www.abracon.com	20	20
AVX[2]	CX2016DB114M2P0HPLC1	http://www.kyocera-crystal.jp/eng/	20	20
Connor- Winfield	CS-023E[3]	www.conwin.com	20	20
Hosonic	E3SB114.285T00M33	www.hosonic.com	30	30
ILSI	ILCX13-114.285000M-2795	www.ilsamerica.com	20	20
NDK	EXS00A-CS00871	www.ndk.com	100	100
NDK	EXS00A-CS00997	www.ndk.com	20	20
NDK	EXS00A-CS06528	www.ndk.com	20	20
Pericom	FLB420004[4]	www.pericom.com	20	20
Rakon	514324	www.rakon.com	20	20
Rakon	513553	www.rakon.com	100	100
Taitien	S0242-X-003-3	www.taitien.com	20	20
TXC	7MA1470002	www.txc.com.tw	20	20
TXC	7MA1472001[5]	www.txc.com.tw	100	100
Vectron	VXM7-1074-114M285000	www.vectron.com	100	100
Vectron	VXM7-1191-114M285000	www.vectron.com	20	100

Si5236 connections



not needed, we control via I2C

to FPGA bank 2.5 V

I2C branch at 1.8V

not needed, we use I2C

we need to drive this at 1.8V

RDO SoW - Milestones status & outlook

- Design and realisation of a specific ePIC RDO card prototype, housing a FPGA, LDO, optical transceiver and I/O and LV power connections to provide the read-out to four ALCOR v3 ASIC. A high degree of integration is foreseen between the RDO card and the 4 FEBs that will house each an ALCOR64 v3 chip.

- as per report design is in progress, no major show stoppers identified

- Realization of a RDO card ePIC-compliant for the ALCOR readout: 10/2024

- on target, schematics should go to ext. company for layout in May. Delivery in October possible. Full FW development/test will go beyond 10/24!

Next steps:

- Discussion with FEB team to consider direct routing of SIPMbus to FEB. If agreed this will simplify RDO layout
- Inclusion of Flash and Polarfire connections in firmware design
- Finalize design → "EIC/ePIC review?" (we believe we would benefit of a closer look from experienced people in the community: William, Jeff, Tonko and Jo obvious candidates but conveners to lead…)