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Status report of the eRD109 project on SALSA chip development

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EPIC DAQ/electronics WG meeting

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SALSA CHIP TARGET SPECIFICATIONS

Versatile front-end characteristics

- Dedicated to MPGD detectors and beyond
- 64 channels
- Large input capacitance range, optimized for 50-200 pF, reasonable gain up to 1nF
- Large range of peaking times: 50-500 ns
- Large choice of gain ranges: 0-50, 0-250, 0-500 fC or 0-5 pC
- Large range of input rates, up to 100 kHz/ch with fast CSA reset (limit assumed for EPIC: 25 kHz/ch)
- Reversible polarity
- Front-end elements can be by-passed

Digital stage

- Fast sampling ADC for each channel on 12 bits (> 10 effective bits) at up to 50 MS/s
- Possibility under study to double rates by coupling pairs of channels
- Integrated DSP for internal data processing and size reduction, treatment processes to be selected according to user needs
- Continuous readout compatible with streaming DAQ foreseen at EIC, triggered mode also available
- Several 1 Gb/s output data links

General characteristics

- ~1 cm² die size, implemented on modern TSMC 65nm technology
- Low power consumption ~ 15 mW/channel at 1.2V
- Radiation hardened (SEU, TID)

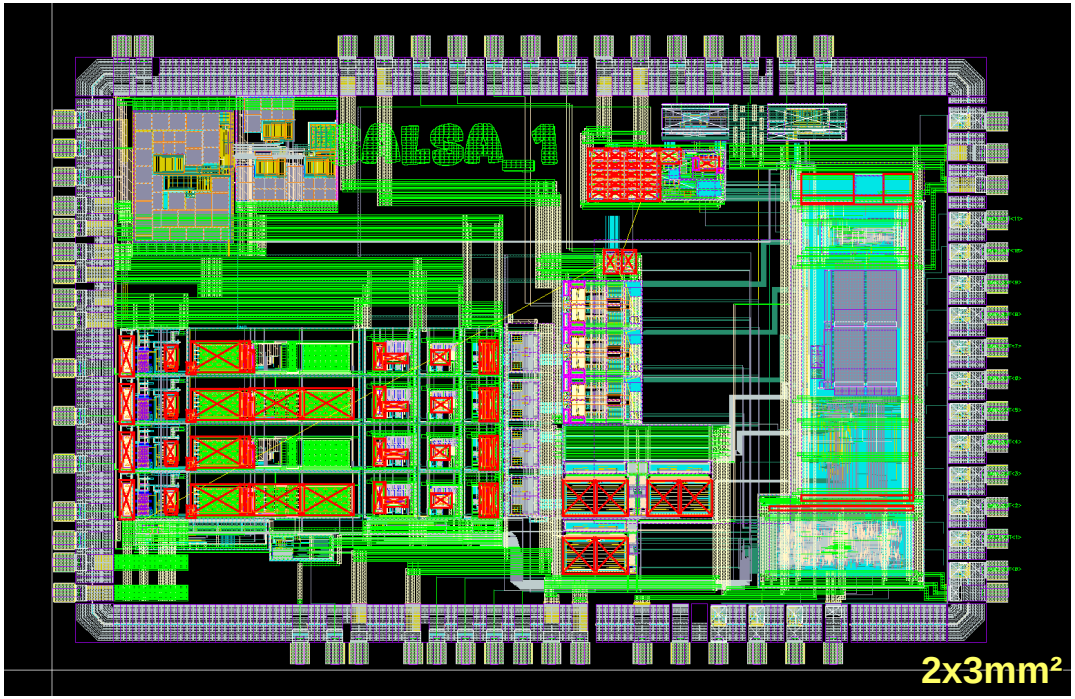
LAST UPDATES ON SALSA PROTOTYPES

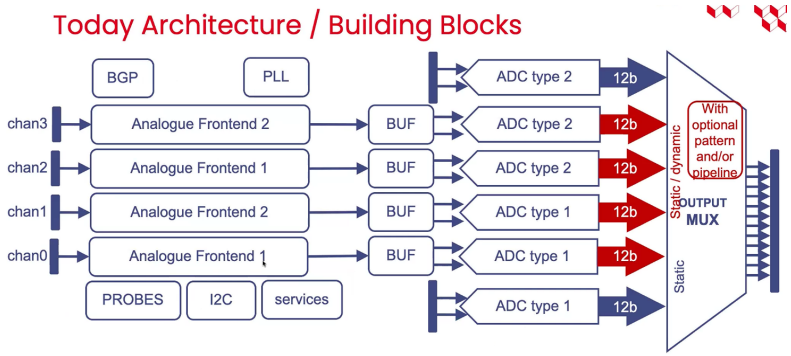
PRISME

- Tests were suspended as peoples were busy with SALSA1
- Being resumed from now

SALSA1

- Design submitted April 19th, request from IMEC (TSMC representative) to do some corrections
- After some exchanges with IMEC, corrected design accepted on April 29th
- Production now ongoing, delivery in 4 to 6 months
- In between, work starting on packaging and test-bench





STATUS OF SALSA2 DEVELOPMENT

Purpose and architecture

- Like final SALSA but with reduced number of channels - 32 ?
- Implement full chip architecture including DSP and input/output interfaces in a version close to the final one

DSP and output interface

- Features discussed at the common DAQ/electronics + MPGD meeting April 18th
- Allowed to clarify some points: monitoring of reconstructed data, trigger management, calibrations, data format, etc...
- Front-end specifications to be slightly adapted to MPGD needs, in particular for intermediate gain ranges, to be discussed
- We plan to freeze DSP and interface specifications end of June, inputs to be given before
- Study ongoing to determine internal buffer sizes needed and estimate output bandwidth, taking into account realistic hit rates from detectors. Model in Python written to simulate internal behavior of DSP

Input interface

- Unified input interface proposed, combining clock + synchronous commands + slow-control in one diff line, under study
- Synchronization of chip with EIC/EPIC time structure, connection with DAQ commands, etc... still to be clarified

Expected to be submitted end of first trimester 2025

PROJECT MILESTONES AND NEXT STEPS

eRD109 FY23 project milestones

- Specifications of SALSA1 design → done
- Production of SALSA1 prototypes → submitted
- Packaging and test card production → expected Autumn 2024
- Performance evaluation → expected end of 2024 / beginning of 2025

Milestones of generic R&D program for EIC project (new 65nm PLL block)

- PRISME prototype submission → done July 19th 2023
- Packaging and test card production → done February 2024
- Radiation tests → Summer 2024 ?

eRD109 FY24 project milestones

- SALSA2 specifications → July 2024
- SALSA2 submission → March 2025
- Beginning of SALSA2 tests → September 2025

Very next steps

- SALSA1 packaging and test-bench → preparation in progress, to be ready Autumn 2024
- Tests on PRISME prototypes → restarting
- SALSA2 specifications and architecture → in progress, to be ready Summer 2024