Status of the eRD109 “RDO/Timing/Service Hybrid”

EPIC DAQ Meeting, 02-May-2024

Wei Li, Mike Matveev, Tonko Ljubicic (Rice University)

William Gu (Jlab), as an external contributor and interested party

Zhenyu Ye (LBL)

Prithwish Tribedy, Prashanth Shanmuganathan (BNL)

Status as of today

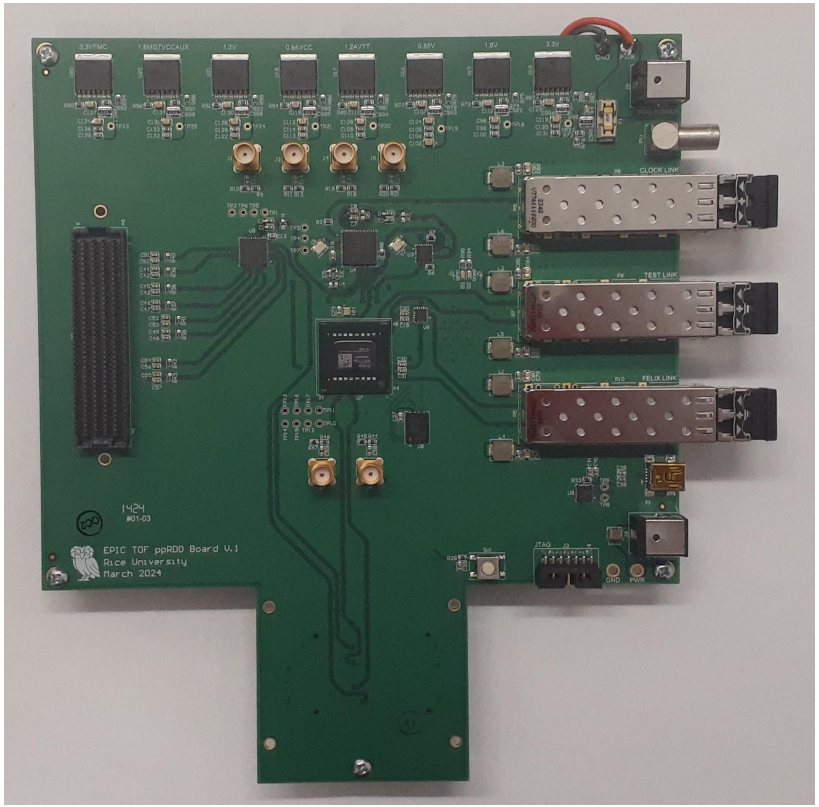
	Feb 1	Mar 7	Apr 4	May 2, 2024 (today)	In Proposal
Schematics	90%	100%	100%	100%	Jun 1
0th firmware	90%	100%	100%	100%	–
Purchase long-lead items	0%	100% FPGA 90% others	100%	100%	Jun 1
Board layout	50%	90%	100%	100%	–
PCB design	0%	50%	100%	100%	Aug 1
Boards complete	–	~end April	Apr 18 (expected) 6 boards	Received all 6 boards Production complete	Sep 31

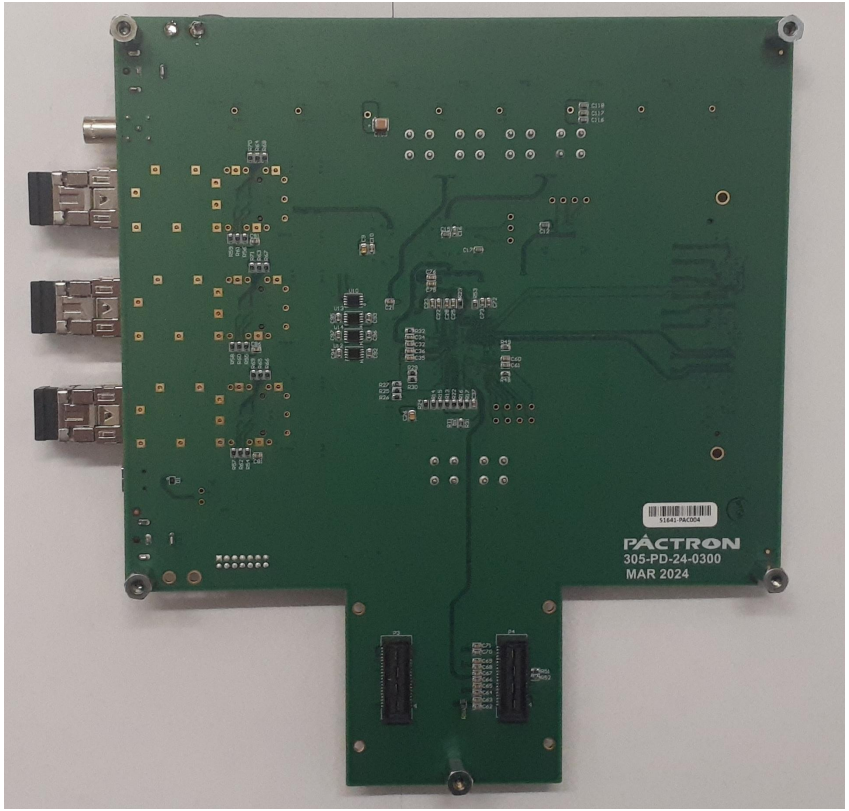
⇒ comfortably ahead of schedule

Board status

- 5/6 boards work well
  - power OK, FPGA programming OK, PROM OK, PLL I2C programming OK, all clocks OK…
- 1 board with bad FPGA – sent back and will be fixed
- Minor issues
  - schematics error: swapped AC coupling caps and terminating resistors between PLLs ⇒ easy fix by hand
  - 1 SMA debugging connector of 1 board has a short to GND ⇒ not fixed, we don't use it
- 2 boards shipped to WG & TL for firmware development
- 1 board stays at Rice for tests as well as CMS ETL ETROC integration
- Production Details (previously requested by Fernando)
  - 10 layer PCB
  - single company did the PCB layout design, PCB manufacturing and parts assembly ("Pactron", Santa Clara, CA) with excellent results and on time!
  - **Cost for quantity=6**
    - PCB layout design: $4800
    - parts: $600 per board
    - PCBs & assembly: $4950 + $950 NRE

ppRDO photos

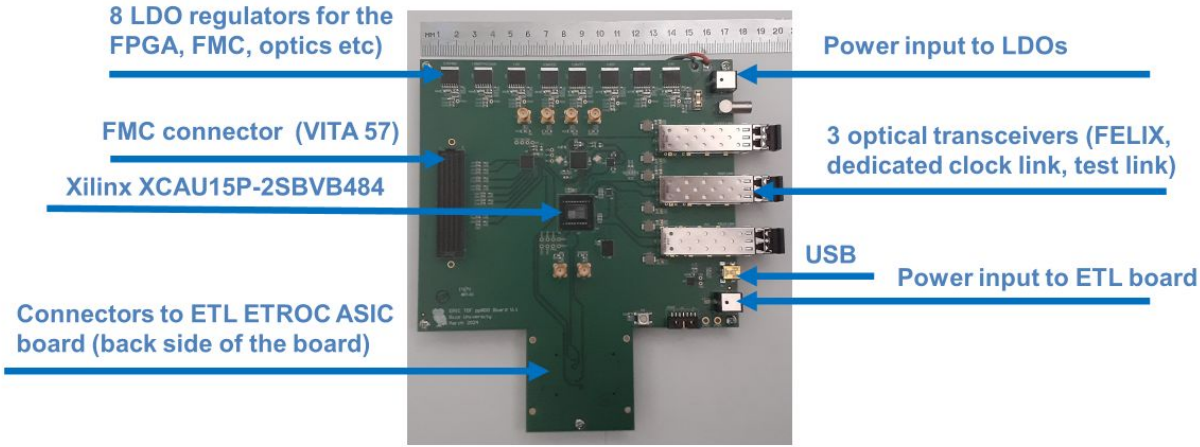




ppRDO Board

From Mike Matveev/Rice

(note components):



❑ Prototype of the TOF Readout Board built with the following goals

- Evaluate various clocking schemes on the board
- Evaluate clock distribution via optical link
- Develop firmware communication protocols with the Readout ASICs and backend
- Evaluate FPGA resources required, power consumption and mechanical constraints

Summary

- Hardware production complete
- Firmware development progressing
  - William/JLAB: fiber protocols, clock recovery
  - TL: framework, I2C interfaces, PLL control, ASIC emulator, readout…
  - Goal: June/July to have all the subroutines & primitives in hand
- Precise power measurements (@BNL & Rice) as the firmware progresses
  - 0th version dummy firmware measured right now at Rice
    - at the PS: 4V @ 1.2 A with all clocks ticking
    - at the regulators
      - 3.3V: 550 mA (but with all 3 SFPs running)
      - 1.8V: 600 mA
      - 0.85V: 100 mA
      - other: too low to measure with the 0th FW
  - measurements will continue as the FW keeps building up