Quick ppRDO status (Mike,William,TL): as of 10-May-2024

- All 6 boards arrived: 5 good, 1 bad FPGA
  - but FPGA was fixed, Mike took it for a spin and now all 6 are OK
  - 1 is with William, 1 is with me, 4 are with Mike
- Tests done (Mike, TL)
  - power OK, FPGA JTAG OK, FPGA PROM and configuration OK (for all 6 boards)
  - PLL I2C ok (found 2 devices), SFP I2C OK (found 1 device)
  - PLL Si5338 programmed and checked, Si5345 programmed and checked, Si53302 setup correctly and checked
    - correct clock counts seen in the FPGA
    - default firmware does the programming through the FPGA pins
  - SFP External loopback tested: clock recovered by Si5345 – looks OK but I need a more serious check. Later.
  - SFP: all SFPs (when connected with fiber loopbacks) see the Link (no LOS)
  - William working on the fiber and clocking scheme (William?)
    - sent fw to Tonko to incorporate it in the framework – TL successfully re-synthesized it on his system
    - TL & William discussing features – in progress…
    - this is the last important step in the pre-testing
  - Xilinx Soft CPU core (Microblaze) implemented
    - USB serial port tested and works (and in use by Mike, TL)
  - Mike connected the ETL board successfully
    - we scanned it on I2C and found ETROC at the right address
    - read/write of some typical registers look just fine
    - next steps – later
- Xilinx Project setup (TL)
  - idea is to create a common project setup so that we (William, TL, others) can simply use it “from scratch”
  - discussed options with William – in progress, expect ~1 week
  - also step-by-step instructions on how to set it up
    - as well as register/bits of the FPGA which I use
- Next steps…
  - William – MGT & clocking (will have a “Data Format on the Fiber” V0.1 from the DAQ Group “soon”)
  - Tonko: ASIC emulator to emulate reasonably precisely up to 32 ASICs per RDO (moving along…)
  - ETL readout (Zhenye, TL?, Mike?)
  - FMC connector stuff: TL will meet with the EPIC Calorimeter Group (Norbert, etc) at CERN next week
    - discuss firmware for the ASIC readout (based on H2GROC currently)
    - discuss options on how to test it (they send their board to Rice, or we send the ppRDO to ORNL – TBD)
  - BNL: detailed power measurement (to be discussed with Prithwish et al)
  - Linux setup in Rice lab so that TL can do remote development on the ppRDO – discussed with Mike – soon
- **Conclusion – Very quick progress! – NO showstoppers seen** 🙂