eRD109 5/8/24

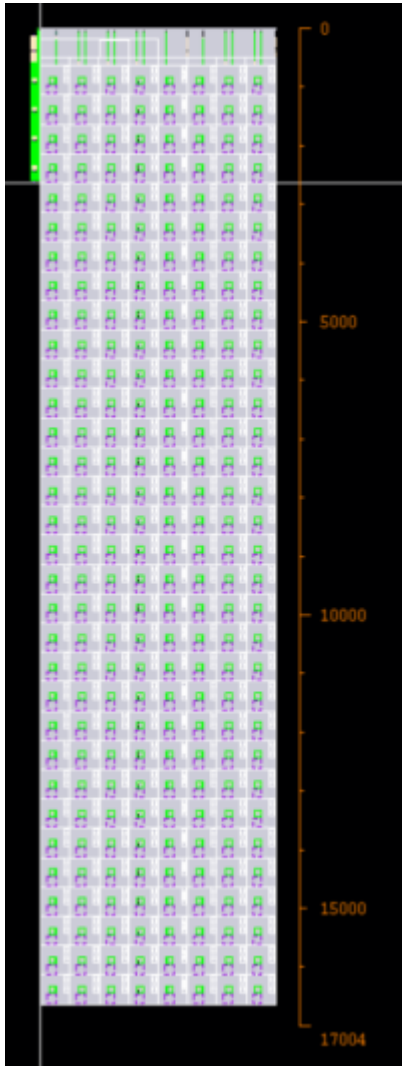
- **EICROC:**
  - **EICROC0 (4x4) being measured. EICROC0A/B to investigate digital noise and reduce ADC power.**
  - **EICROC1 (8x32) layout started, with selective EICROC0-like readout (hit+9 neighboring channels),**
- **FCFD:**
  - **FCFDv1 (6) being tested. FCFDv1 connected to 5mm strip sensors will be tested with beam in May**
- **Low mass FPC (and bonding)**
  - **FPC will be produced with HV, LV to study co-curing with CF modules and mechanical properties**
- **ppRDO:**
  - **6 boards produced and being tested, FW under development.**

Status and plans for EICROC

- EICROC0 still under measurement
  - See https://indico.bnl.gov/event/23162/
  - Triggered readout, all data shipped out : 16 ch * 8 samples ADC + TDC
  - Present power ~2 mW/ch (+ 4*20 mW « analog probe preamp »)
  - New versions prepared 4x4
    - Digital noise investigation
    - ADC power + shaper/driver to be reduced from ~1 mW to 100 µW/ch => EICROC0A
  - EICROC0A/B : simulations and layout in progress

- EICROC1 will address larger dimensions : 8x32
  - Address floor planning and power distribution
  - Selective readout : hit + 9 neighbouring channels
  - Status : layout started based on EICROC0, adding more testability
  - Still EICROC0-like readout

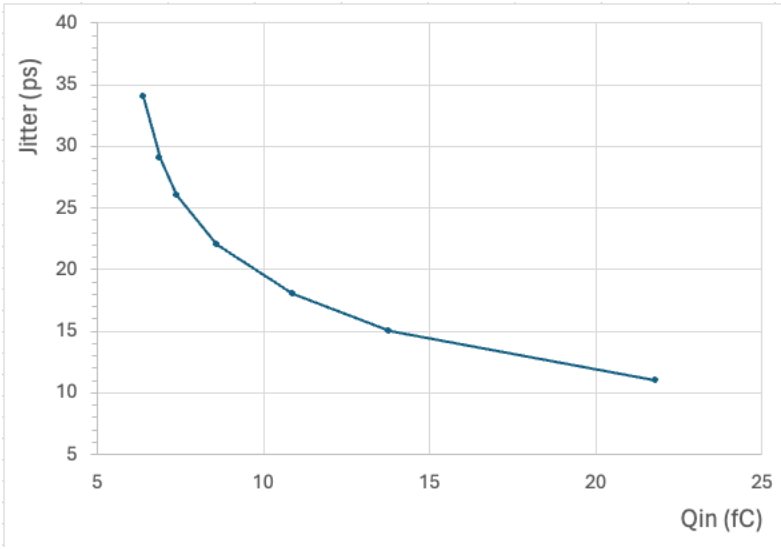
- Submission in ER fall/end 2024



Christophe

Status and Next plans

- FCFDv1 chip is now being tested
  - Measurements with internal charge injections performed with an LGAD-like signal being injected.
  - With input capacitance ~3.5 pF we achieve around 11 ps time resolution
  - The analog output works linearly over the range of input charge from 7 fC to 60 fC, the discriminator flip time output stays constant within around 10 pS



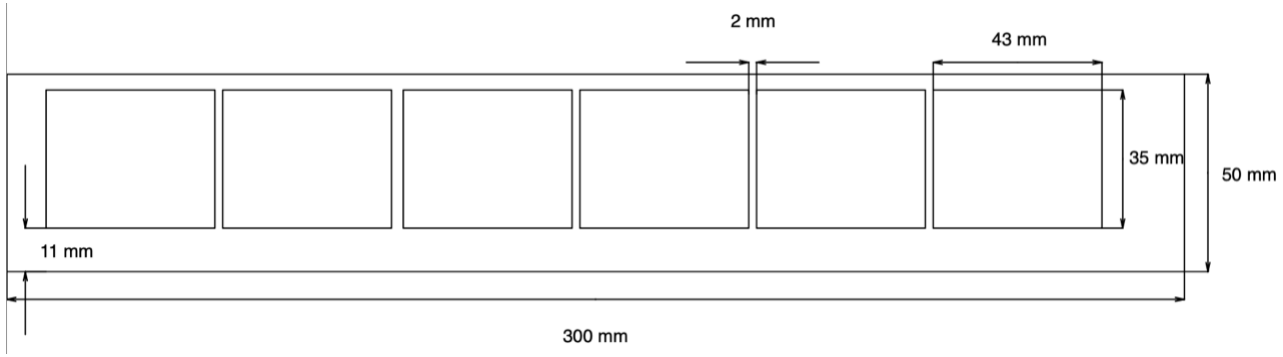
Jitter measurements with 3.5 pf input capacitance and charge injection

- We have now started preparing for the test beam in FNAL in the end of May
- Our measurements of the AC-LGAD strip sensors showed the complex CR-network which complicates operation of the ASIC
  - Additionally, the capacitance for some of the sensors is a lot larger than we originally specified
  - Hamamatsu 5mm E-type strip sensors behave the best so far, and we are now adapting the readout board to optimize performance

Artur

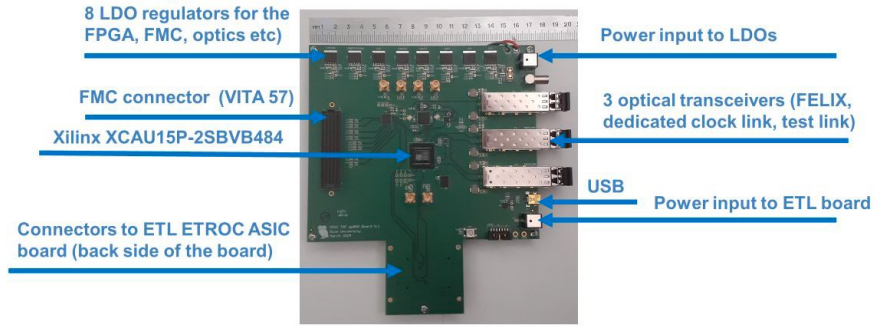
Flex PCB R&D

- LFHCAL Flexes assembled by vendor, will be included in CERN HGCROC Test campaign
  - Not yet tested, on their way back
- First barrel TOF mechanics test structures produced at Purdue
  - Next step: co-cure Kapton flex into 12" carbon fiber structure, bond sensors and Si-heaters onto structure
- Designing test flex for co-curing:
  - LV, HV, maybe some temperature sensors
  - 2 layers first, multi layer for exploration later
  - Produce in different stackups to test mechanical stability and precision (12" within reach of all standard manufacturers)
  - Ideally produced with peel-off kapton film on top to keep ENIG pads clean from resins etc.



Oskar

Summary



❑ Prototype of the TOF Readout Board built with the following goals
- Evaluate various clocking schemes on the board
- Evaluate clock distribution via optical link
- Develop firmware communication protocols with the Readout ASICs and backend
- Evaluate FPGA resources required, power consumption and mechanical constraints

- Hardware production complete
- Firmware development progressing
  - William/JLAB: fiber protocols, clock recovery
  - TL: framework, I2C interfaces, PLL control, ASIC emulator, readout…
  - Goal: June/July to have all the subroutines & primitives in hand
- Precise power measurements (@BNL & Rice) as the firmware progresses
  - 0th version dummy firmware measured right now at Rice
    - at the PS: 4V @ 1.2 A with all clocks ticking
    - at the regulators
      - 3.3V: 550 mA (but with all 3 SFPs running)
      - 1.8V: 600 mA
      - 0.85V: 100 mA
      - other: too low to measure with the 0th FW
  - measurements will continue as the FW keeps building up