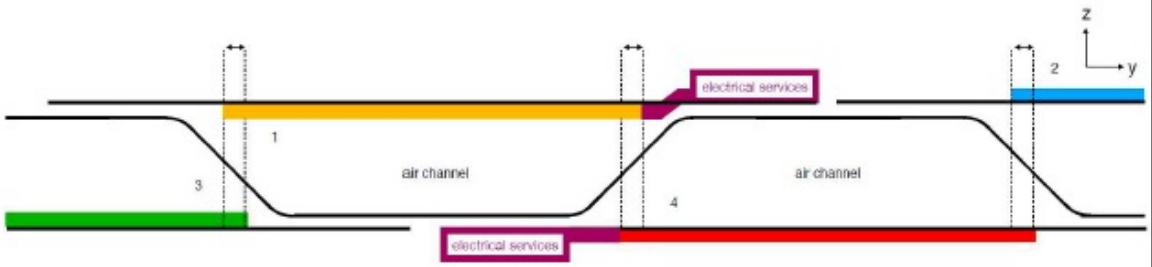


Disk configuration

Disk concept — variant 2; sensor placement



Having a sensor module part of the face-sheets — as shown here — would seem preferred.
 Arguments include that services can be guided to areas with mechanical support

Two module sides or heights would thus result in four sensor planes on the disk — color coded above

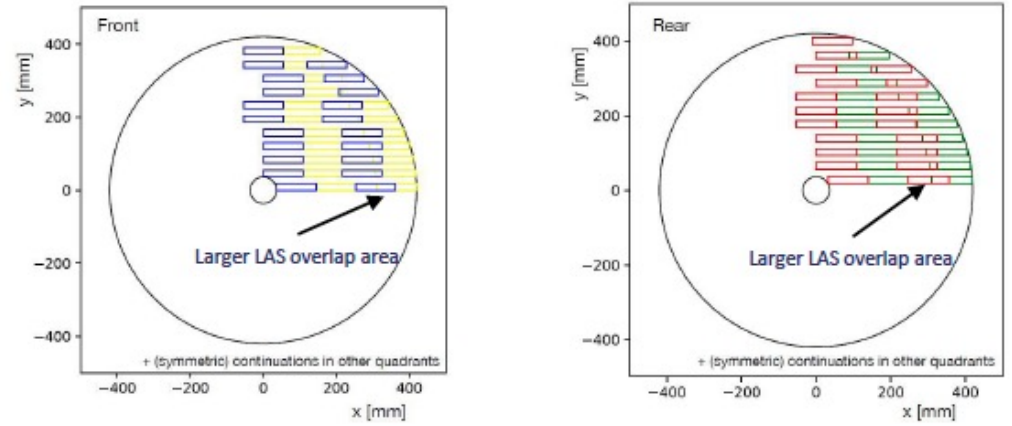
Note:
 Only T5 LAS considered for tiling disks;

LEC overlaps REC like in barrels to increase hermeticity;



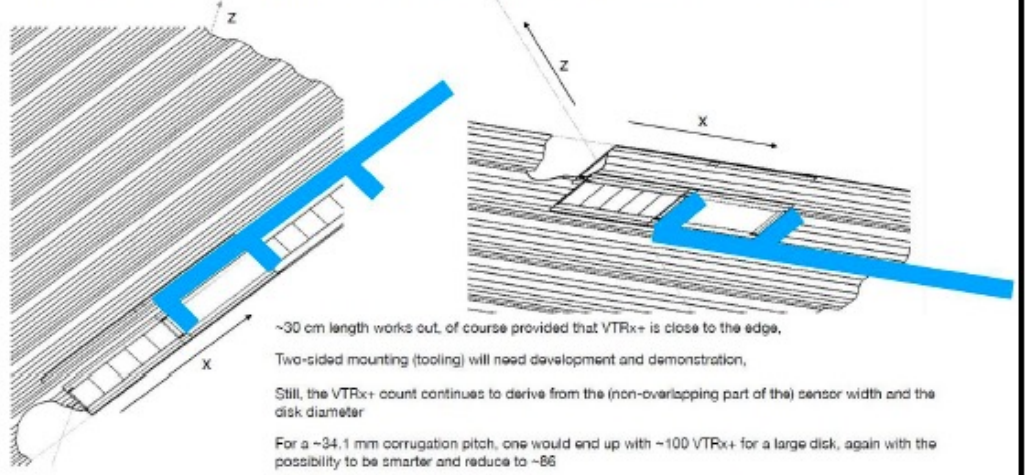
Disk concept — variant 2; tiling

The layout of modules — here with 5 RSUs — onto a large disk could now be done as follows:



Note: algorithm makes some approximations on overlap — not too relevant here.

Disk concept — variant 2; FPC initial thought(s) and VTRx+ counts

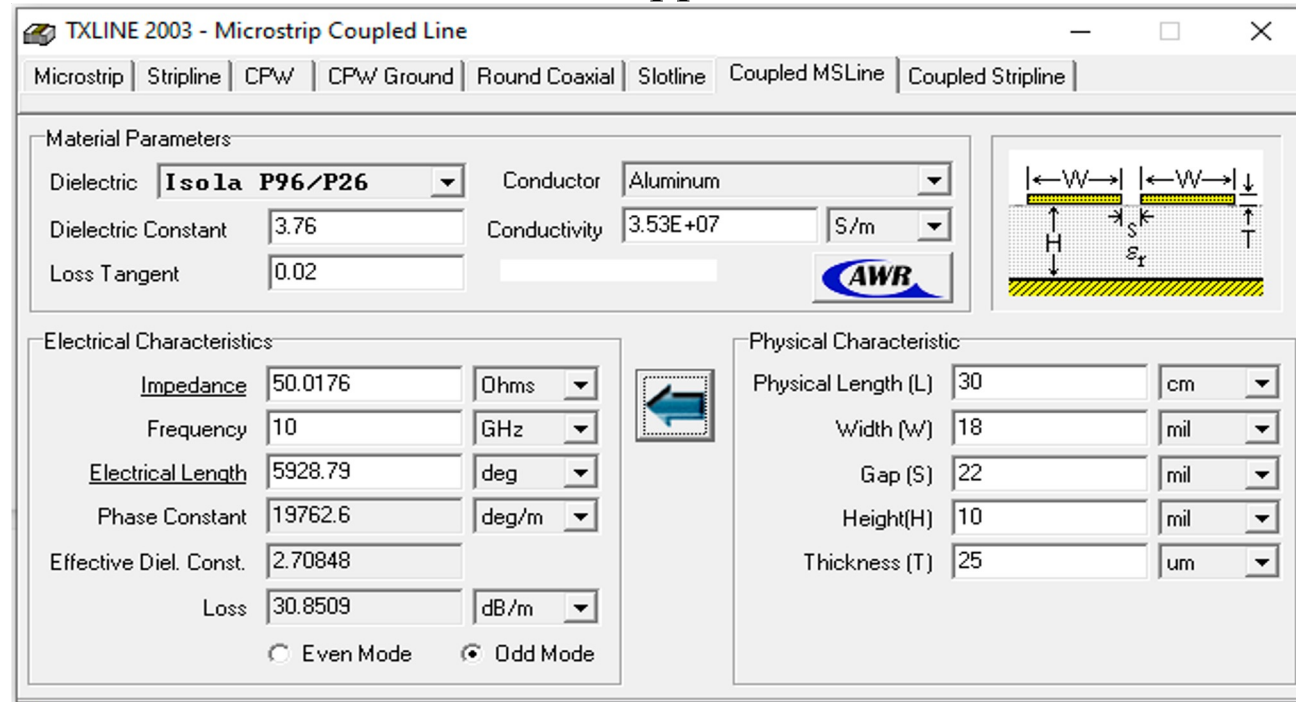


~30 cm length works out, of course provided that VTRx+ is close to the edge,
 Two-sided mounting (tooling) will need development and demonstration,
 Still, the VTRx+ count continues to derive from the (non-overlapping part of the) sensor width and the disk diameter
 For a ~34,1 mm corrugation pitch, one would end up with ~100 VTRx+ for a large disk, again with the possibility to be smarter and reduce to ~86
 i.e. ~30% increase compared to an area-derived estimate; ~720 instead of ~540; length of pig-tails are determined primarily by the inter-disk spacing, the desired end-point, and the max-length (1 m ?)
 Slow-control to be worked out further; OIMbps, i.e. no ~30 cm length constraint. May be multiplexed or grouped across rows (presumably adjacent; considering grouping by up to 8 EIC-LAS).

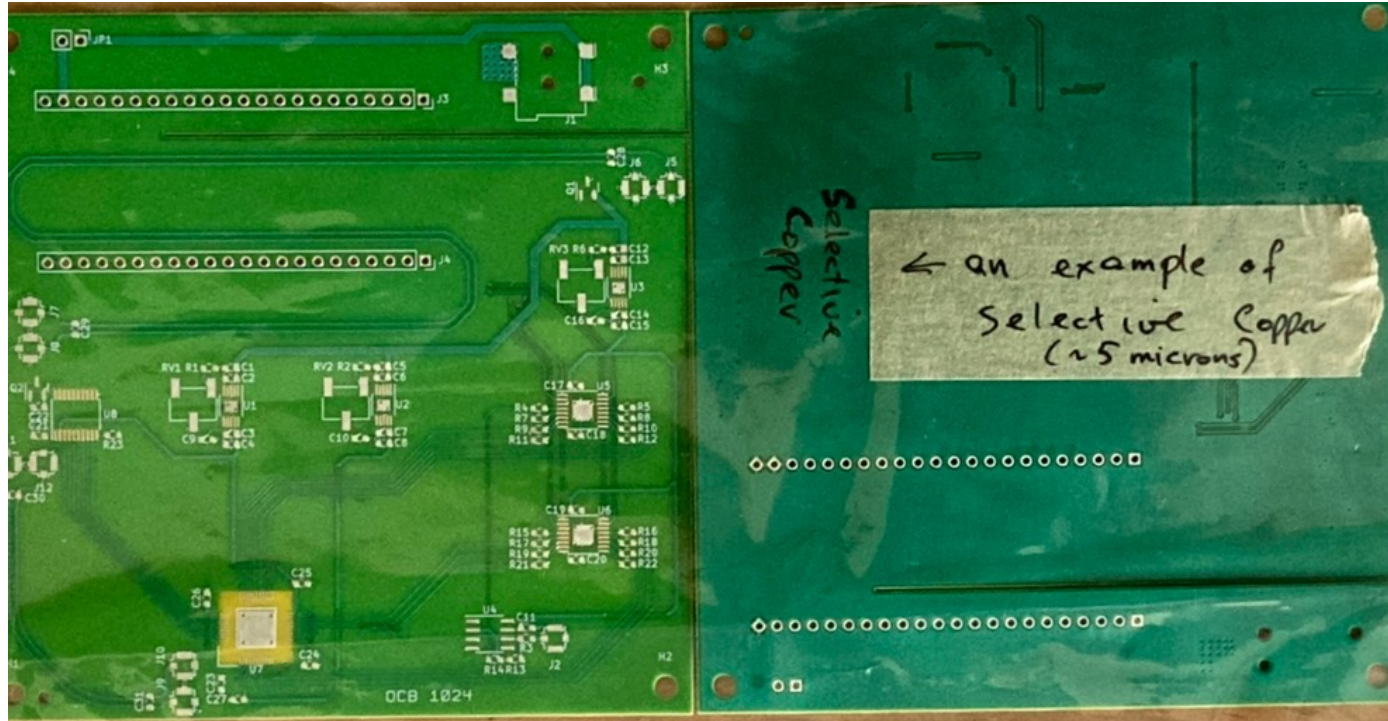
AI-based FPC (Yuan Mei)

Constraints from vendor

- Prefer 1mil thick Polyimide-fiber glass substrate (Isola);
- Prefer 20 μm Al - 8 μm Cu - Polyimide stack. Can be without Cu, but Al - Polyimide adhesion is weak.
- Prefer burying traces between substrates for added strength. 5mil/5mil width/spacing in small area, 7mil/7mil for long traces.
- Not support SMD soldering. Al in a few small places can be plated with 5 μm copper for solder.
- 0.016" wide (minimum) cutout. Plated vias must be copper based.

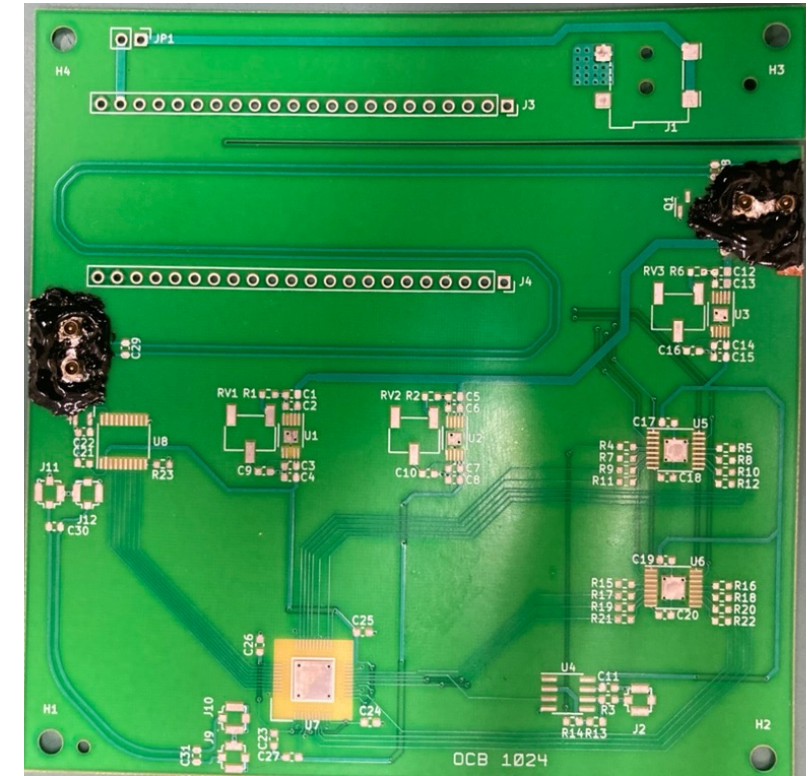
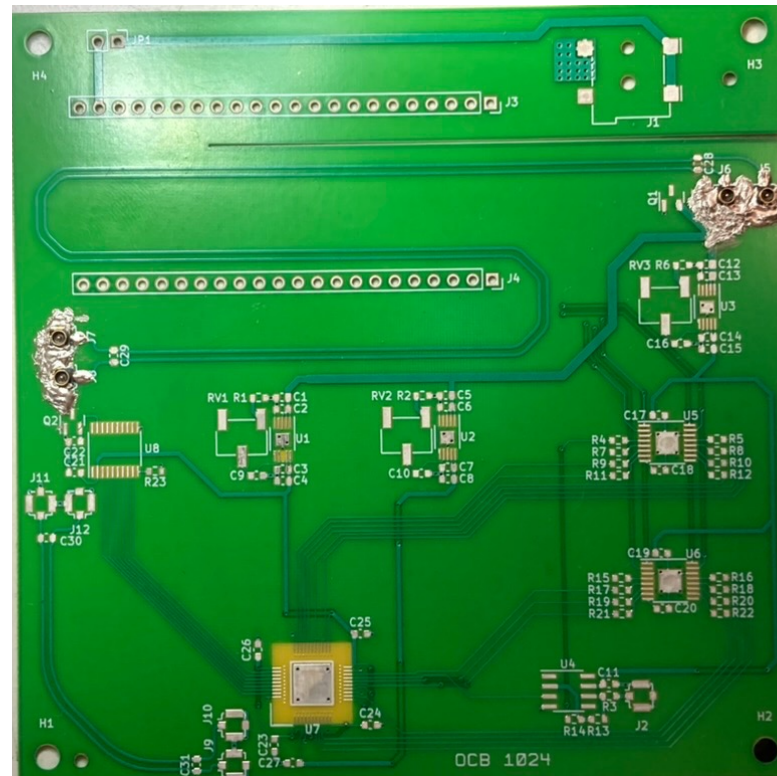
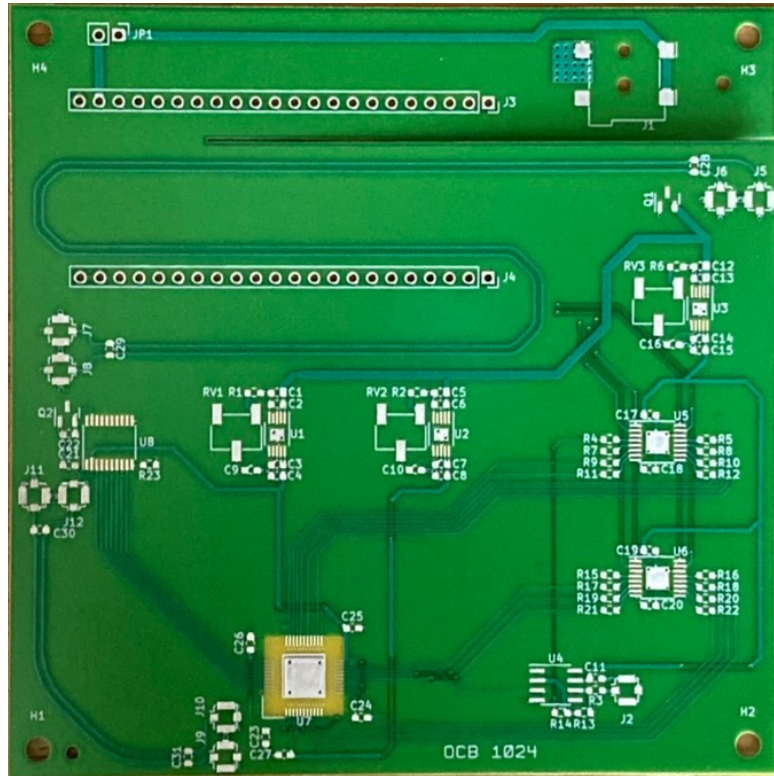


First Low TRL Prototypes



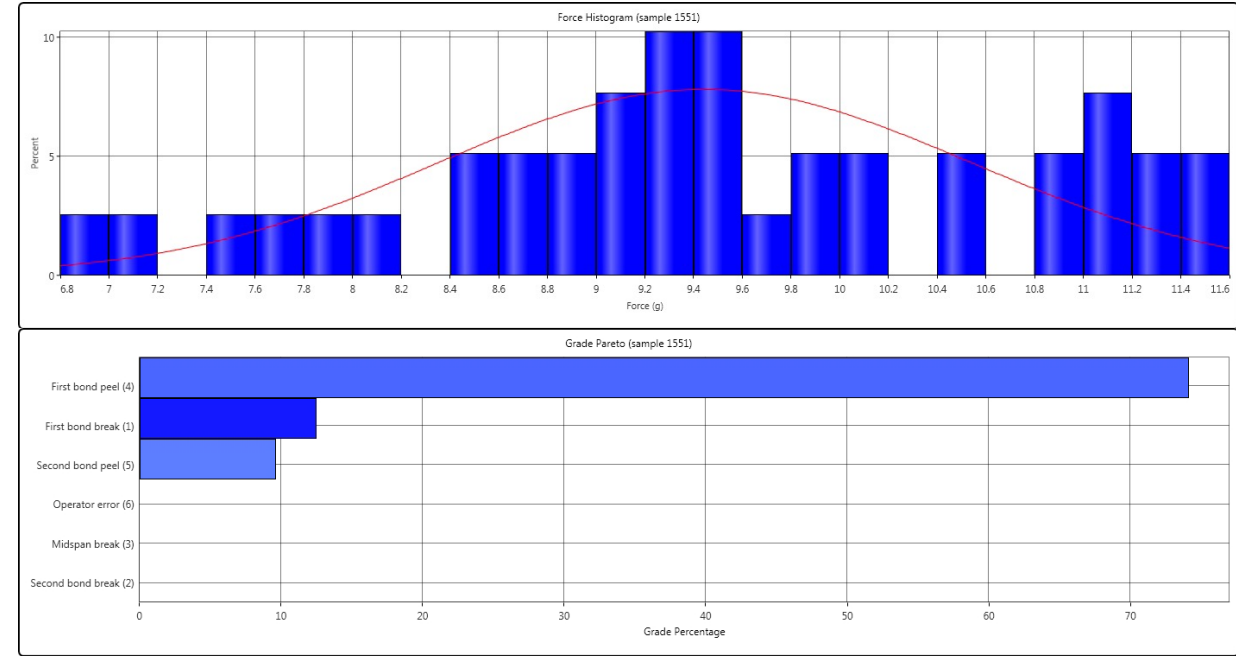
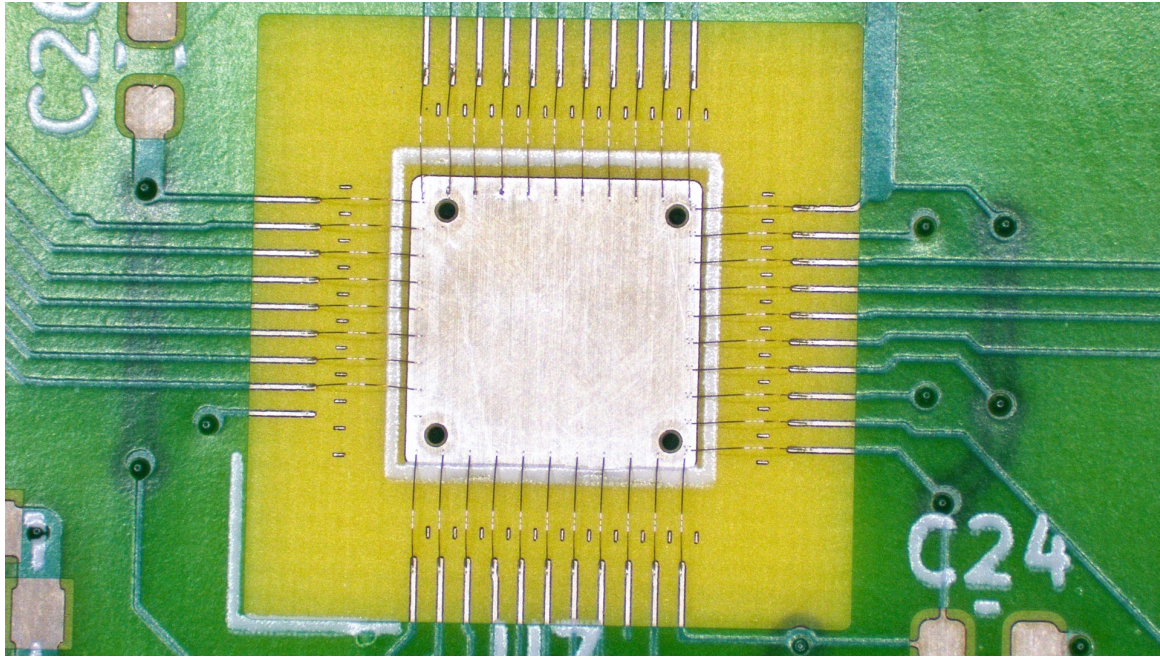
- A PCB design from another project was adapted to produce the first TRL FPC prototype
- 3 prototypes produced, one of them has 5um copper in selective area

First Low TRL Prototypes



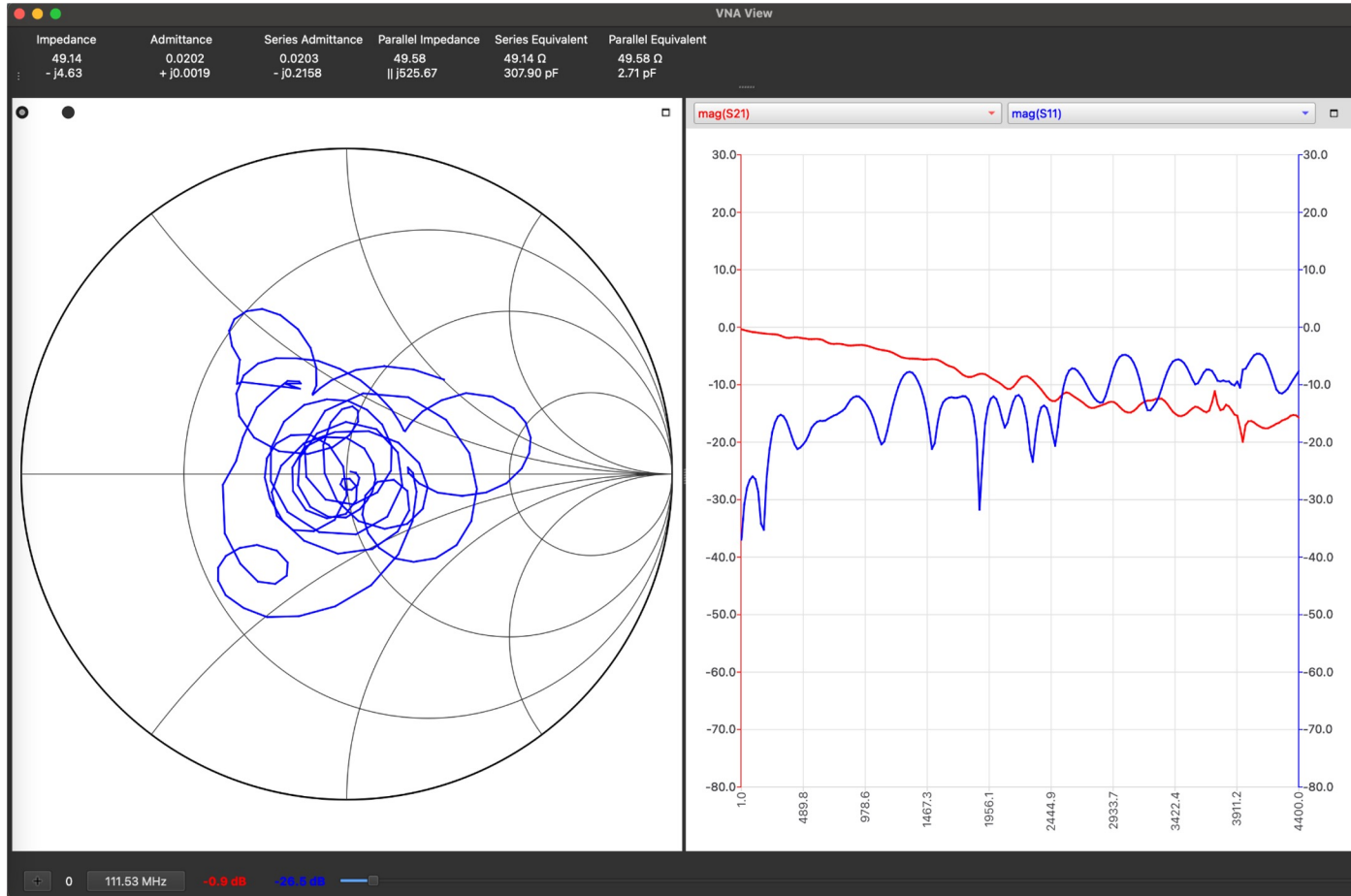
- Connectors were mounted via non-standard methods (removing the soldermask, epoxies).

Wire-bonding and Pull Tests



- Number of tests: 39
- Mean - 3 * standard deviation: 5.7782 g
- Minimum load: 6.9011 g
- Maximum load: 11.570 g
- Mean: 9.5195 g
- Standard Deviation: 1.2471 g

Single-ended VNA Measurements



$$\alpha_d = 0.9106 \times \sqrt{\epsilon_R} \times F_{GHz} \times \tan\delta \quad (\text{dB/cm})$$

	polyimide	ArlonEMD	soldermask
Dk	0.9106	0.9106	0.9106
	3.76	4.3	3.6
	1	1	1
Df	0.017	0.0036	0.025
dB/cm	0.030017	0.006798	0.043194

- More signal loss than expected

Summary and Outlook

- First low TRL prototypes produced and evaluated
 - Based on a PCB design from another project
 - Ok for wire-bonding but not soldering
 - Significant signal loss at high frequency
- Second iteration is being worked on
 - Dedicated for signal transmission investigation to understand and improve signal losses: different substrate materials, different width/pitch, with and without soldering mask
 - Make use of selective Cu plating for soldering, and wire-bonding to connect top and bottom
 - Make plated-thru holes in an all-aluminum stack

