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OB FPC prototyping

WP3 Electrical interfaces



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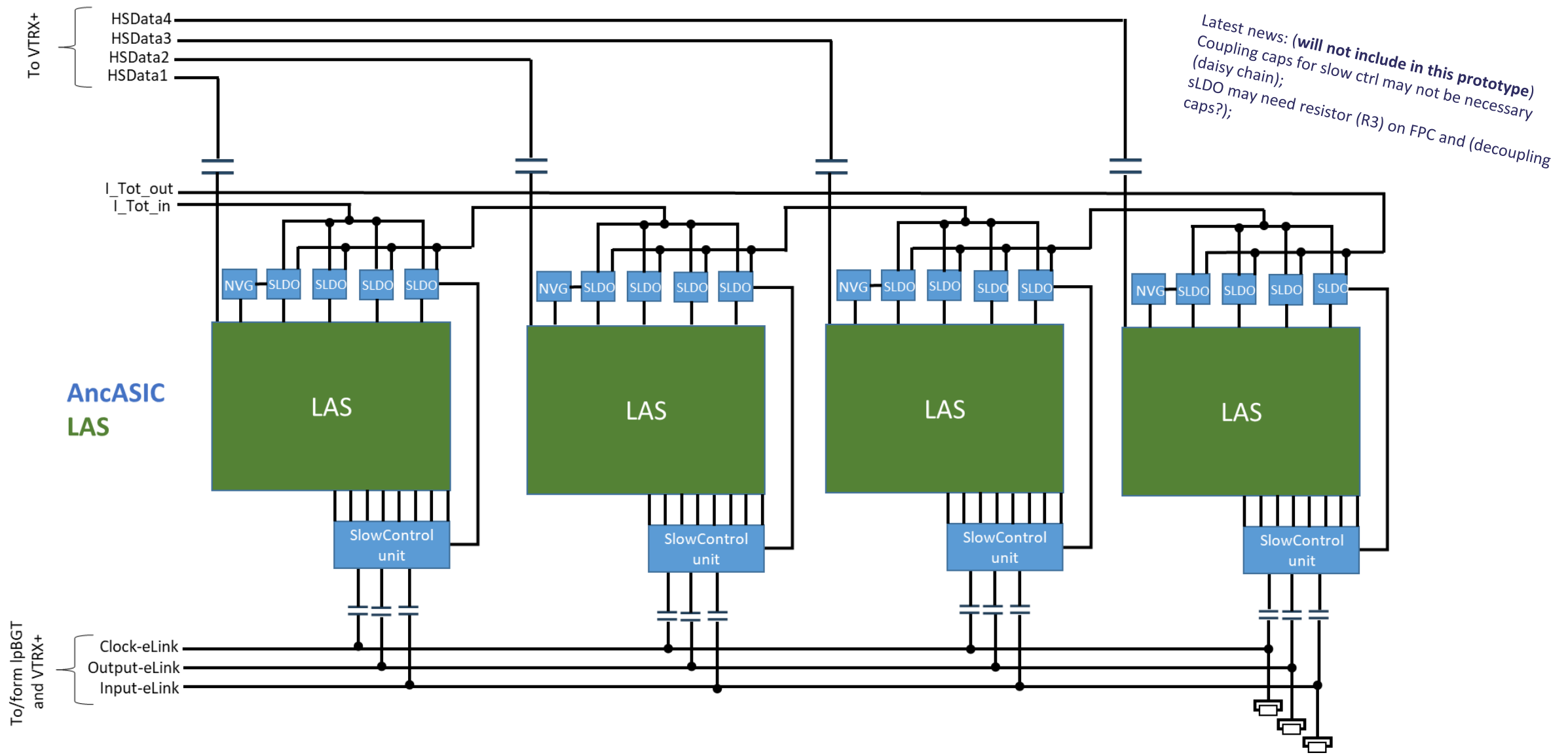
Outline

- Recap of design on low TRL prototyping for OB:
 - Based on a snapshot of project from Feb. 2024;
 - Stave layout;
 - Circuit definition;
 - Signal ratings;
- Manufacturing technology;
- Module layout;

Reporting a snapshot
of the evolutionary development
of the SVT & its components

Stave layout

Circuit definition



FPC connects the AncASIC to the DAQ system and pwr supplies.

Presenting a sequence of 4 sensors.
 [longest sequence in Epic Svt]

Signal ratings

Signal name	Type	Comment	Coupling	Standard	IpGBT eLink	Rate
slow ctrl clk (down)	AC	from IpGBT to AncASIC	Capacitive	CERN Low Powering Signal (CLPS)	clock-eLink	80 Mb/s
slow ctrl write (down)	AC	from IpGBT to AncASIC	Capacitive	CERN Low Powering Signal (CLPS)	output-eLink	80 Mb/s
slow ctrl read (up)	AC	from AncASIC to IpGBT	Capacitive	CERN Low Powering Signal (CLPS)	input-eLink	160 Mb/s
data	AC	from AncASIC to VTRX+ (1 diff line/AncASIC)	Capacitive	CERN Low Powering Signal (CLPS)	N/A	5.12 Gb/s (or 10Gb/s)
voltage supply	DC	Max: (2.5V/AncASIC) * (4 AncASIC)	Direct	10% Vdrop for 2.5V/LAS, is it OK?	N/A	N/A
current	DC	2.5 A (total per AnASIC)	Direct		N/A	N/A

To check: Is voltage supply still 2.5V ? (1.8V?)

To check: Is current supply still 2.5A ? (worst case)

Manufacturing technology

Supplier RPE LTU

Updated preliminary design: unfolded assembled FPC

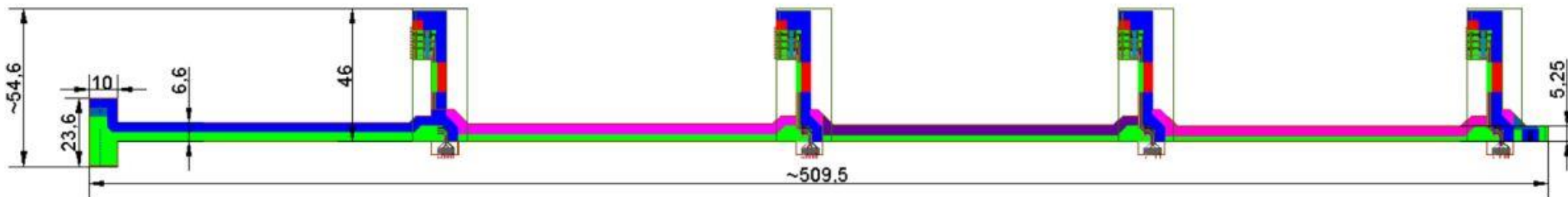
Base cross-section of M-FPC and B-FPCs

Cover layer (insulating)	Glue ~5um	PI 12.5 (25)um	Kapton	Ni-SnBi (for soldering)
Top Layer (signals)	Glue ~5um	Al 14um	FDI-A-24	
Spacer	Glue ~5um	PI 10um	Kapton	
Bottom (GND)	Glue ~5um	Al 14um	FDI-A-24	
		PI 10um		

Composition of the assembled FPC:

- a) Main FPC (M-FPC in short) – 1pc
- b) Bridge FPC (B-FPC in short) – 4 pcs (same FPCs)

Schematic cross-section



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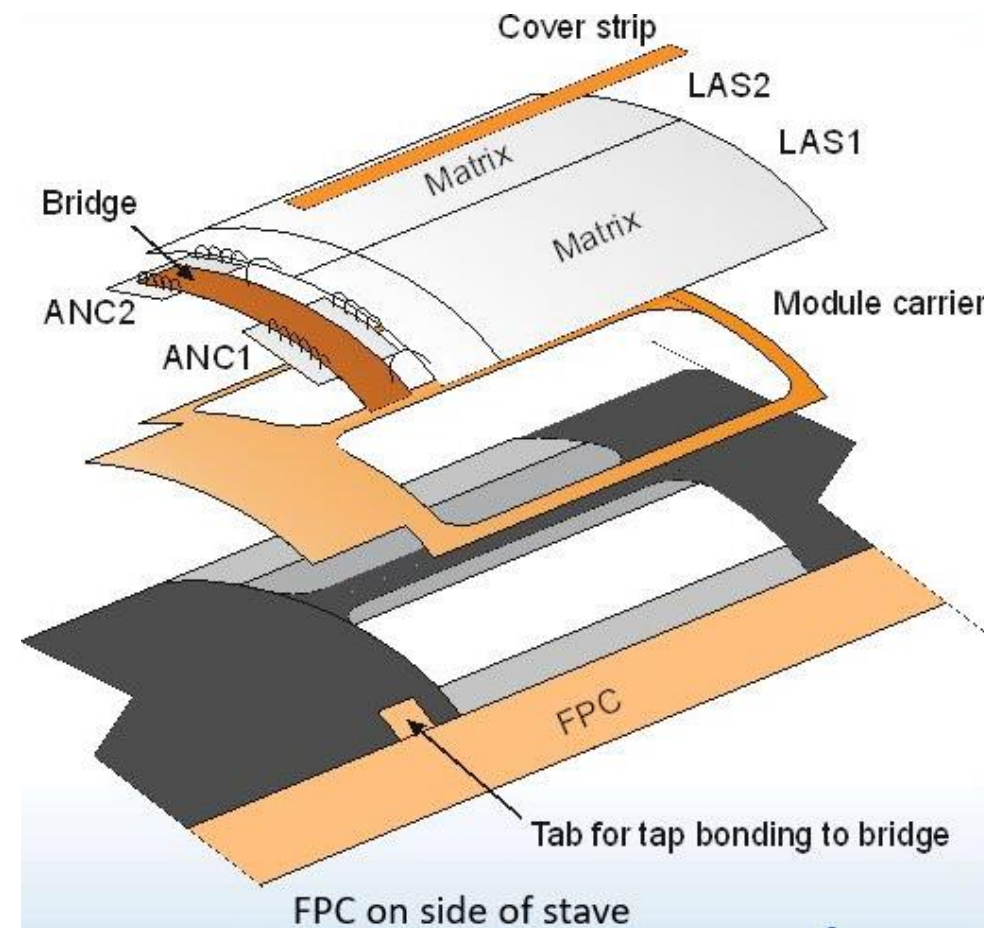
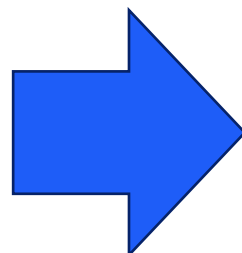
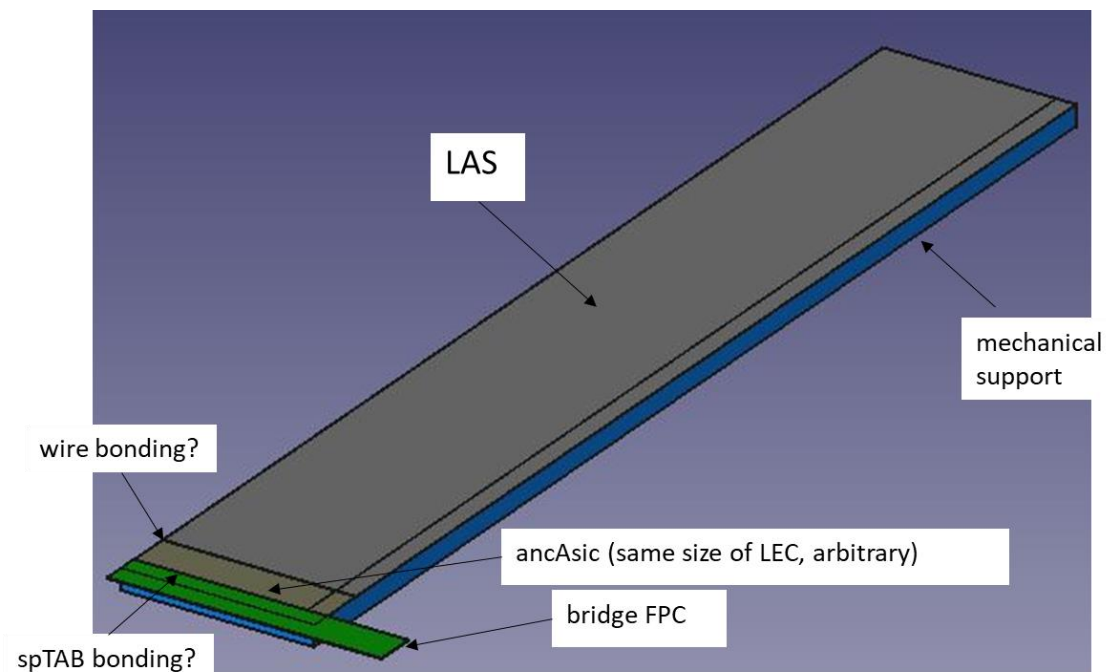


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Module (a.k.a. HIC)

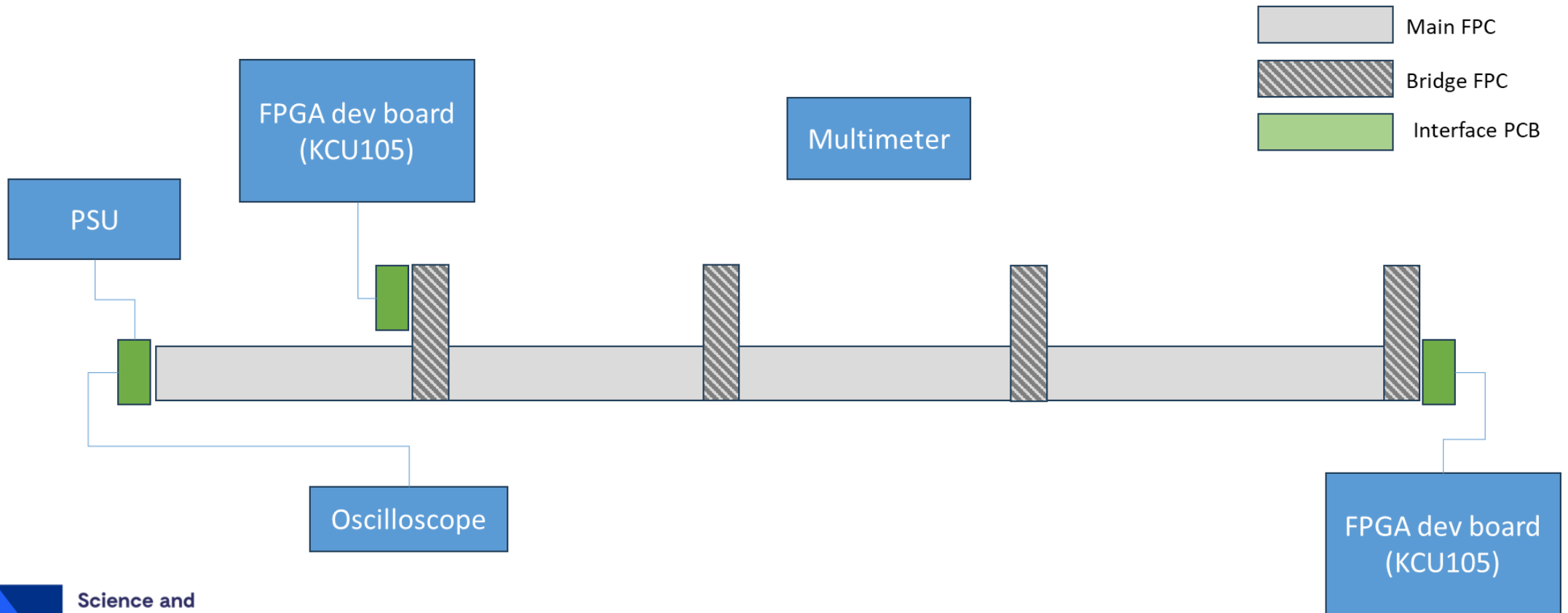
Module based approach to OB stave



1st low TRL prototype

Test set-up

Sketch of test set-up



Conclusion

- The definition stage of a Low TRL prototype (OB L4 stave) was based on a snapshot of the project from ~Feb.2024;
- Design stage approaching completion, to be reviewed next week;
- Next: procurement and testing (w Oxford and LANL);



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Thank you

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