Front-end electronics (WP2) report

Wei Li (Rice University)

ePIC TOF DSC weekly meeting
May 15, 2024

Electron-Ion Collider

https://indico.bnl.gov/event/23237/ for details

BROOKHAVEN NATIONAL LABORATORY | Jefferson Lab | U.S. DEPARTMENT OF ENERGY | Office of Science

Pre-prototype readout board (ppRDO)

- Mike, Tonko (Rice), William (JLab), Zhenyu (LBNL), Prithwish (BNL)

6 boards: 1 w/ Tonko, 1 w/ William, 4 w/ Mike at Rice

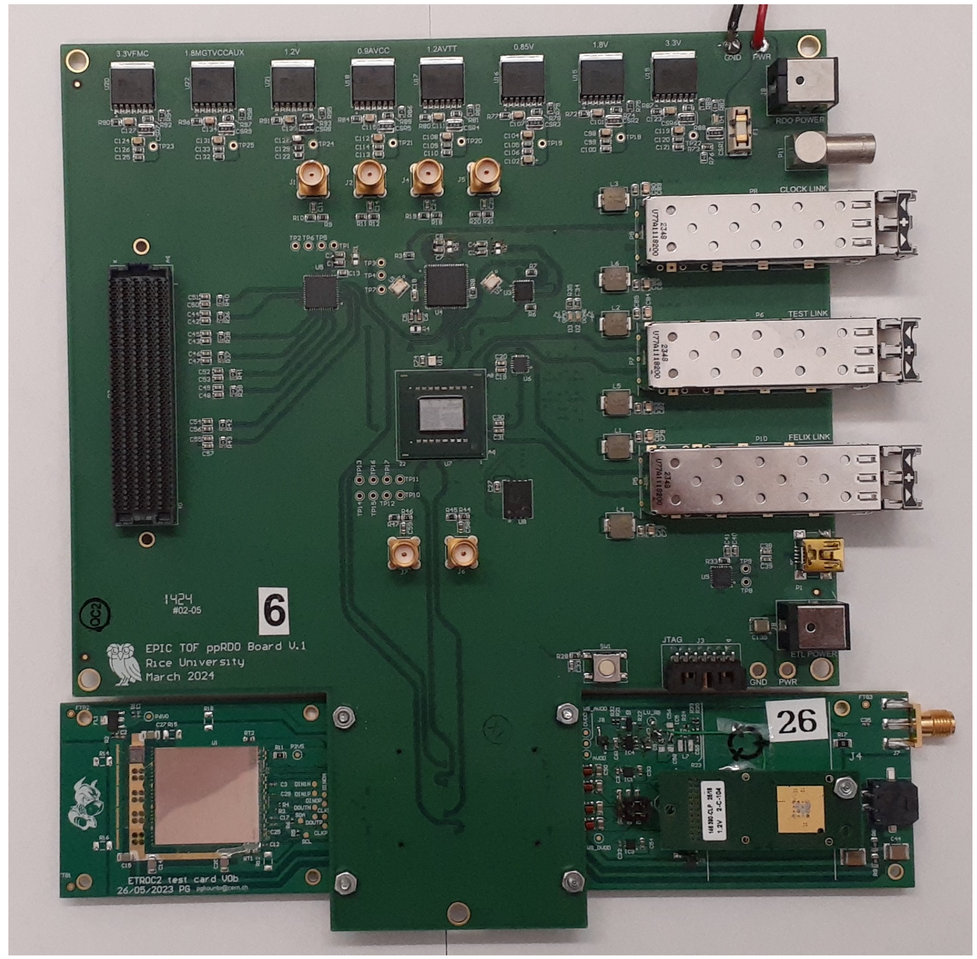
- Basic functionalities tested: minor issues addressed and all boards are good now.
- Connection with ETROC2 module board (v0) established

Xilinx project setup for the firmware development

- A Linux setup at Rice ready for remote access and development

Next steps:

- FPGA firmware development
- Readout test development with ETROC2
- Detailed power measurements



ppRDO + ETROC2 Module Board (v0)

Power board design

- Tim Camarda (BNL)

Power/voltage requirements:

- EICROC: 1W @ 1.2V
- FPGA: 1.8, 1.2, 0.9, 0.85 V
- SFP+: 3.3V

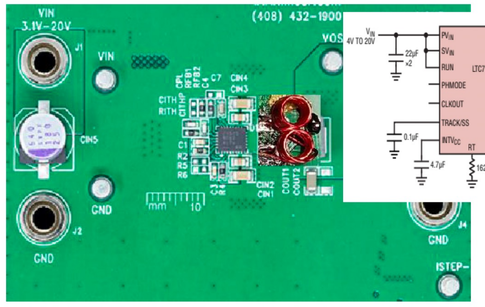
– 5 different voltages needed from PB

Several options of DC-DC convertors being evaluated:

- Preliminary test results encouraging – all showing good efficiency (>=80%)

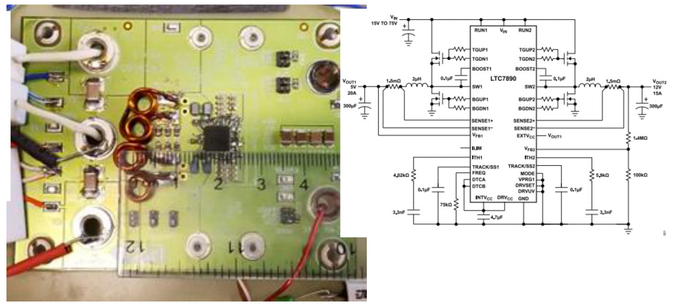
Next steps:

- Irradiation tests at UCDavis
- Prepare for the 1st PB design



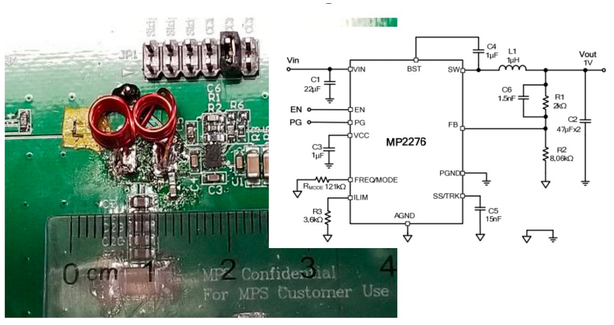
LTC 7151 DC|DC regulator evaluation board

- Package size: 5mm x 4mm (QFN)
- Power FET (Internal)
- T °C (need to record)
- Vin: 4 to 20V, Vout 0.5 to 5.5V
- F_{Sw} => 0.4 – 3MHz
- Power Output => 14.5W => 1.2V @ 12A (80%)
- Switching phase: 180° out (reduce EMI)
- P_{EFF} > 80% ($12V_{IN}$, 12A)
- Noise/ Ripple < 0.5% @ 12A
- Regulation => 99%
- Will require 2x for ASIC power boards
- Tested w/ 300nH solenoid inductor 2MHz



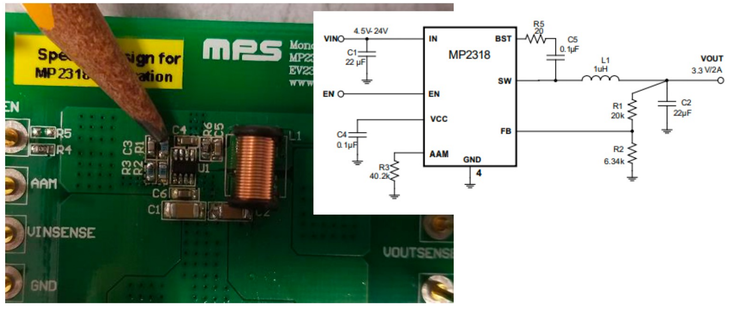
LTC 7890 (GaN Controller) evaluation board (replacement candidate for CERN bPOL48V controller for lesser harsh rad environments)

- Package size: 6mm x 6mm (QFN)
- Power FET (external GaN)
- T_{CHIP}:54°C , T_{IND} 56°C, T_{PCB} 46°C (open air, no heat sink)
- Vin 4 to 100V, Vout 0.8 to 60V
- F_{Sw} => 0.1 – 3MHz
- Power Output => 30W => CH1 1.2V @ 12A, CH2 1.2V @12A (80%)
- Switching phase: 180° out (reduce EMI)
- P_{EFF} ~ 80% ($12V_{IN}$, CH1 12A, CH2 12A)
- Noise/ Ripple < 0.5% @ 12A/ channel
- Regulation => 99%
- Will require 1x for ASIC power boards
- Tested w/ 300nH solenoid ind. 2MHz



MP2276 DC|DC regulator evaluation board

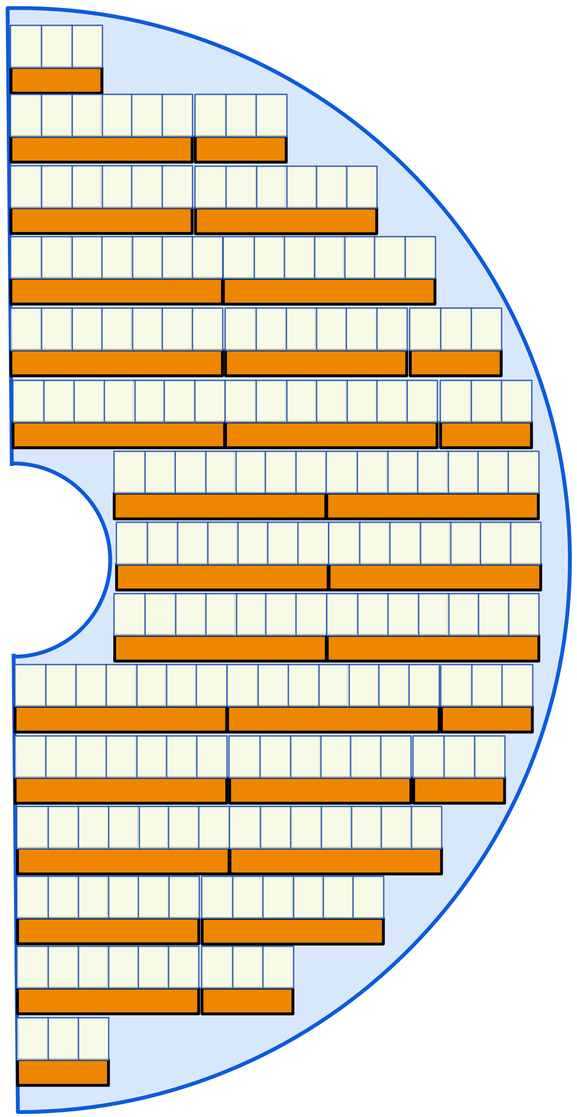
- Package size: 2mm x 3mm (QFN)
- Power FET (Internal)
- T_{2276} 50°C, T_{IND} 40°C
- Vin: 2.7 to 16V, Vout 0.8 to 6V
- F_{Sw} => fixed 2MHz
- Power Output => 8W => 1.2V @ 6.5A (80%)
- Switching phase: (fixed)
- P_{EFF} > 80% ($12V_{IN}$, 6A out)
- Noise/ Ripple < 0.5% @ 6.5A
- Regulation => 99%
- Tested w/ 300nH solenoid inductor 2MHz

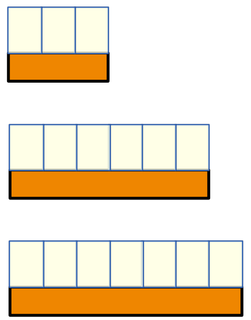


MP2318 DC|DC regulator evaluation board (possible to use on ASIC board)

- Package size: 3mm x 3mm (TSOT23-8)
- Power FET (Internal)
- T_{IND} = 30°C, T_{CHIP} = 34°C
- Vin: 4.5 to 24V, Vout 0.8 to ~ Vin
- F_{Sw} => fixed 2MHz
- Power Output => 2W => 1.2V @ 1.6A (80%)
- Switching phase: (fixed)
- P_{EFF} ~ 75% ($12V_{IN}$, 1.2A out)
- Noise/ Ripple < 0.2% @ 1.2A
- Regulation => 99%
- Tested w/ 760nH solenoid inductor 2MHz

FTOF layout update





RB3 (3-module)

RB6 (6-module)

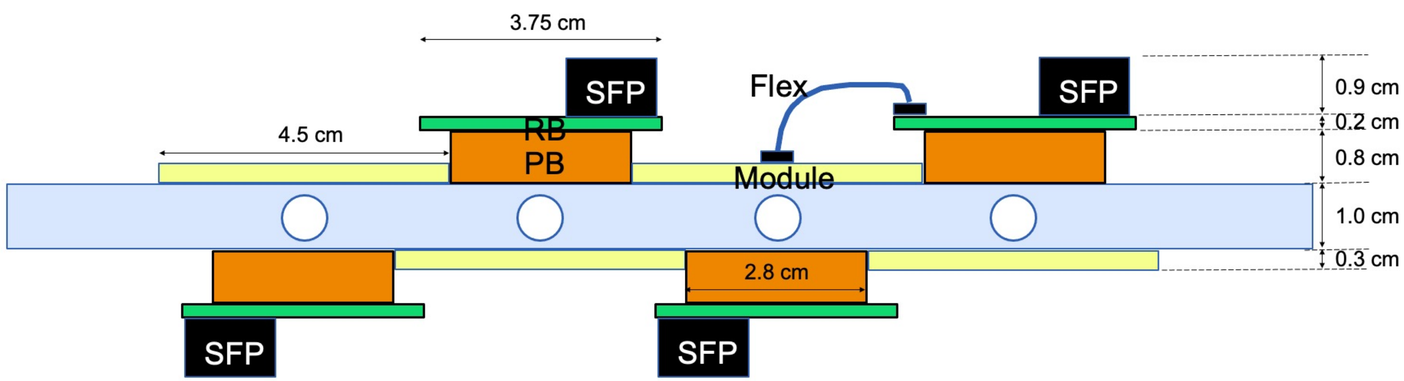
RB7 (7-module)

4 EICROCs per module

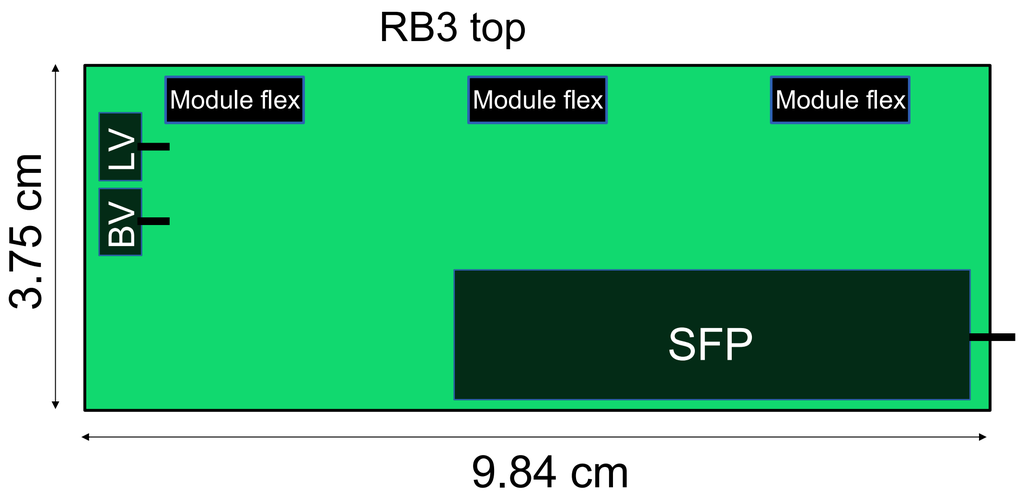
Total number of modules: **736**

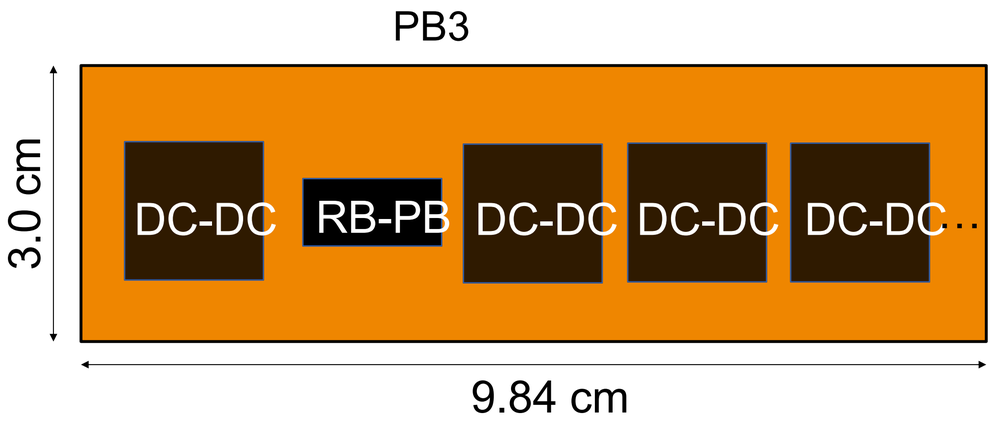
Total number of service hybrids: **128**

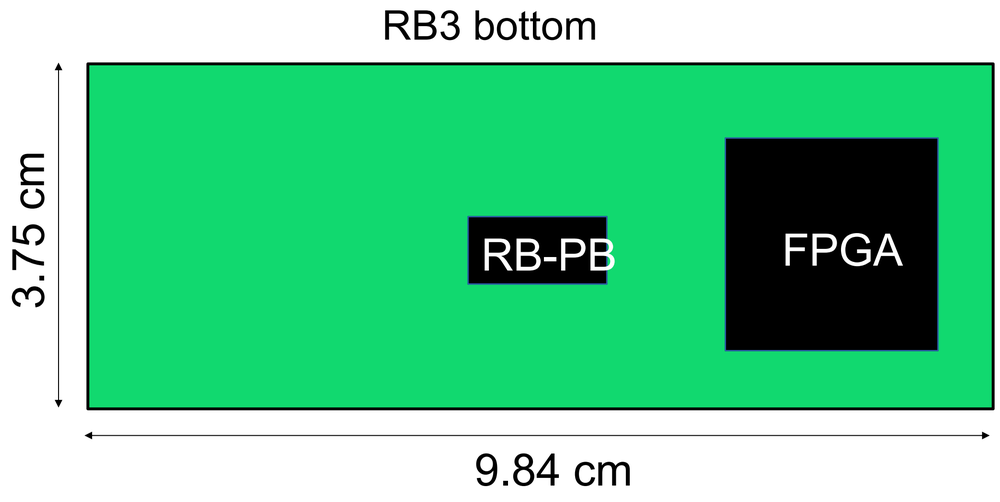
Envelope in z is now **8cm**



Readout and power board design

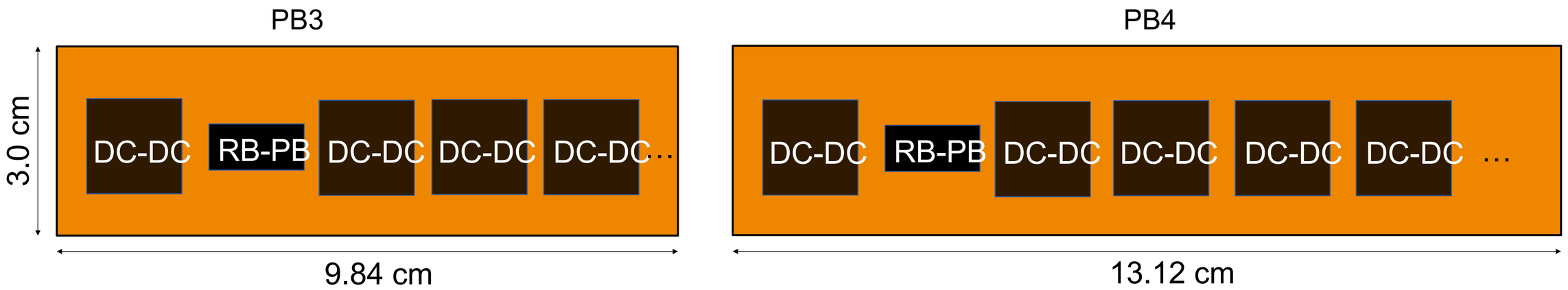






Backups

Power board design



Number of DC-DC converters to be decided, depending on the choice of converters