Low Q^2 DAQ update
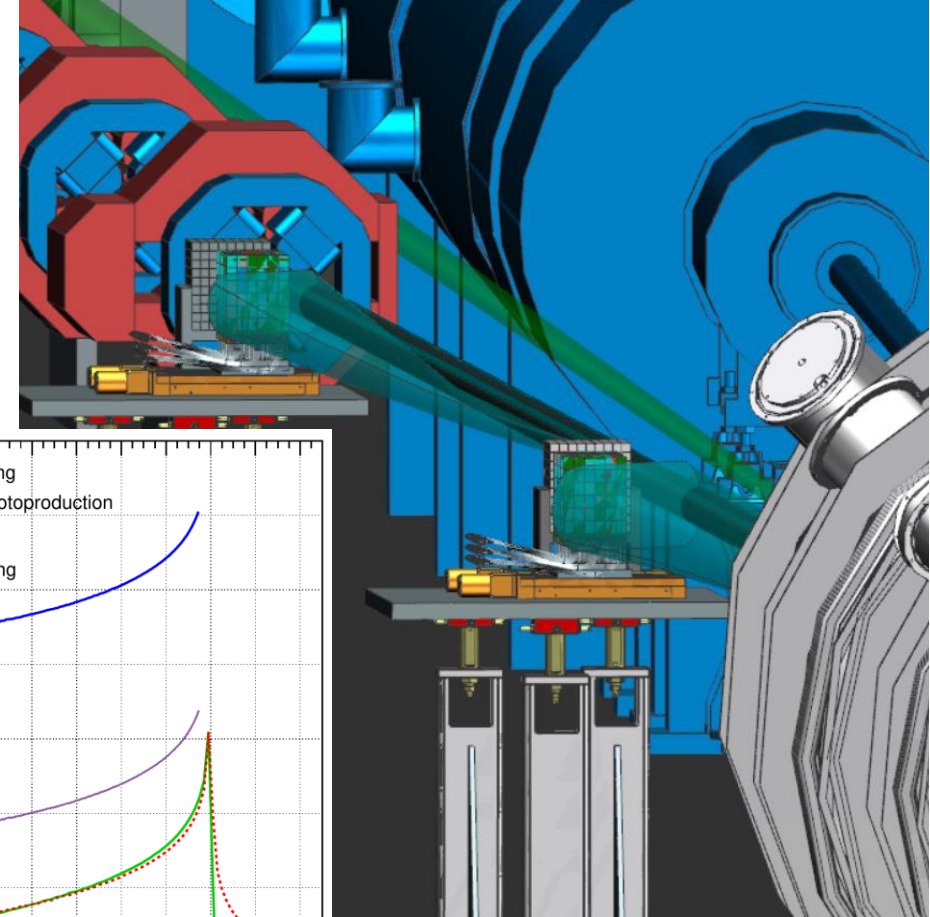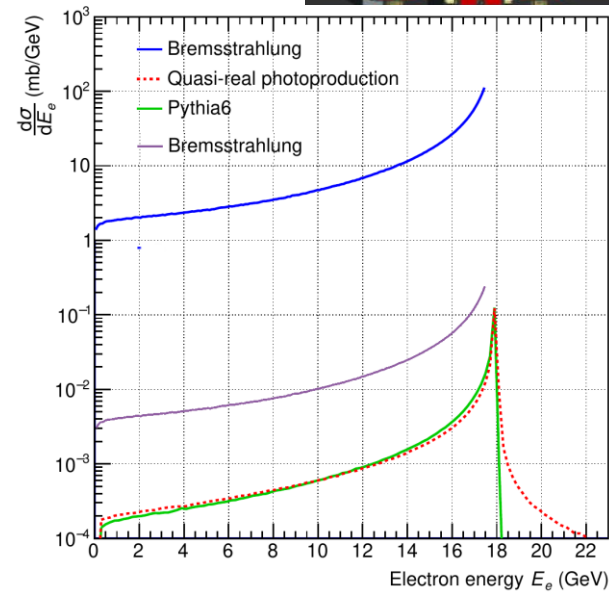
Simon Gardner

ePIC DAQ meeting
16th May 2024

Requirements

- Extend Q^2 acceptance
- Allow quasi real ($Q^2 \sim 0$) physics
- Very close to beamline.

  - 2 Taggers covering different electron energies

  - Pixel based trackers with rate capability and pixel resolution to identify > 10 tracks per beam bunch (Bremsstrahlung BG)

Technology

- ## Tracker

  - **Timepix4 Hybrid (ASIC+Si) + SPIDR4 readout.**
    - Pixels: 55x55 um. 448 x 512 pixels. Area = 6.94 cm^2
    - Individual thresholds, data driven
    - Timing: < 2 ns.
    - Rates: < 5.5 MHz per 2x256 column
  - **Layout**
    - 1 board: 6x2 Timepix4 → SPIDR4 readout.
    - 1 layer: 3 boards
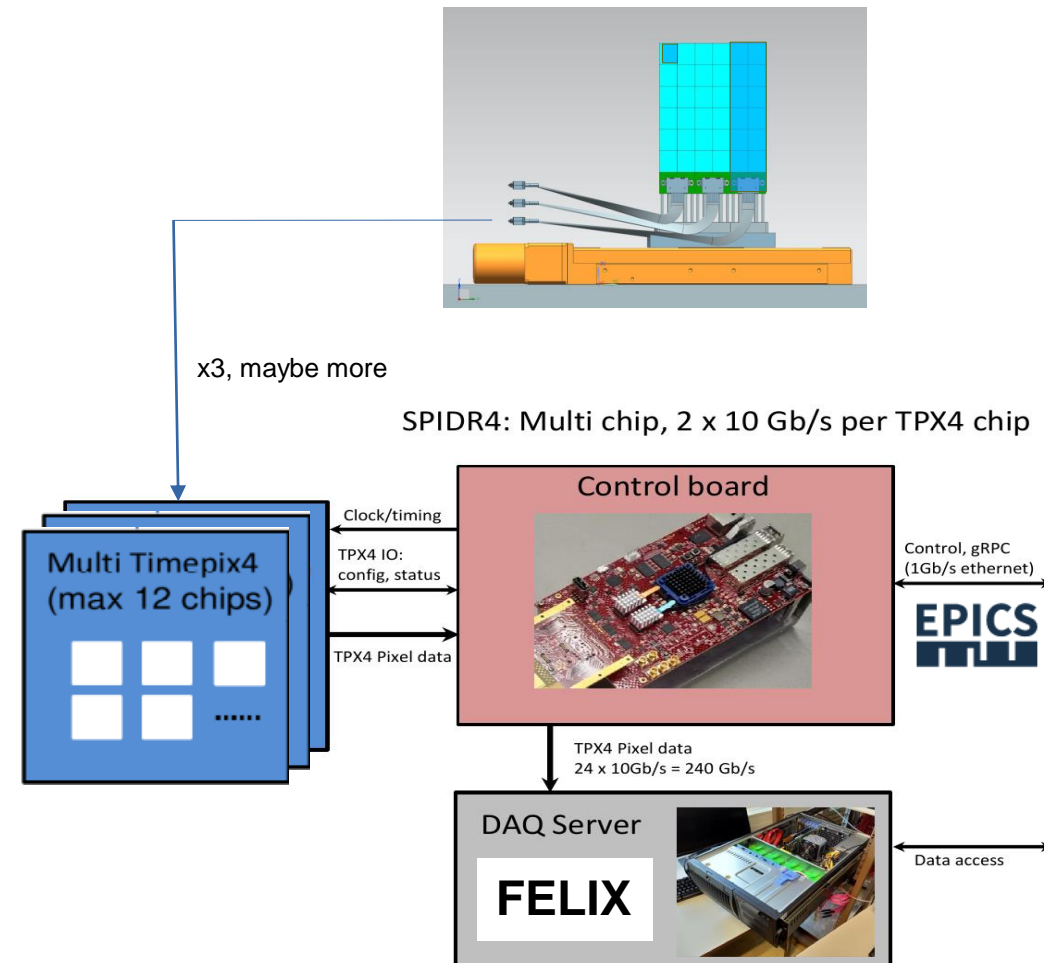   - 1 tagger: 4 layers → total of 12 boards, 144 x Timepix4
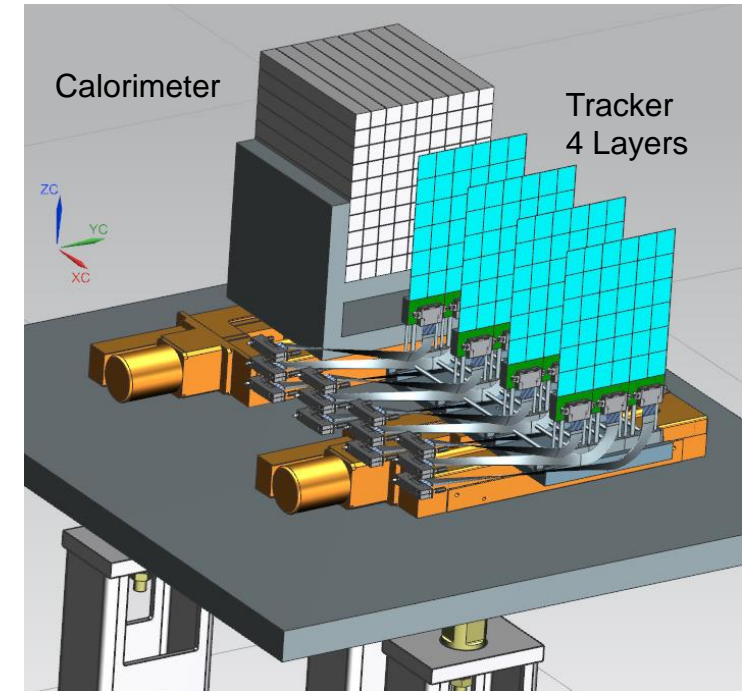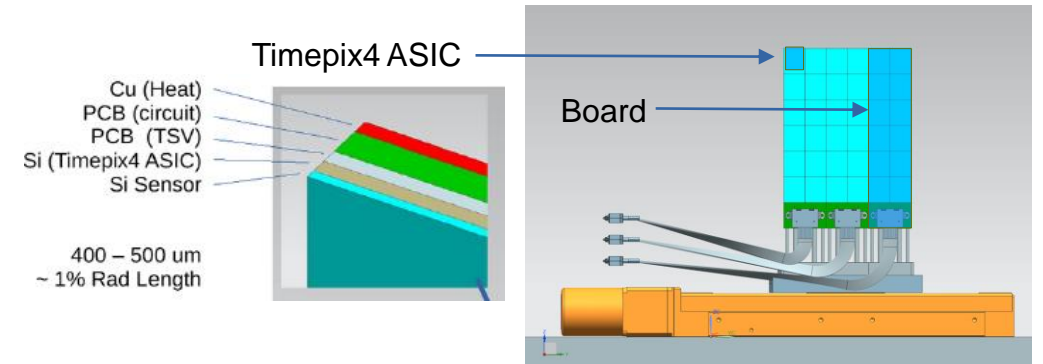
Readout and DAQ

- ## Tracker
  - Timepix4 readout SPIDR4, NIKHEF
  - Digitization on ASIC. Individual thresholds. Very low noise.
  - Control board, handle up to 12 Timepix4
  - Data → FELIX boards / Buffering
  - Buffered data filtered **on coincidence** with central detector

- ## Calorimeter
  - Fibres → SiPM → standard DAQ channels
  - 2 x 900 channels per calorimeter = 900

x3, maybe more

SPIDR4: Multi chip, 2 x 10 Gb/s per TPX4 chip

Multi Timepix4 (max 12 chips)

Clock/timing

TPX4 IO: config, status

TPX4 Pixel data

Control board

Control, gRPC (1Gb/s ethernet)

EPICS

TPX4 Pixel data
24 x 10Gb/s = 240 Gb/s

DAQ Server

FELIX

Data access

Rate - PREVIOUS

- High Brem BG, Non uniform distribution.

- Maximum rates
- Pixel (P1)   70 kHz
- 2 column (C1)   8 MHz
- Tpix4 (T1)   600 MHz   38 Gb/s
- Board (B1)   1500 MHz   96 Gb/s
- Layer (L1)   2500 MHz   160 Gb/s

- Total integrated rates
- Tagger 1   2 GHz   130 Gb/s
- Tagger 2   7 GHz   480 Gb/s
- **Total**   **9 GHz**   **600 Gb/s**

- Data buffered & filtered: need a hadron in main detector
- Trigger rate: 500 kHz: 99.4% rejection (brem only)
- Data rate (signal):   4 Gb/s
- **Data rate** (incl BG and rand sample)   **<20 Gb/s** To tape

Low Q^2 tagger rates kHz / pixel. (18x275 GeV @ 10^{34} cm^{-2} s^{-1})

Q.R.
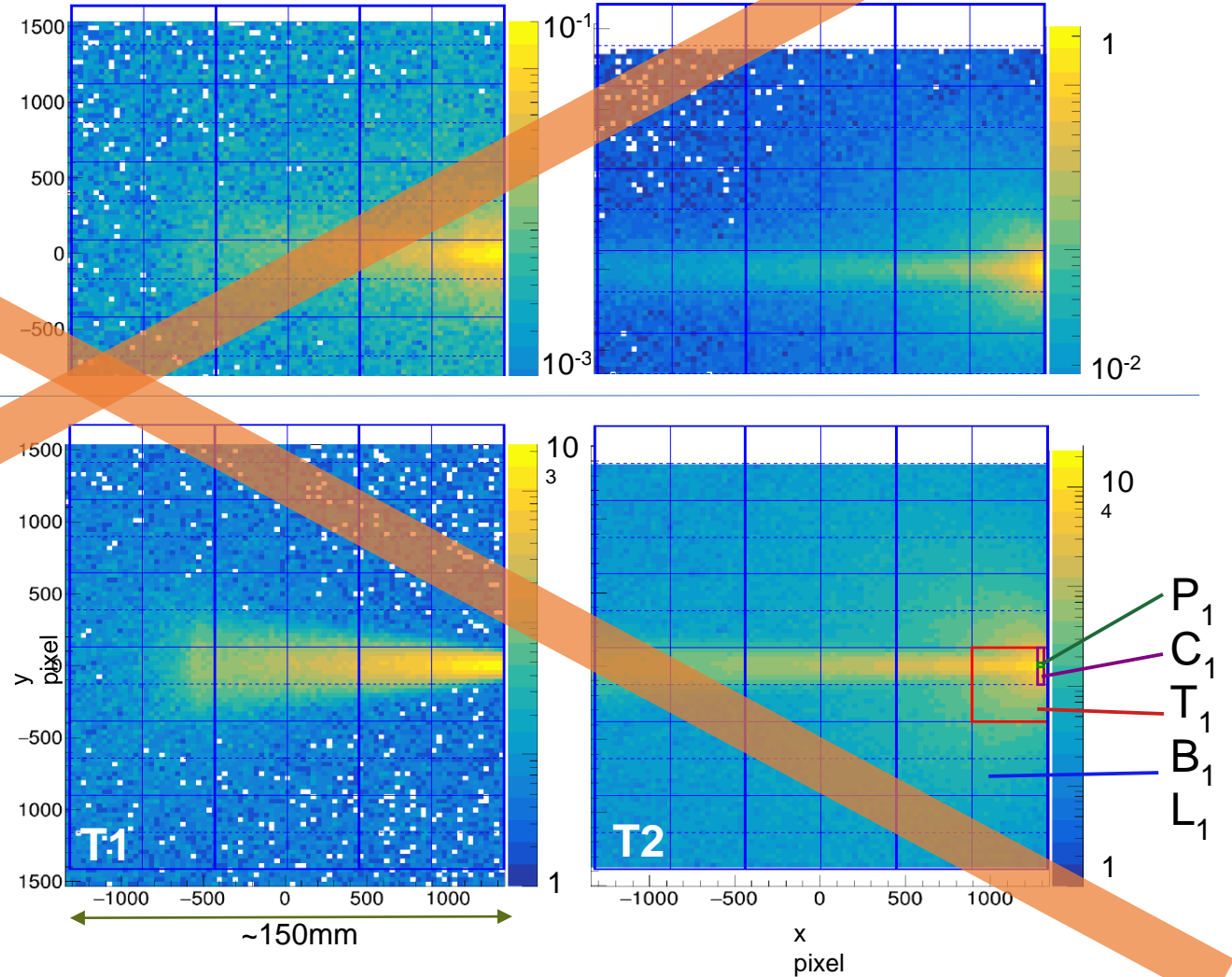
Brem.

Rate – Plots need updating

- Previous raw rates were a factor of 17 too high, number of Bremstrahlung interactions per bunch applied twice.
- Maximum per pixel now ~4kHz

Status and plans

- 2 x SPIDR4 kits in Glasgow   Jan 2024

- Timepix4 ASICS bonded to carrier boards and ready to start tests

- Once confident will visit Nikhef and discuss what we need from the SPIDR4

- Looking into data reduction with GNNs prior to main DAQ via cluster and track based rejection.

- Working on more detailed simulation of sensor response and digitization.
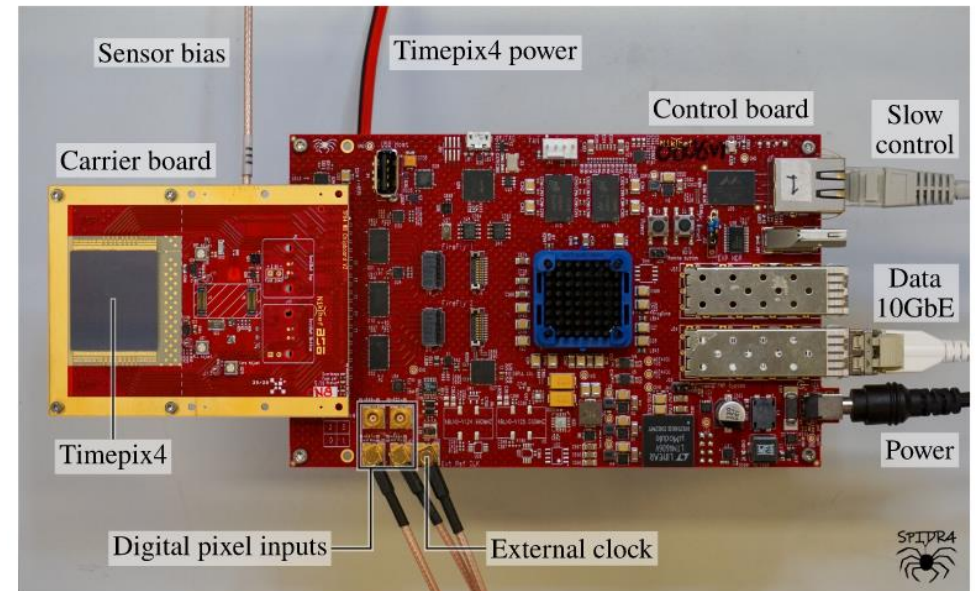
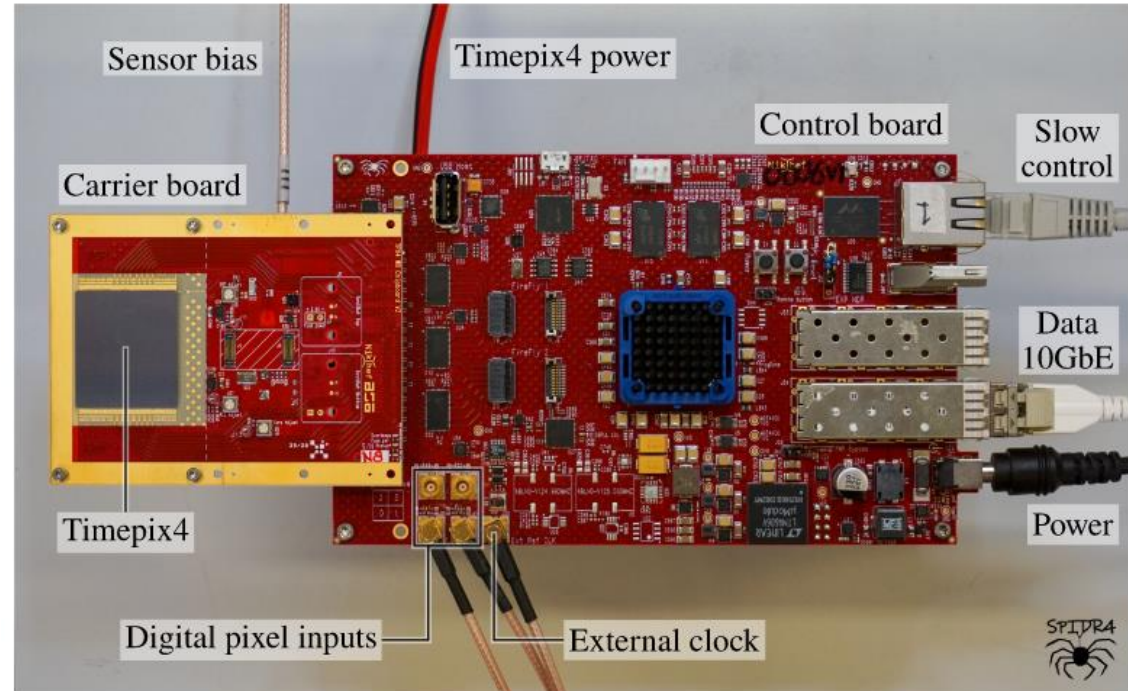• Timepix4 + SPIDR4 Engineering test setup.

Timepix3 vs Timepix4

Timepix4: A 4-side tillable large single threshold particle detector chip with improved energy and time resolution and with high-rate imaging

		Timepix3 (2013)	Timepix4 (2019)	
Technology		130nm – 8 metal	65nm – 10 metal	
Pixel Size		55 x 55 µm	55 x 55 µm	
Pixel arrangement		3-side buttable 256 x 256	4-side buttable 512 x 448	3.5x
Sensitive area		1.98 cm²	6.94 cm²	
Readout Modes	Data driven (Tracking)	Mode	TOT and TOA		
		Event Packet	48-bit	64-bit	33%
		Max rate	0.43x10⁶ hits/mm²/s	3.58x10⁶ hits/mm²/s	
		Max Pix rate	1.3 KHz/pixel	10.8 KHz/pixel	8x
	Frame based (Imaging)	Mode	PC (10-bit) and iTOT (14-bit)	CRW: PC (8 or 16-bit)	10x
		Frame	Zero-suppressed (with pixel addr)	Full Frame (without pixel addr)	5x
		Max count rate	~0.82 x 10⁹ hits/mm²/s	~5 x 10⁹ hits/mm²/s	8x
TOT energy resolution		< 2KeV	< 1Kev	
Time resolution		1.56ns	~200ps	
Readout bandwidth		≤5.12Gb (8x SLVS@640 Mbps)	≤163.84 Gbps (16x @10.24 Gbps)	

Xavier.llopart@cern.ch Medipix Symposium, Sept 2019

Sensor bias — Timepix4 power — Control board — Slow control — Carrier board — Data 10GbE — Timepix4 — Digital pixel inputs — External clock — Power

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