

## Lab Roadmap: BNL

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### *Abstract*

BNL is actively involved in the ATLAS detector upgrade, both in Phase-I and HL-LHC. For Phase-I, BNL is a main contributor to the three subsystems: Liquid Argon Calorimeter, Muon New Small Wheel (NSW) and the TDAQ System. BNL is leading the architecture design of Phase-I LAr trigger electronics upgrade. The 320-ch LAr Trigger Digitizer Board (LTDB) demonstrator has been installed on detector in July 2014, data taken from it shows satisfactory performance. Test on the 320-ch LTDB pre-prototype and 64-ch prototype, design of the 320-ch prototype are ongoing. The low power, mixed-signal front-end ASIC VMM chip is designed for Muon NSW, which is suitable for both of MicroMegas and sTGC (Thin Gap Chamber) detectors. The ART Data Driver Card designed by BNL is also part of NSW Phase-I upgrade, which is used to transfer the Address in Real Time signals. A single ATCA module gFEX with high-density optical transmission and parallel DSP in FPGA is used to process the whole ATLAS calorimeter information for finding large-R jet. BNL is also involved in FELIX project, which is a new approach to interface on-detector front-end and trigger electronics. The role of BNL is to develop the GBT link firmware, and design the prototype hardware, which is a 16 lanes Gen 3 PCIe card with 48 high-speed optical links. For LAr upgrade of HL-LHC, BNL will be involved in the 65nm based FESOC design. This presentation will cover the status of these trigger, DAQ and detector readout related development.