OAK RIDGE National Laboratory

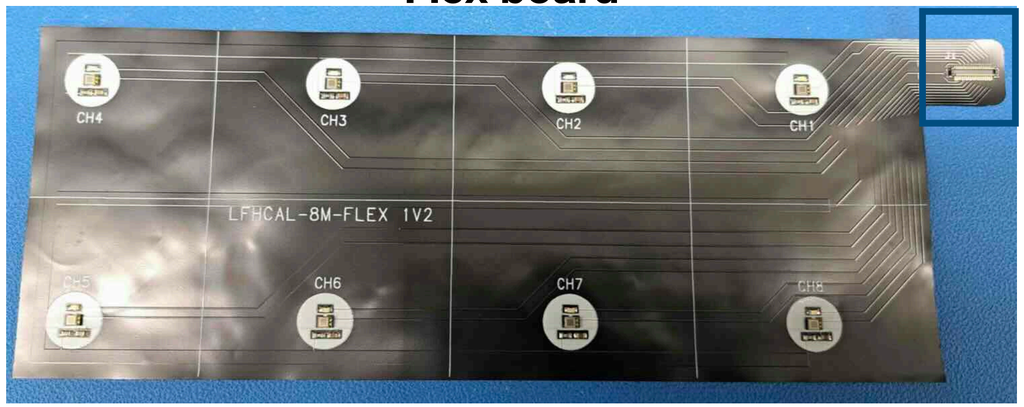
# LFHCal electronics concept

Norbert Novitzky, Miklos Czeller,
Gabor Nagy
(ORNL)
Shihai Jia, Ian Bearden
(Københavns Universitet)

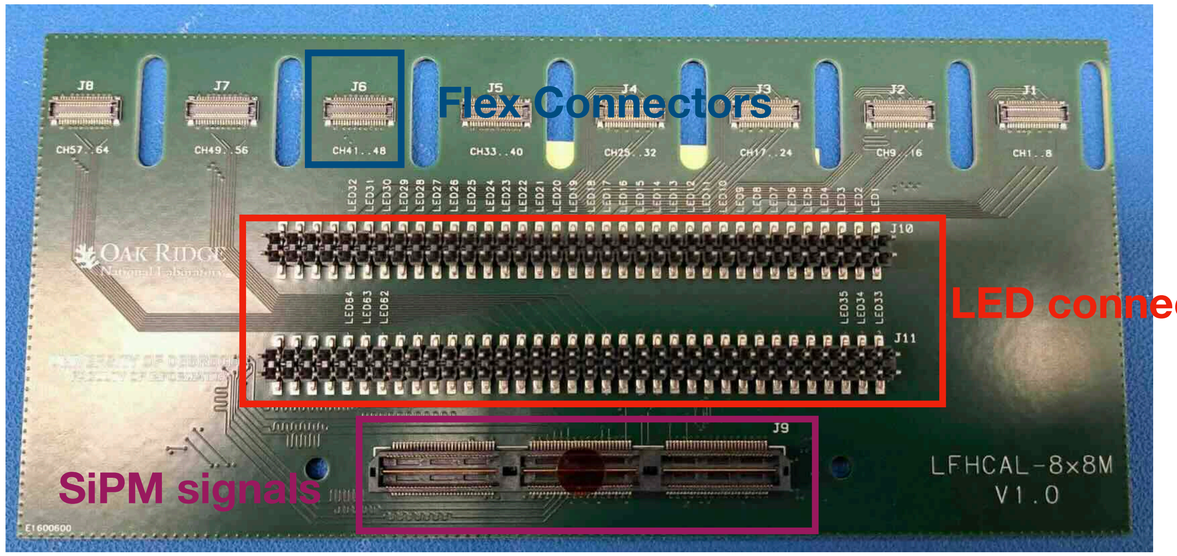
ORNL is managed by UT-Battelle LLC for the US Department of Energy

# First prototype

## Flex board



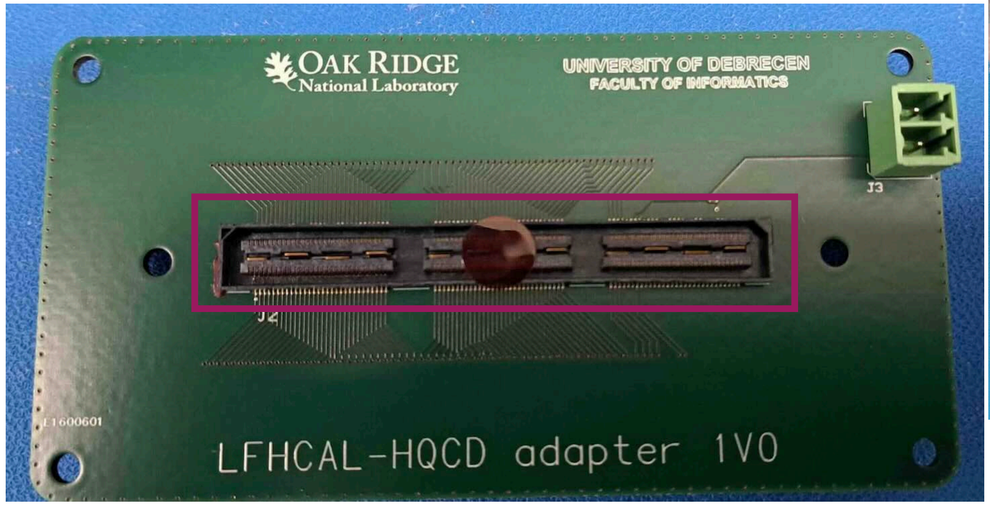

## Short Long board (prototype)




**Just electronics in this:**

- Flex board - 8 SiPM's and 8 LED's. Some noise cancellation capacitors are added
  - Each will occupy one layer in LFHCal
- Short-long board is the first prototype for the longer board:
  - SiPM signals are connected with a Samtec cable
  - LED connections are on pins:
    - We plan to make a daughter board and driver prototype
- Adapter board:
  - Connects to the HGCROC/CAEN boards on the back

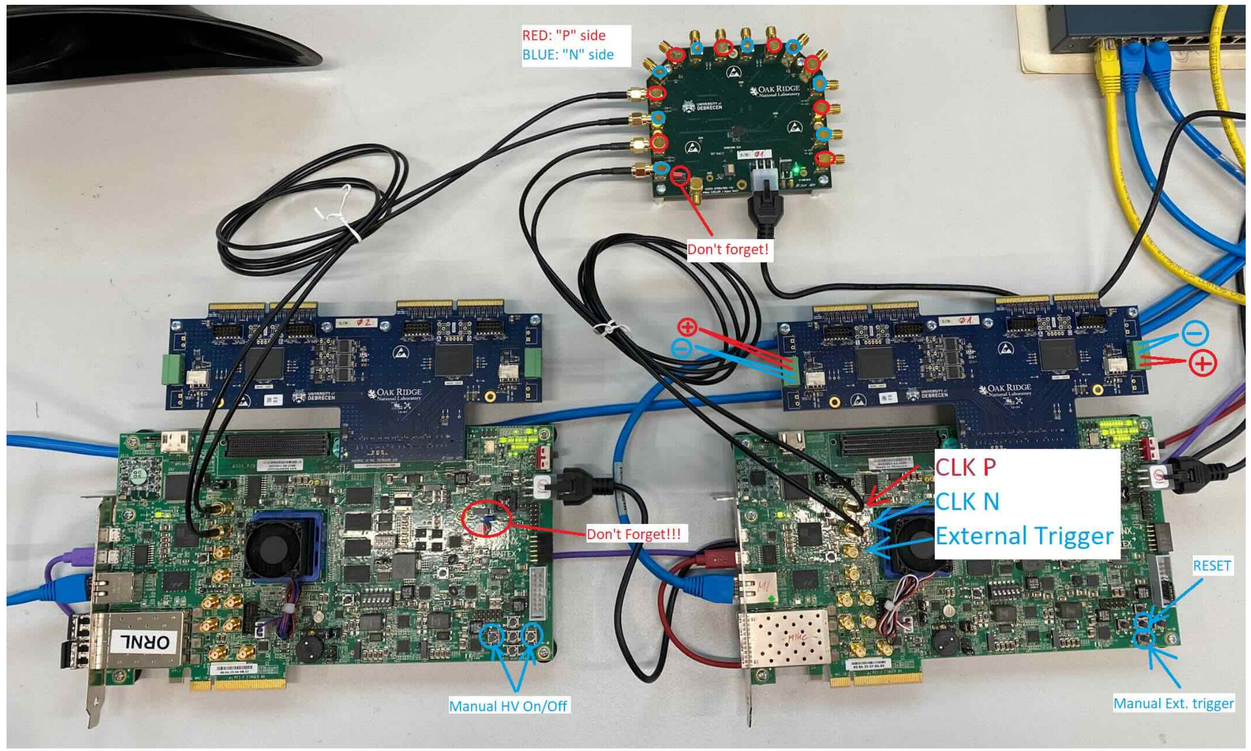
## Adapter board

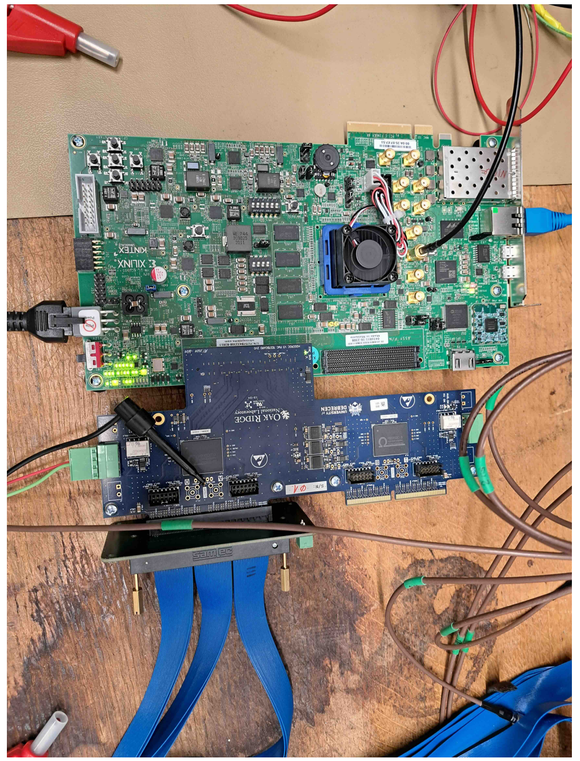





OAK RIDGE National Laboratory

# All setup with the HGCROC prototype boards

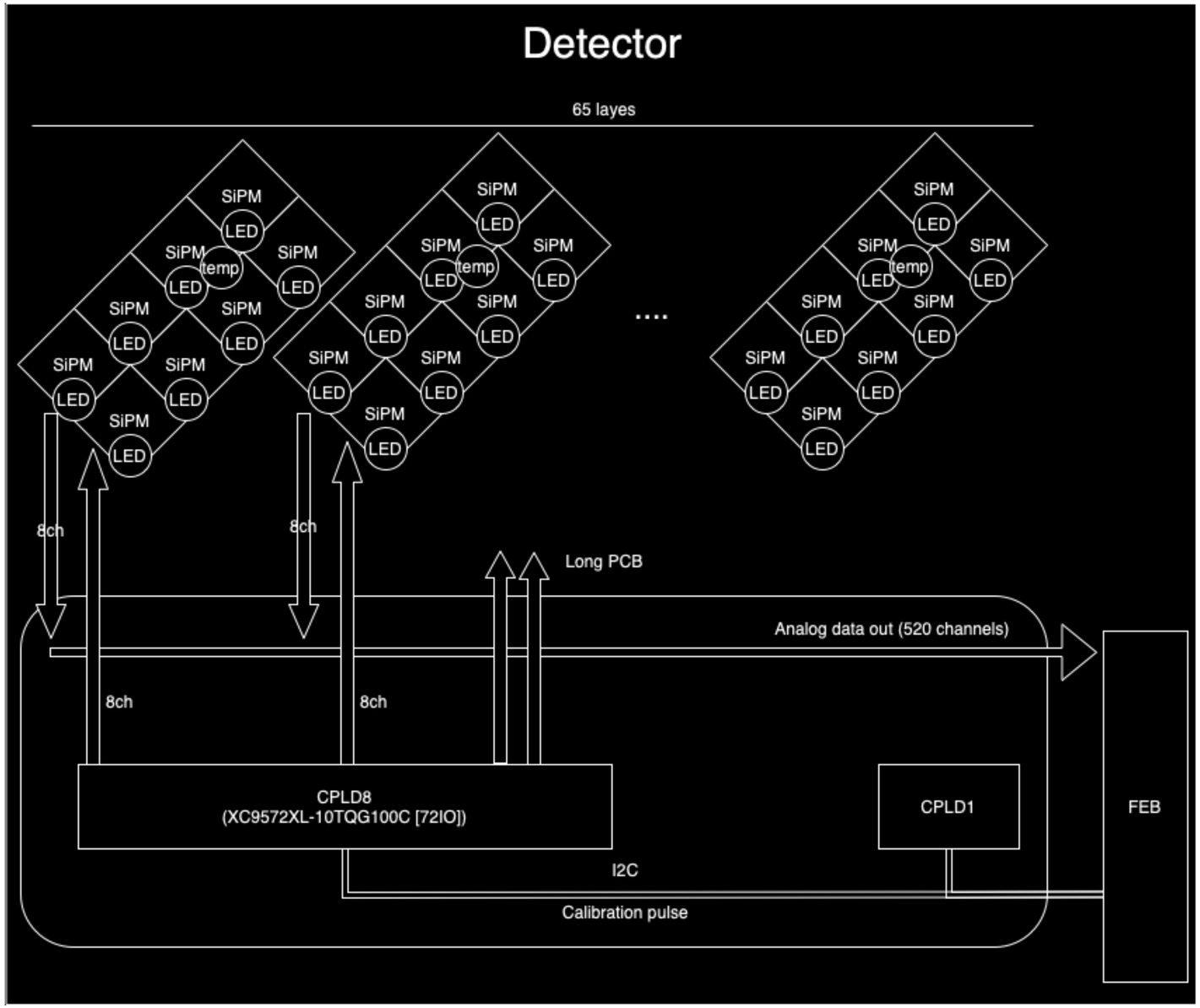


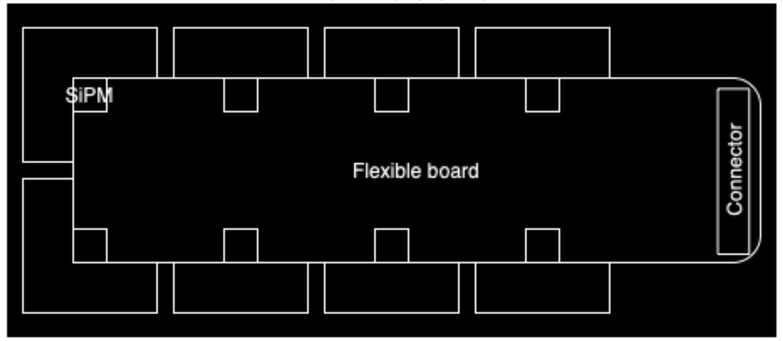

**Readout prototype:**

- HGCROC chips are connected to a Kintex Ultrascale 040 (KCU105)
  - FMC connection provides also power and the data lines
  - Clock is synchronized with an external clock board
- Front adapter is then connected to the HGCROC input and then all the way to the SiPM's
  - Shown in the pictures

# Towards final prototype



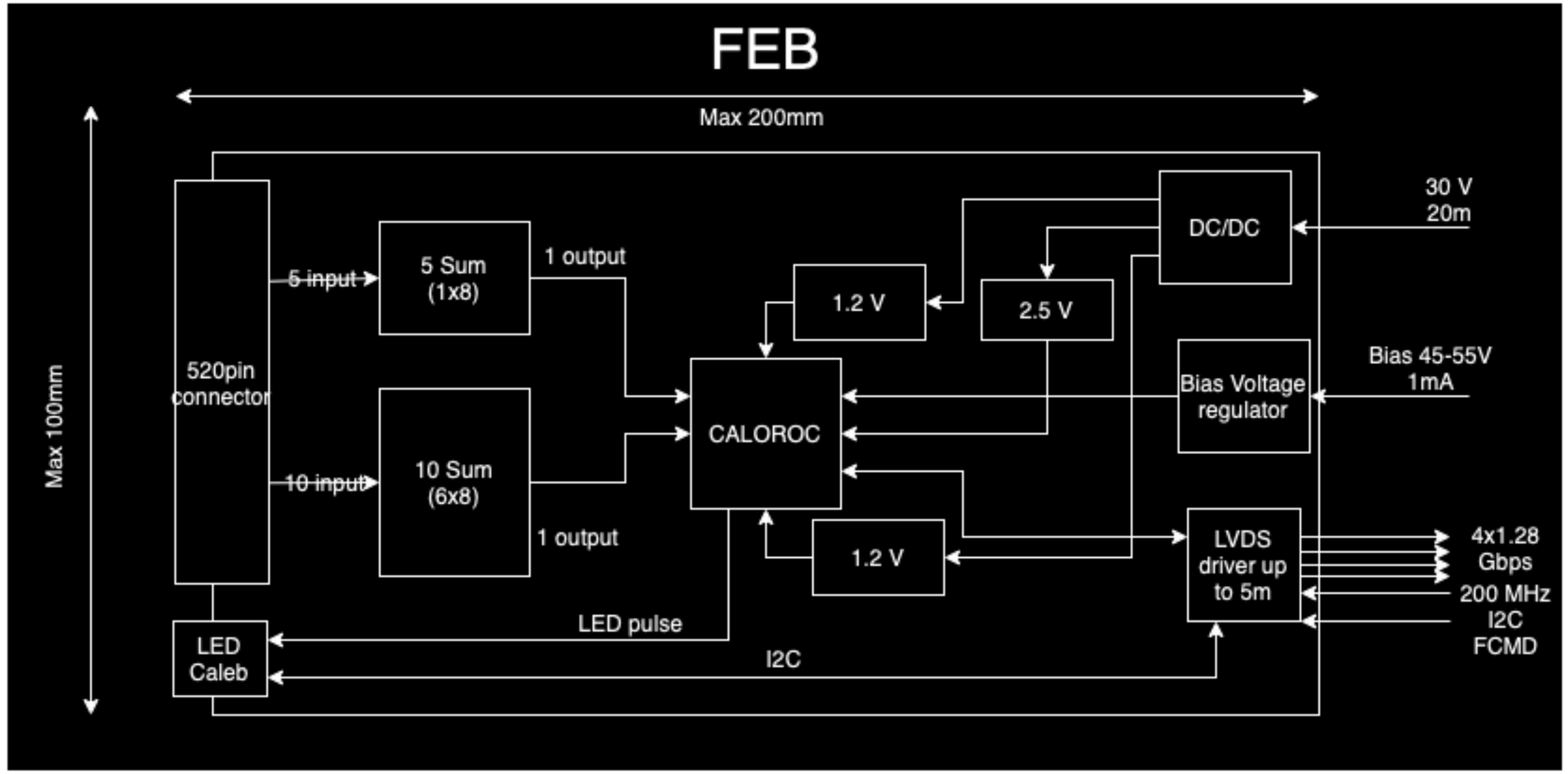

**Flex board**




**Final Long board (about 1.4 m):**

- Each flex board is the same as the ‘prototype’:
  - 8 SiPM for signal
  - 8 LED for the calibration
  - Additional noise cancelling components (passive)
- Long PCB board:
  - Transfer 520 signal lines towards the back of the detector (FEB)
  - Control the LED signals for calibration:
    - 8xRadHard CLPD with 64/72 IO’s to be able to flash each LED separately
    - Calibration pulse can be taken from the HGCROC/CALOROC
    - I2C will be used to setup the CLPD to which LED to drive

# FEB with the CALOROC




**FEB is placed on the back of the 8M module:**

- Has to fit in the 200mm, 100mm space
- 520 pin connector for all the input from the SiPM
- Power tree:
  - 30 V (need detailed testing) as input
  - DC/DC steps down to 2.7-2.8 V
  - 2xLDO @1.2V analog and digital
  - 1xLDO @2.5V analog
- CALOROC:
  - Setup is on I2C
  - 4x Data lines at 1.28 Gbps output
  - Input 200 MHz clock
  - Fast command
  - Output for the LED driver
    - Currently under testing

**This is so far a preliminary design and we are currently testing each component for making the first version next year:**

- Summing circuits, passive or active
- LED calibration circuit
- DC/DC, LDO testing - found already RadHard components which would be sufficient
- LVDS drivers

# RDO ideas, power, etc

**We plan this will be a future development:**

- Design a versatile RDO board to with flexibility to use different FPGA for different detectors
- Easy exchange of FPGA on the board within the same packaging
- Compact design

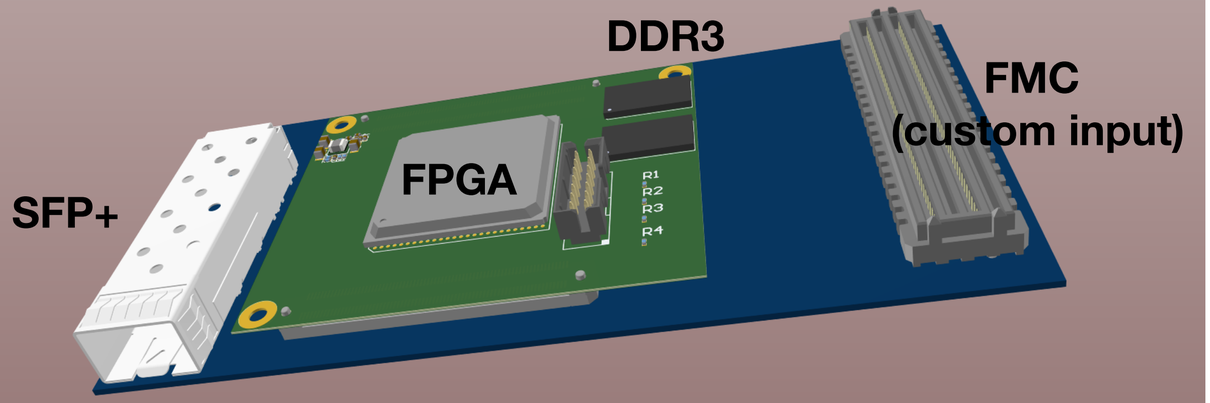
**FPGA choices, power and # ASIC**

| | Reduce the common Memories 126 >> 64 and 6BRAM/ASIC | | | | |
|---|---|---|---|---|---|
| | FPGA | Nr. Of BRAM | SUM (W)75% | Max. Nr. Of ASIC | USD |
| **Basic Artix Ultrascale+** | XCAU10P-2FFVB676E | 100 | 4.1 | 4 | 277 |
| | XCAU15P-2FFVB676E | 144 | 5.7 | 12 | 347 |
| | XCAU20P-2FFVB676E | 200 | 7.4 | 20 | 499 |
| | XCAU25P-2FFVB676E | 300 | 10.4 | 32 | 596 |
| | | | | | |
| **Kintex Ultrascale+ (more powerful)** | XCKU3P-2FFVB676E | 360 | ? | 48 | 2 198 |
| | XCKU5P-2FFVA676E | 480 | ? | 64 | 2 922 |
| | | | | | |
| Kintex Ultrascale (What we use now, reference only) | KCU 040 FPGA | 600 | 10 | 64 | - |

Baseline

Same footprint, we can use any of these FPGA on the board

**Preliminary design**




**All RDO's would look the same:**

- Choose the XCAU20P Artix Ultrascale+ as a baseline for now:
  - All of the above chips has the same footprint, they are interchangeable on the board - if one needs more ASIC/RDO ratio or more computing power
  - Daughter card
- Should be applicable on other detectors also
  - Front FMC connector can be changed as needed

# Short-long term plans

**LFHCal testbeam in August:**

- All electronics is ready
- Tested the HGCROC in May testbeam (non-ePIC project):
  - Very successful, smooth data taking
  - Working on a more user-friendly readout software:
    - First GUI version this week

**Other summer activities:**

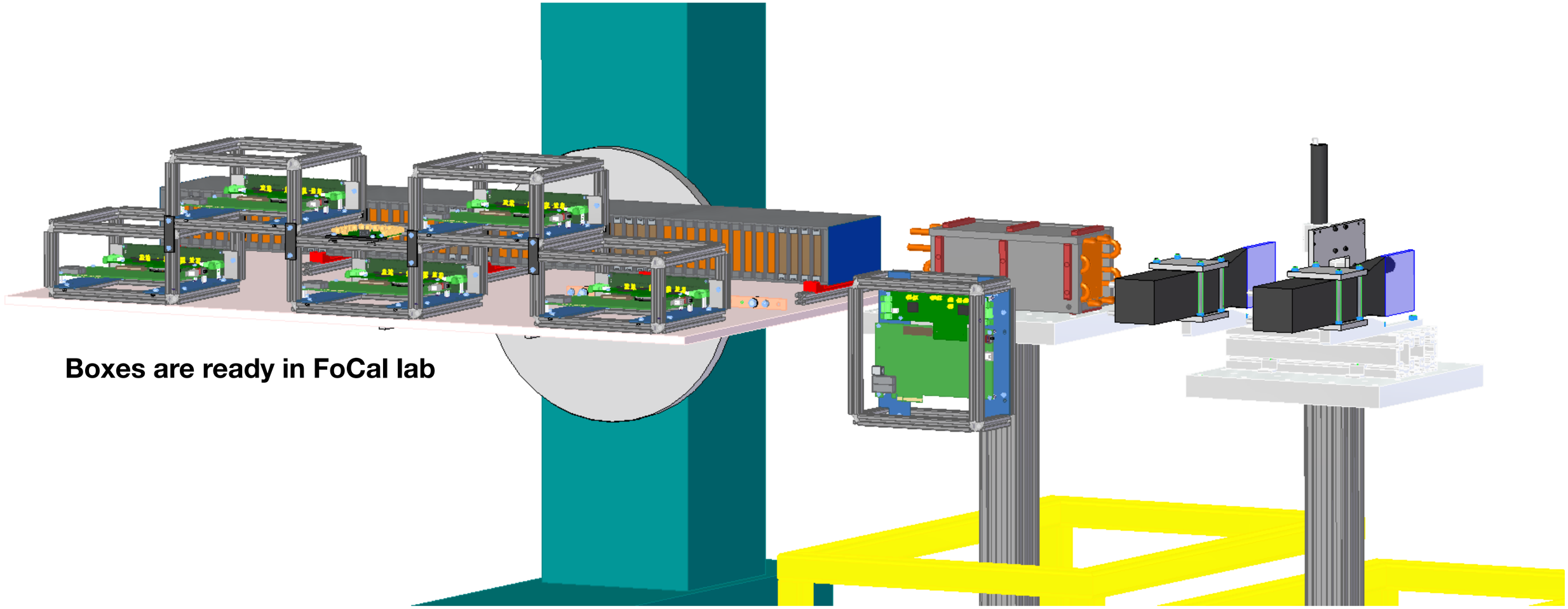
- Construct 2-3 different summing boards:
  - Passive would probably elongate the signal
  - Active summing could be tested also
- LED daughter card:
  - To be added to the short-long board as a prototype
  - Can be tested with external function generator and the HGCROC external signal

**Longer plans (let's say PED request next year):**

- Towards FEB 'test article':
  - CALOROC should be available in early 2025:
    - We will receive the RTL already in end of July if available
  - Test different DC/DC, LDO's.
  - Summing boards on the FEB, driving signals
- Towards the RDO 'test article':
  - Versatile and flexible board
  - Possible extension for non-calorimeter readouts

***PED request would be not only for LFHCal, but include Barrel HCal, BIC, backward HCal readouts***

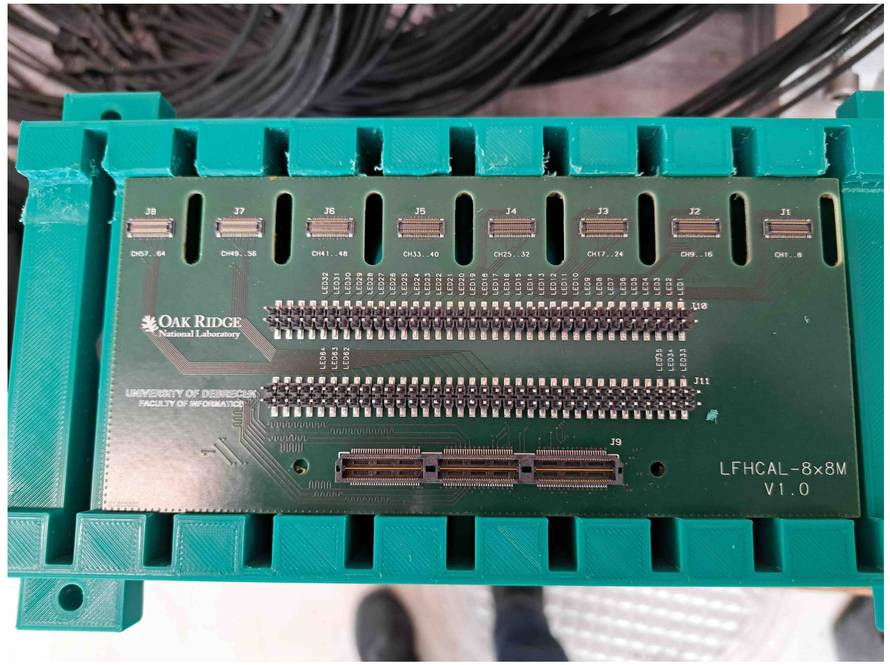
# LFHCal testbeam

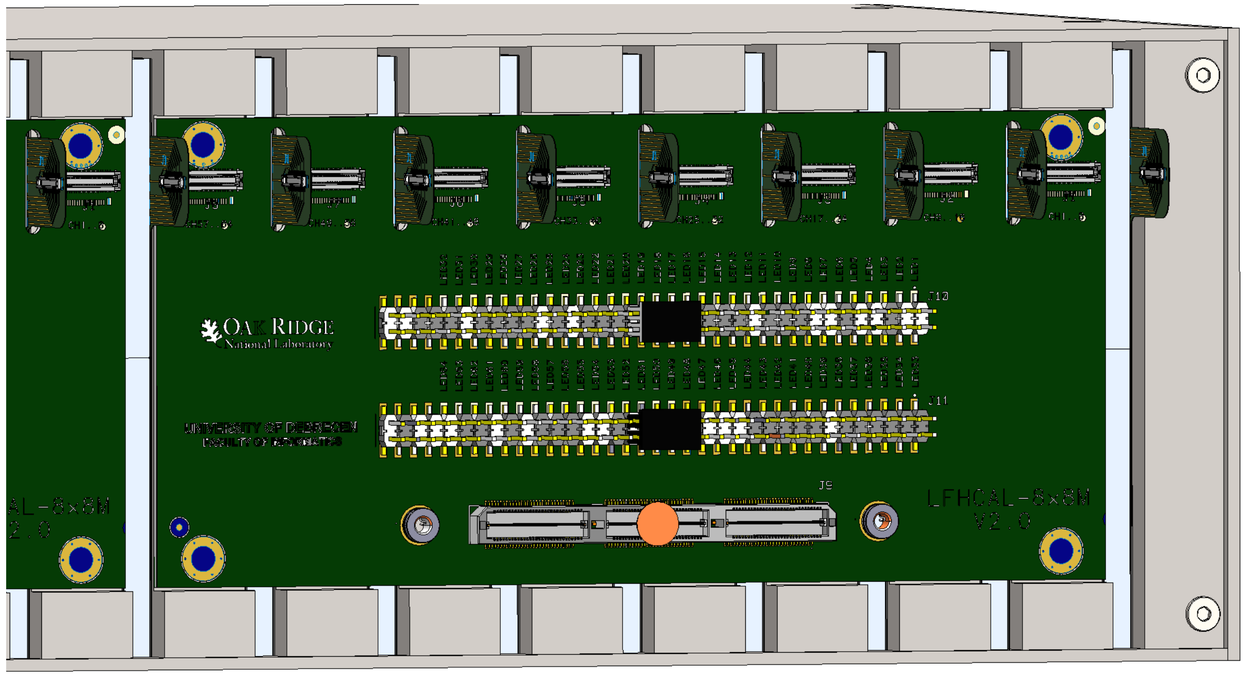


**Boxes are ready in FoCal lab**

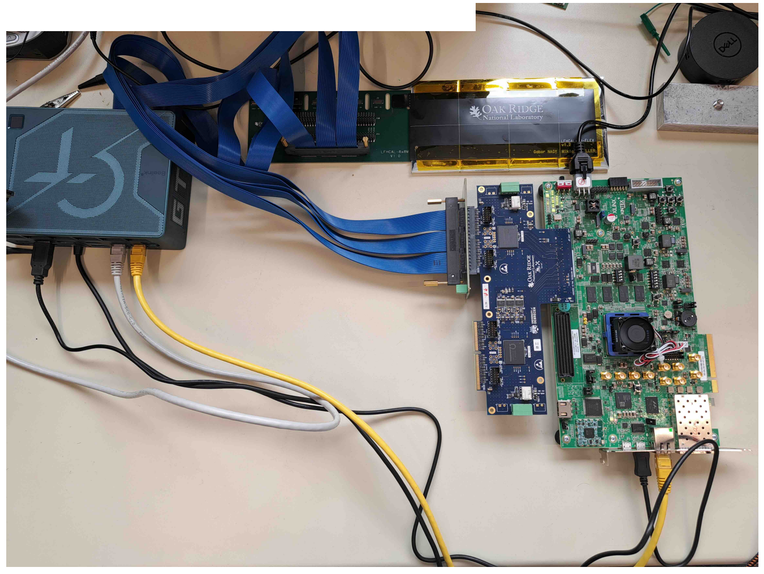
**Need 5 KCU's: ORNL, FoCal lab, KU, Miki, CTP group CERN. Need at least 1 more for spare.**

# Mechanical fit




**Visualization how it all fits together…**



# General electronics MPOD

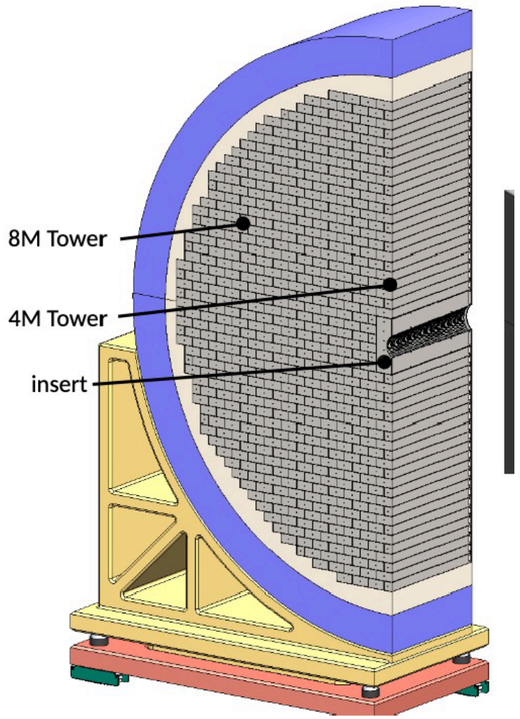
https://www.wiener-d.com/product/mpod-full-size-crate/

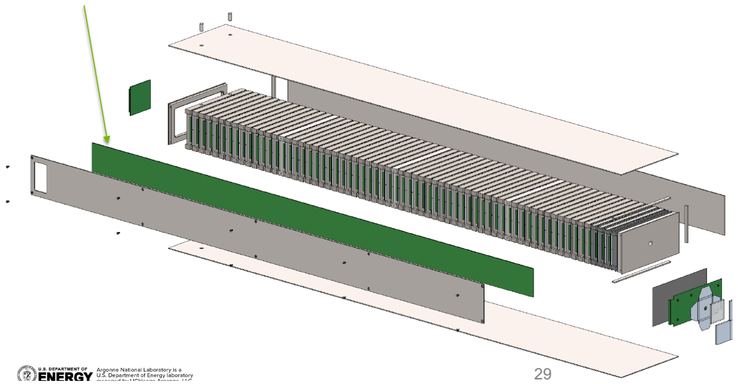
**One of these crate can handle 10 modules:**

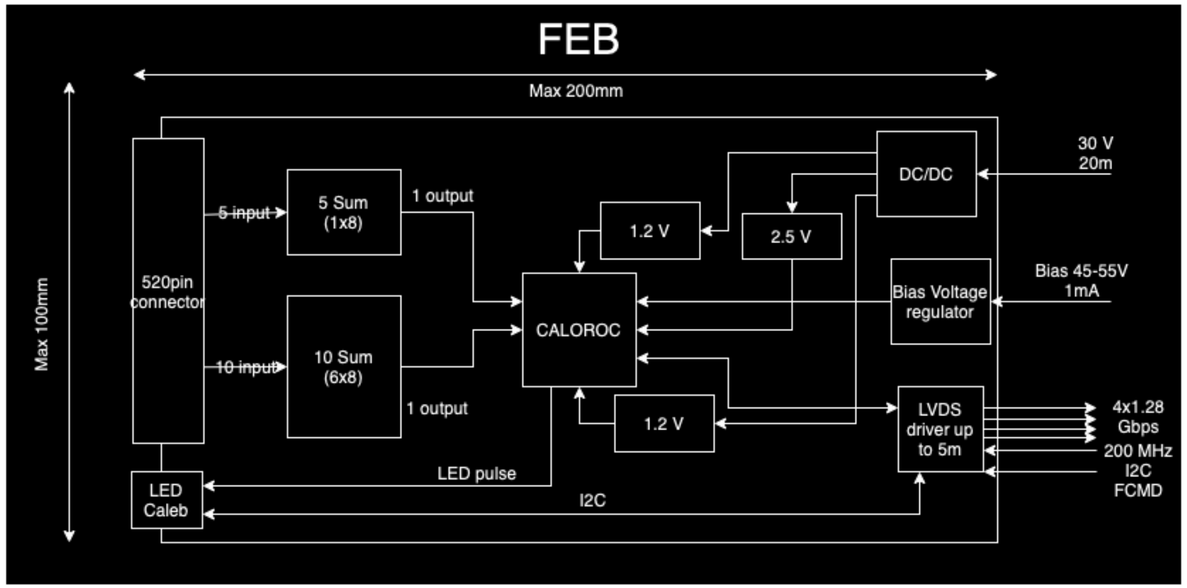
- LV we can choose between more channels+less power or less channels+more power
- Bias - 8060I model seems to fit our needs

| Type | Channels per module | Voltages | I Max | Peak Power | V-Res | I-Res | Ripple* |
|---|---|---|---|---|---|---|---|
| MPV 8008I | 8 | 0 - 8V | 10A | 50W / ch. | 0.5mV | 0.5mA | <3mVpp |
| MPV 8016I | 8 | 0 - 16V | 5A | 50W / ch. | 1mV | 0.25mA | <2mVpp |
| MPV 8030I | 8 | 0 - 30V | 2.5A | 50W / ch. | 2mV | 0.12mA | <2mVpp |
| MPV 8060I | 8 | 0 - 60V | 1A | 50W / ch. | 4mV | 0.06mA | <2mVpp |
| MPV 8120I | 8 | 0 - 120V | 100mA | 50W / ch. | 4mV | 4 µA | <2mVpp |
| MPV 8008H | 8 | 0 - 8V | 10A | 50W / ch. | 2µV | 1.5µA | <3mVpp |
| MPV 8016H | 8 | 0 - 16V | 5A | 50W / ch. | 5µV | 760nA | <2mVpp |
| MPV 8030H | 8 | 0 - 30V | 2.5A | 50W / ch. | 8µV | 760nA | <2mVpp |
| MPV 8060H | 8 | 0 - 60V | 1A | 50W / ch. | 17µV | 300nA | <2mVpp |
| MPV 8120H | 8 | 0 - 120V | 100mA | 50W / ch. | 40µV | 32nA | <2mVpp |
| MPV 4008I | 4 | 0 - 8V | 20A | 100W / ch. | 0.5mV | 0.5mA | <3mVpp |
| MPV 4016I | 4 | 0 - 16V | 10A | 100W / ch. | 1mV | 0.25mA | <2mVpp |
| MPV 4030I | 4 | 0 - 30V | 5A | 100W / ch. | 2mV | 0.12mA | <2mVpp |
| MPV 4060I | 4 | 0 - 60V | 2A | 100W / ch. | 4mV | 0.06mA | <2mVpp |

# LFHCal






- **63280 channels in total**
- **Each 8M module get an ASIC**
  - **1100 CALOROCs in total**
- **Total consumption 4345W on LV, <5W on HV:**
  - **<2400W per side (sliding)**
  - Can be covered with 6 modules in 4030I
  - HV 8 channels in 8060I module, each side would get one module

- RDO (55-60 for the whole detector)
  - 30 on each side, 222W (3 channels from 4030I, one module)

- One MPOD crate can take up to 10 modules, so each side could be handled by 1 crate (6 LV_FEB, 1 HV_FEB, 1 LV_RDO)