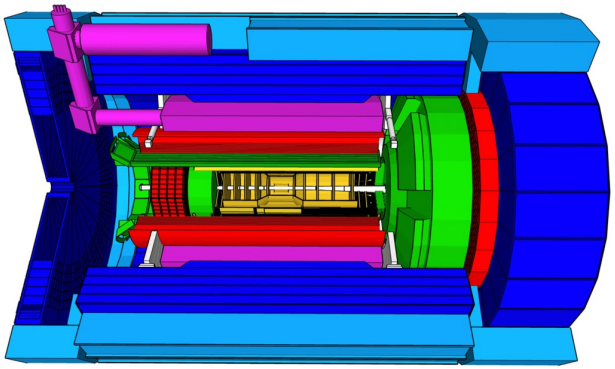

VTRX+ for the dRICH RDO

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on behalf of the dRICH DSC

Incremental Preliminary Design and Safety Review
of the EIC Detector DAQ and Electronics // June 2024

VTRX+ and dRICH

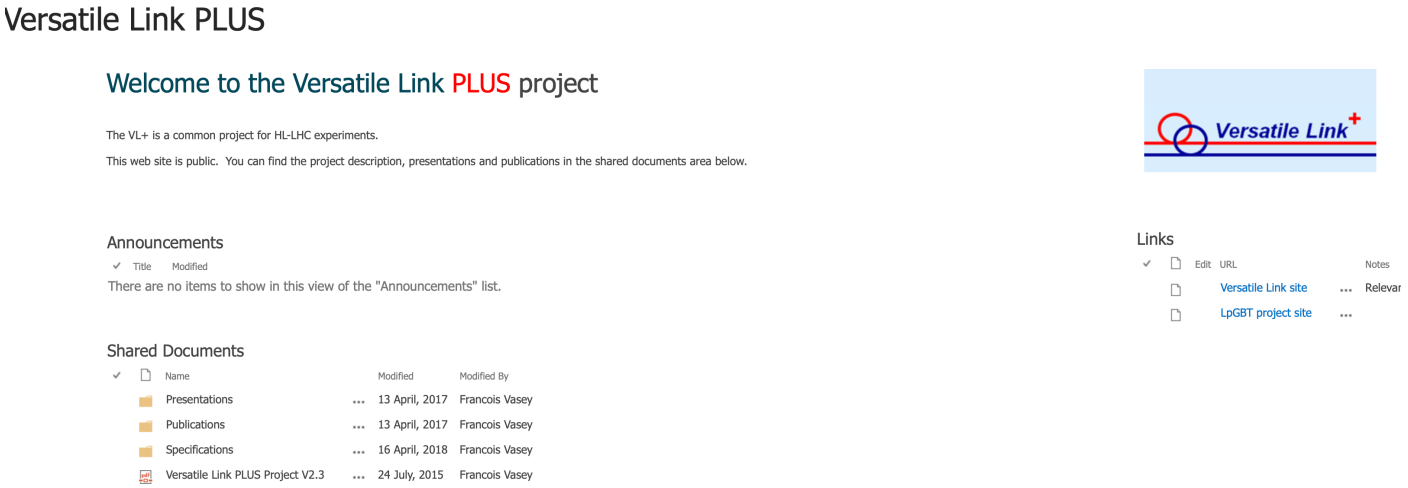
- optical link engineered by CERN: rad hard, as front-end link standard for HL-LHC (and beyond)
- all R&D and qualification done by CERN. Refer to CERN documentation
- dRICH group pointed out to EIC project/DAQ group interest back to June 2023 and the need of early procurement (only production run is next year)

This presentation:

- references about VTRX+
- why VTRX+ for dRICH RDO (re-cap)
- interface: VTRX+ on dRICH RDO
- VTRX+ integration (the pigtail)
- procurement by INFN for RDO prototypes and pre-production // expertise

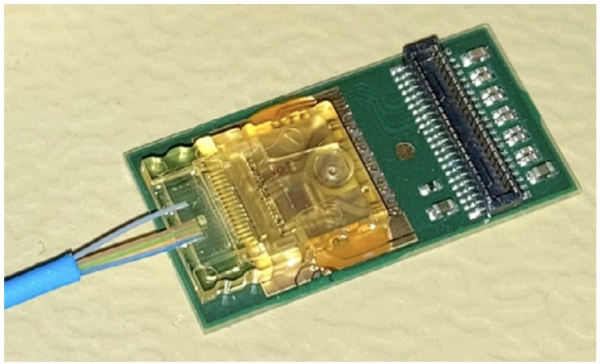
Main reference

CERN main reference: https://espace.cern.ch/project-Versatile-Link-Plus/SitePages/Home.aspx



and: https://espace.cern.ch/project-versatile-link/public/default.aspx

Motivation: space requirements + rad hard + ok in terms of bandwidth



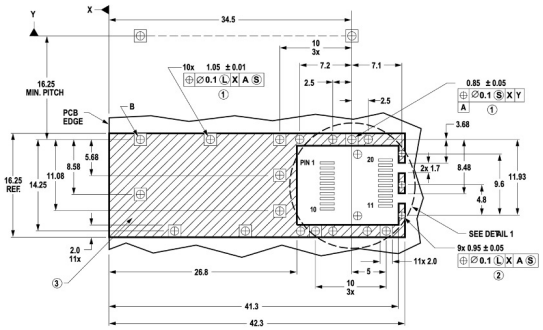
(see previous presentation on RDO)

VTRX+ gives to the dRICH:

- space
- radiation tolerance
- enough bandwitdh

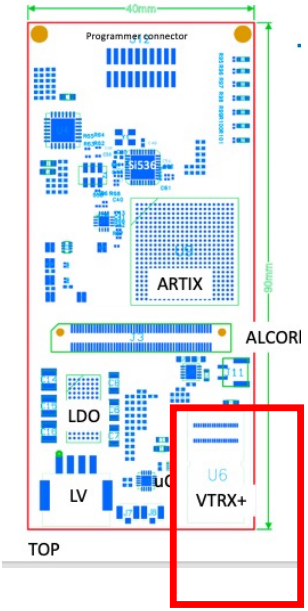
VTRX+: 20 x 10 x 2.5 mm^3

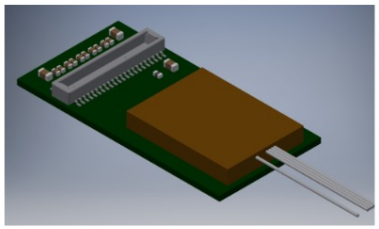
Commercial choice (just an example up to 14.025 Gb/s)

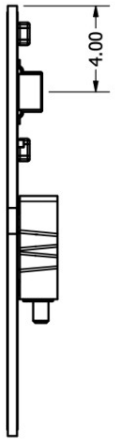


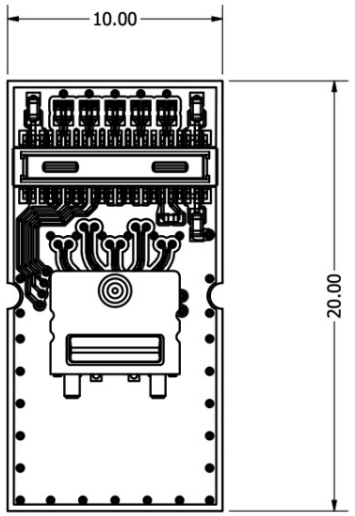
Example of commercial choice: 4.23 x 1.62 cm!

Interface (1)







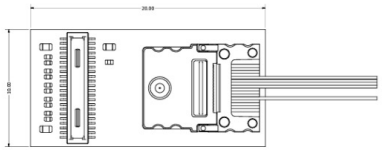


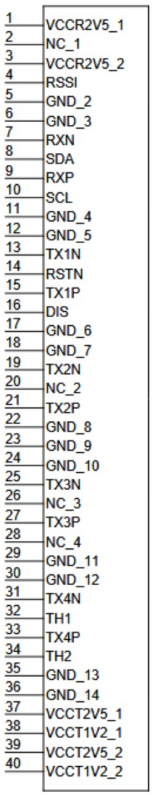
3D model from CERN used for CAD
footprint etc. from CERN in schematics/layout

Interface (2): VTRX+ connector

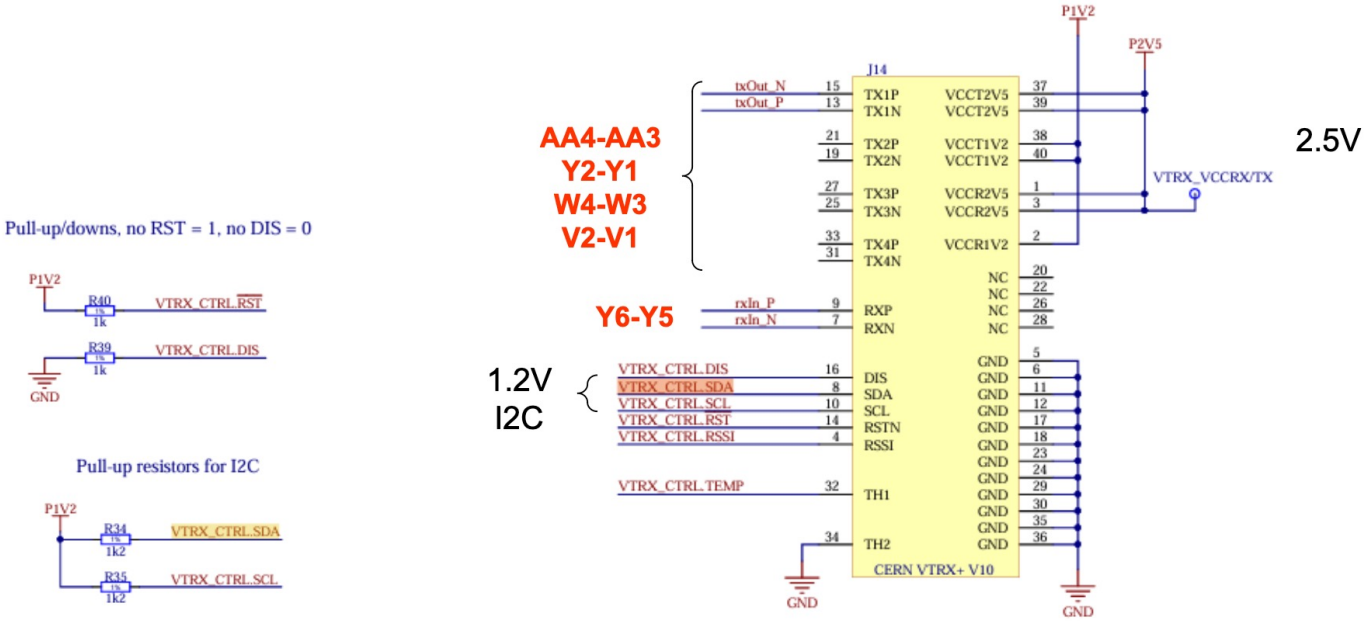
Pin #	Name	Description	Pin #	Name	Description
1	VCCR2V5	2.5V Power supply for TIA	2	n/c	
3	VCCR2V5	2.5V Power supply for TIA	4	RSSI	RSSI current output from TIA, to be pulled up via a resistor to VCCR2V5
5	GND	Ground	6	GND	Ground
7	RXN	Rx output	8	SDA	I2C data (to be pulled-up to VCCT1V2)
9	RXP	Rx output	10	SCL	I2C clock (to be terminated to VCCT1V2)
11	GND	Ground	12	GND	Ground
13	TX1N	Tx Ch.1 input	14	RSTN	Laser Driver Reset
15	TX1P	Tx Ch.1 input	16	DIS	Laser Driver Disable
17	GND	Ground	18	GND	Ground
19	TX2N	Tx Ch.2 input	20	n/c	
21	TX2P	Tx Ch.2 input	22	n/c	
23	GND	Ground	24	GND	Ground
25	TX3N	Tx Ch.3 input	26	n/c	
27	TX3P	Tx Ch.3 input	28	n/c	
29	GND	Ground	30	GND	Ground
31	TX4N	Tx Ch.4 input	32	TH1	10k Thermistor Terminal 1
33	TX4P	Tx Ch.4 input	34	TH2	10k Thermistor Terminal 2
35	GND	Ground	36	GND	Ground
37	VCCT2V5	2.5V Power supply for Laser Driver	38	VCCT1V2	1.2V Power supply for Laser Driver
39	VCCT2V5	2.5V Power supply for Laser Driver	40	VCCT1V2	1.2V Power supply for Laser Driver

HIROSE DF40HC(4.0)-40DS-0.4V connector to plug the VTRx+ on it





Interface (3): VTRX+ connections to FPGA



from https://edms.cern.ch/ui/file/2391528/2/EDA-04075-V2-0_sch.pdf

- We use just one TX line, but possiblity to connect all four
- I2C connected to Polarfire (1.2V bank)

Procurement for prototypes and production

- INFN-BO has already in hands 20 VTRX+ (for RDO prototypes in 2024/2025 (and a VLDB+ card from CERN)
- VTRX+ procurement for dRICH from the project via CD-3B→ delivery end of 2026 ok!

Additional expertise/contact

good contacts with INFN-PD (CMS): they have realized a card (CMS OBTD-CARD) with one direct interface of the VTRX+ to the FPGA **without lpGBT** as per dRICH RDO application. Reference to 2023 TWEPP presentation

Integration with dRICH == pigtail length

- for prototypes // lab tests we ordered 40 cm length pigtail
- not yet modelled on the CAD cabling on the detector box:
- it is likely a short (few cm) pigtail, connecting to a connection bar

This study will be done by end of 2025 in time for CD-3B