ppRDO Readout Board

Mike Matveev, Wei Li, Tonko Ljubicic (Rice University)
Prithwish Tribedy, Prashanth Shanmuganathan (BNL)
Zhenyu Ye (LBNL)
William Gu (JLab)

Page Turn - Incremental Preliminary Design and Safety Review of the EIC Detector DAQ and Electronics

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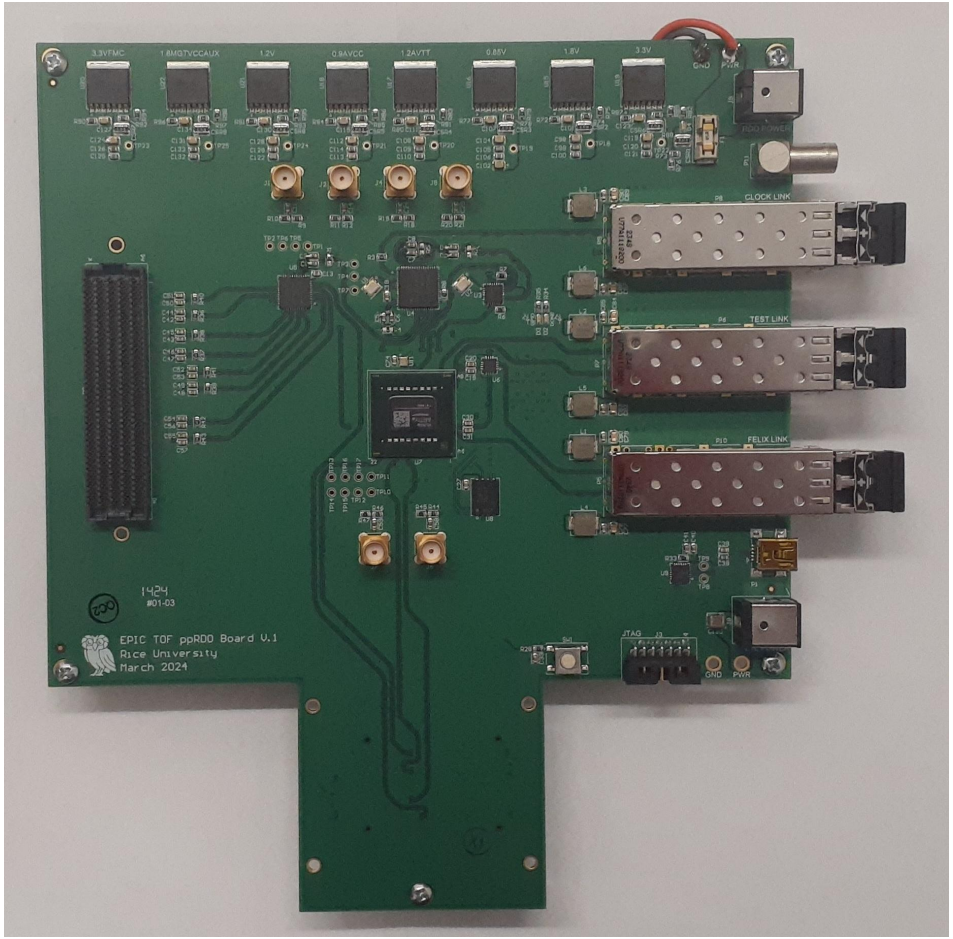
Project Definition & Goals

- ppRDO is a pre-prototype EPIC DAQ Readout Board (RDO)
  - under FY24 eRD109
  - NB: “pre-prototype” means that it is developed before detector specific prototype RDOs → generalized
- Goals
  - design and produce a prototype board with all the elements which are expected to be common to most/many EPIC detector’s Readout Boards
    - **Xilinx Artix+ FPGA** (modern, cheap, CERN TClink compatible)
    - **SFP+ fiber optics interface** (standardized, ~10 Gbs)
    - **Clock cleaner PLLs** → *jitter goal: 5ps for timing detectors* (TOF, HRPPD, Roman Pots, etc)
    - **Clock recovery mechanism using the RX of the SFP ala CERN’s TClink** (“Option A”) [William’s presentation]
      - but additionally establish Option B: direct clock transmission over a dedicated fiber
  - detailed measurement of (all sources of) clock jitter using the above schemes [William’s presentation]
  - detailed measurement of power for all voltages used
    - remember: we need 5 different voltages!
  - reasonably accurate cost estimate
  - provide hardware interfaces to EPIC’s ASIC prototype boards for testing (FMC connector)
  - firmware
    - establish procedures to readout most/many EPIC ASICs
    - develop common streaming readout scheme in concert with DAQ Group’s protocols
  - radiation testing
    - provide framework (and test FW) for SEU upset handling & measurement
    - potential use of entire board for irradiation measurements

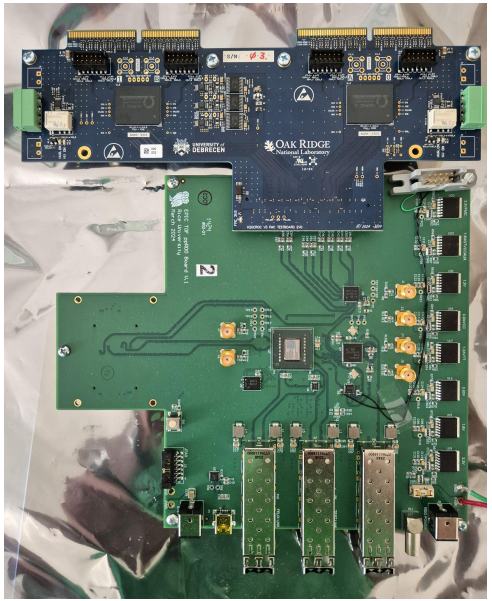
Other Features

- FMC for ASIC test boards
  - we expect EICROC2, FCFD, CALOROC, SALSA?, custom FEEs…
  - e.g. H2GCROC test board exists (next page)
- CMS ETL MB ETROC test board
  - used as a prototypical CERN-developed ASIC
- 2nd fiber interface for loopback testing
- we used linear regulators although we expect to use DC/DC converters for some voltages in the final designs
- many test points, USB console for FPGA control, Lemo fo external triggering, etc.



Current Status

- we produced 6 boards – all working after minor fixes [Mike]
- fiber & clock recovery in progress [William]
- general firmware in progress [TL]
  - PLL I2C setup, ADC readout of various monitored voltages, temperature etc.
  - TBD: remote PROM programming and readback
- readout of CMS ETL ETROC ASIC in progress [Mike, TL]
  - I2C working, basic “fast command” interface working, basic data readout working
  - goal is to make sure we know how to readout the data into the FPGA, align it on word boundary, check data coherence with CRC etc and do this at rather high rates of ~1280 Mbs
- readout of H2GCROC ASIC via their test board in progress [TL, Norbert, Miklos] ⇒
  - board recently obtained from the EPIC Calorimeter group (Norbert et al)
  - Miklos et al provided low level readout firmware & general expertise
  - BTW, we expect these specific interfaces to be ~similar to the future EICROC2 & CALOROC which is why it’s of interest now
- DAQ readout firmware, in progress [TL]
  - plan is a full 32x ASIC readout scheme where the ASICs will be emulated in VHDL
  - this will enable us to design & vet DAQ Group’s fiber protocols
  - and will be used as “test firmware” to
    - a) measure SEUs
    - b) provide schemes and algorithms to handle SEUs
  - the final output of the full emulation is a set of files which contain data very close to what our streaming DAQ will deliver → can be used by software groups



Until the end of FY24

- detailed measurements of all power needs, separately for all voltages on the board [BNL]
  - starts soon
- continue with detailed measurements & characterization of clock jitter [BNL]
  - for both clock options: recovered clock & direct clock
  - preliminary results: 5 ps
  - *supported by William*
- final integration of our ETROC example ASIC [LBNL]
  - finalize FPGA FW blocks which interface to “typical” ASICs

This will complete all the Project’s stated goals in FY24

FY25 and beyond

- finalize emulated readout of 32 ASICs using e.g. EICROC2 as the model
  - NB: this will need a small amount of additional financial support from the Project for cheap, commercial, simple PCIe FELIX board equivalents acting as PC interfaces to the RDO data
- radiation tests of critical board components
  - as soon as possible, need organization & support from the Collaboration/Project, likely not in FY24
    - FPGA & PROM
    - Clock Cleaner PLLs
    - SFP+ fiber modems
    - linear regulators
  - SEU testing & mediation protocols [need emulation, see above]
- continue using the board as a generic testbed for DAQ protocols and readout
  - in concert with the DAQ Group
- use the board as a generic RDO for other ASICs or FEEs
  - e.g. Forward Calorimeter custom FEE, future FCFD digital backend, etc
- continue using the board as a TOF-centric RDO development system [Rice]

Conclusion

Goal	Status
Produce 6 pieces	**Completed**
Develop TClink clock recovery (Option A)	Setup established; preliminary result: 5ps In progress
Develop Direct Clock (Option B)	Hardware works; clock seen but jitter not yet measured In progress
Power Measurement	Preliminary: vetted hardware, established procedure In progress
Firmware Procedures	Many completed: I2C, PLL, clocking, USB readout… In progress
ASIC interfacing; FMC connector	ETROC can be controlled & readout; H2GCROC test board obtained In progress

⇒ we plan to continue using this board for various other EPIC DAQ- and TOF-related projects