Support from DOE/eRD109

The EICROC Project

Objective: **Development** and **characterization** of an **ASIC EICROC (32 x 32)**
able to read out the new generation of pixelated (500 x 500 μm^2) silicon sensors: **AC-LGAD**
(**L**ow-**G**ain **A**valanche **D**iode) coupled **AC**
for the **Electron Ion Collider** (EIC)

1st intention: optimized for Far Forward detectors: the **Roman Pots**

Perspectives: to read out **ALL** (**pixelated** 0.5 x 0.5 mm^2) **AC-LGAD** sensors implemented in other ePIC detectors, e.g. OMD, Forward TOF, pfRICH, hpDIRC.

Stepping up through succesive ASIC iterations
to control performances fulfilling ePIC detector requirements

- **EICROC0 prototype** (16 channels; 4 x 4): under characterization since mid '23

EICROC0 requirements and design: 16 channels (4x4)

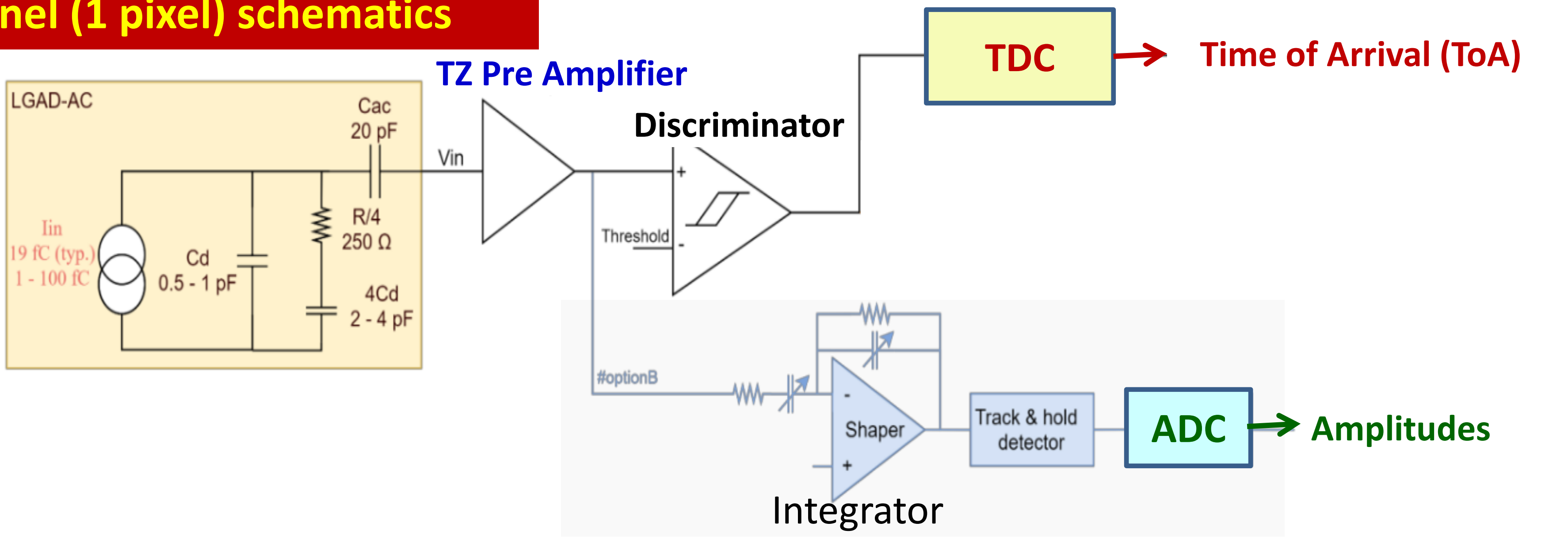
Requirements:
- pixel size **0.5 x 0.5 mm²** ***(HGTD 1.3x1.3 mm²)***
- low power consumption < **2 mW/channel**
- low jitter **~ 20 ps**
- low noise **~ 1 mV/channel**
- sensitivity to low charge **(2 fC)**
- time resolution: **30 ps**
- spatial resolution: **50 microns**

RC1

Charge sharing studies (simulation + β source w/ ALTIROC1_v2)

EICROC0 design:
- **TZ Pre Amplifiers** from ALTIROC (ATLAS/HGTD)
- 10 bit **TDC** from HGCROC (CMS, CEA/Irfu/DEDIP)
- **8 bit ADC** for time-walk correction (AGH Krakow, adapted from HGCROC)

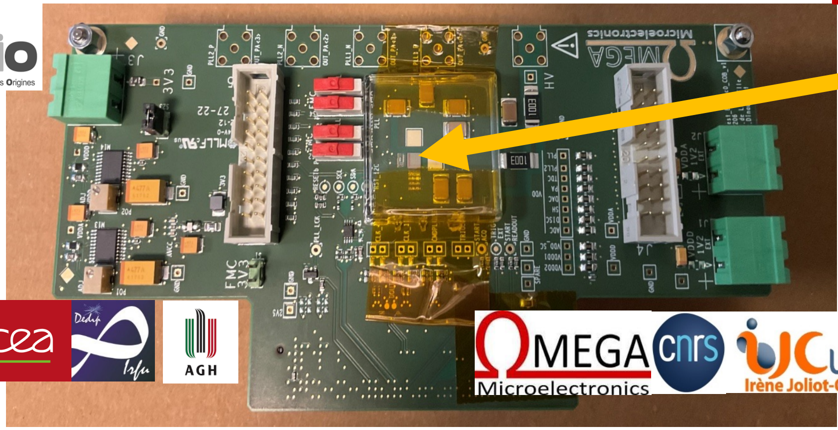
1 channel (1 pixel) schematics



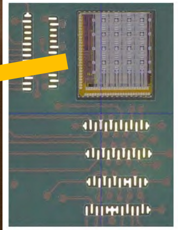
Compared to ALTIROC (ATLAS/HGTD), ToT TDC (non-linear behavior versus the deposited charge) replaced by an ADC

EICROC0 Status (1/3)

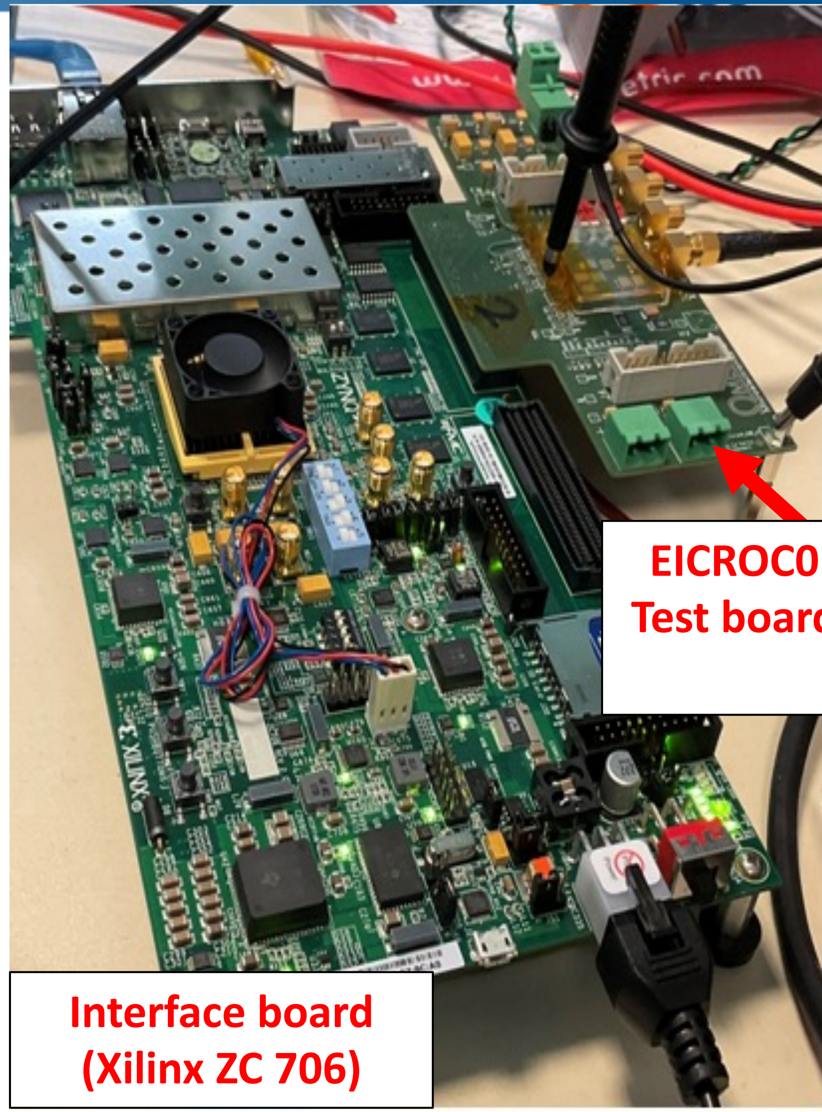
EICROC0 Test board



EICROC0 chip



Wire-bonding by Brookhaven National Laboratory



EICROC0 Test board

Interface board (Xilinx ZC 706)

EICROC0 test bench operational at IJCLab since mid '23

- ✓ I²C communication (firmware + software developments)
- ✓ Data stream written/read
- ✓ EICROC0 DC levels
- ✓ Discri. threshold exploration
- ✓ **EICROC0 charge injection system (0 to 25 fC)**
- ✓ **EICROC0 decoding (TDC, ADC) Firmware + software**
- ✓ **External trigger**: *signal directly injected into TDC*

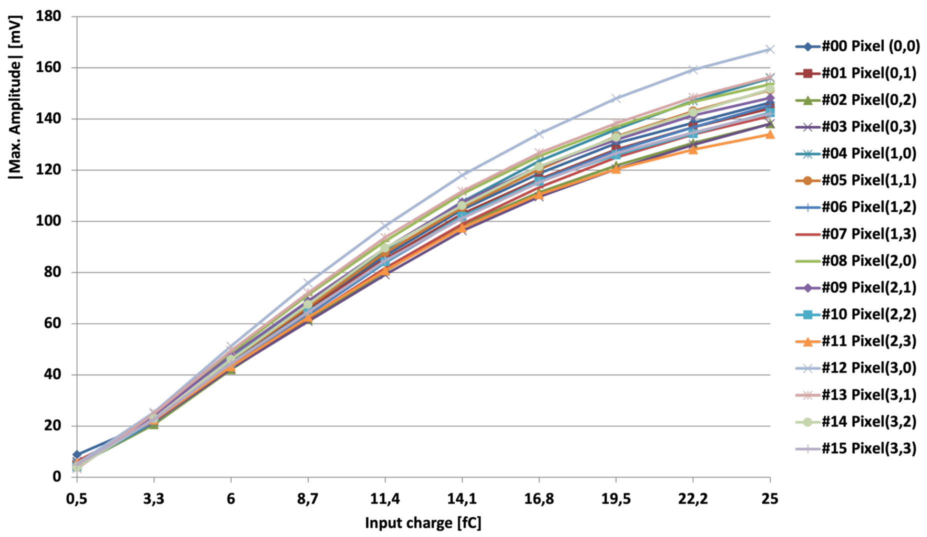
Additional EICROC0 test benches operational at OMEGA, CEA/Irfu, BNL and Hiroshima University

EICROC0 Status (2/3)

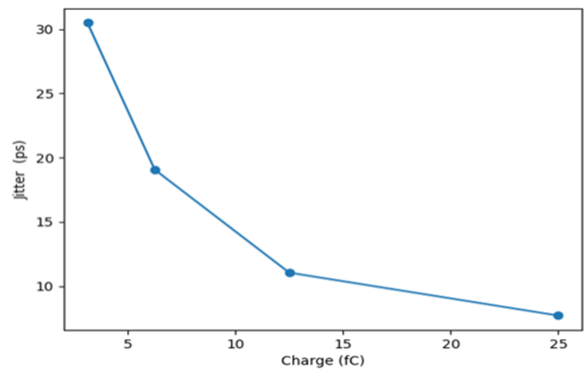
- Firmware update (old version @ Omega)
  - New version implemented ✓
  - Scripts corrected to work with new firmware ✓
- Code development for new firmware
  - Config files, test scripts, data processing scripts ✓
  - Code that allows to plot S-Curves, TDC, ADC, Hit automatically ✓
  - Uploaded on GitLab ✓
- Documentation write-up (updated over time)
  - User guide ✓
  - Code guide ✓
  - Datasheet
  - Uploaded on GitLab ✓
- Tests on ASIC with new firmware and scripts
  - S-Curves ✓
- New boards have been produced and assembled
  - Measurements on-going

EICROC0 1st prototype (4x4 pads) characterization status (3/3)

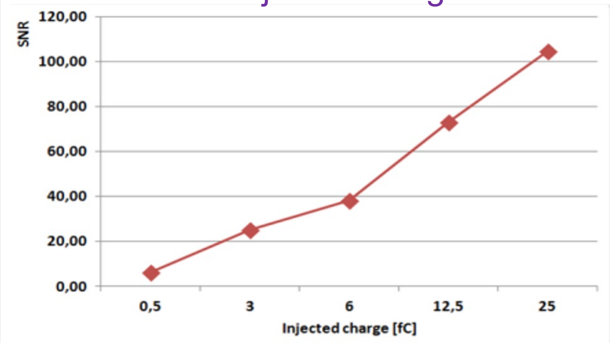
|Probe PA Max. Ampl.| vs injected charge (16 channels)



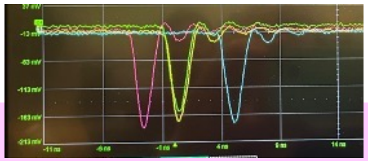
Probe PA jitter vs injected charge

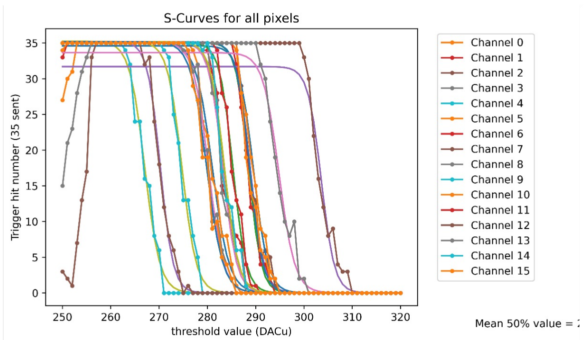


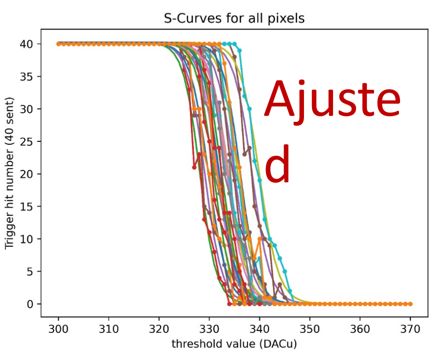
Probe PA Signal-to-Noise Ratio vs injected charge



Discriminator efficiency (S-Curves) vs threshold







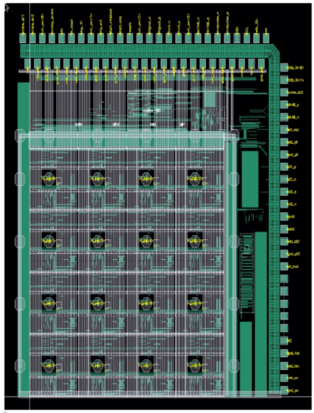
Feature of EICROC0 test board:

Capability to observe 4 Probe PA channels simultaneously

Status:

- ➢ **Individually each component shows performance in agreement with design**
- ➢ Evaluation of cross-talk between neighboring channels underway
- ➢ **Investigation of noise / clock couplings** ***(preventing us to fully exploit TDC & ADC data)*** **mandatory to drive next ASIC iteration**
- ➢ **Board with AC-LGAD sensor: investigation of oscillation origin when > 2 Probe PA channels**

EICROC Project Overview



- EICROC0 is a testbeam prototype => sensor characterization
  - Triggered readout, all data shipped out : 16 ch * 8 samples ADC + TDC
  - Present power ~2 mW/ch + 4*20 mW « analog probe preamp »
  - Status : measurements in progress
  - ADC power + shaper/driver to be reduced from ~1 mW to 100 µW/ch => EICROC0A
  - EICROC0A : simulations in progress

- EICROC1 will address larger dimensions 4x16 or 8x16 or 4x32 or <u>8x32</u>
  - Address floor planning and power distribution
  - Selective readout : hit + 9 neighbouring channels
  - Status : layout started based on EICROC0, adding more testability
  - Still EICROC0-like readout

- EICROC2 final size : 32x32

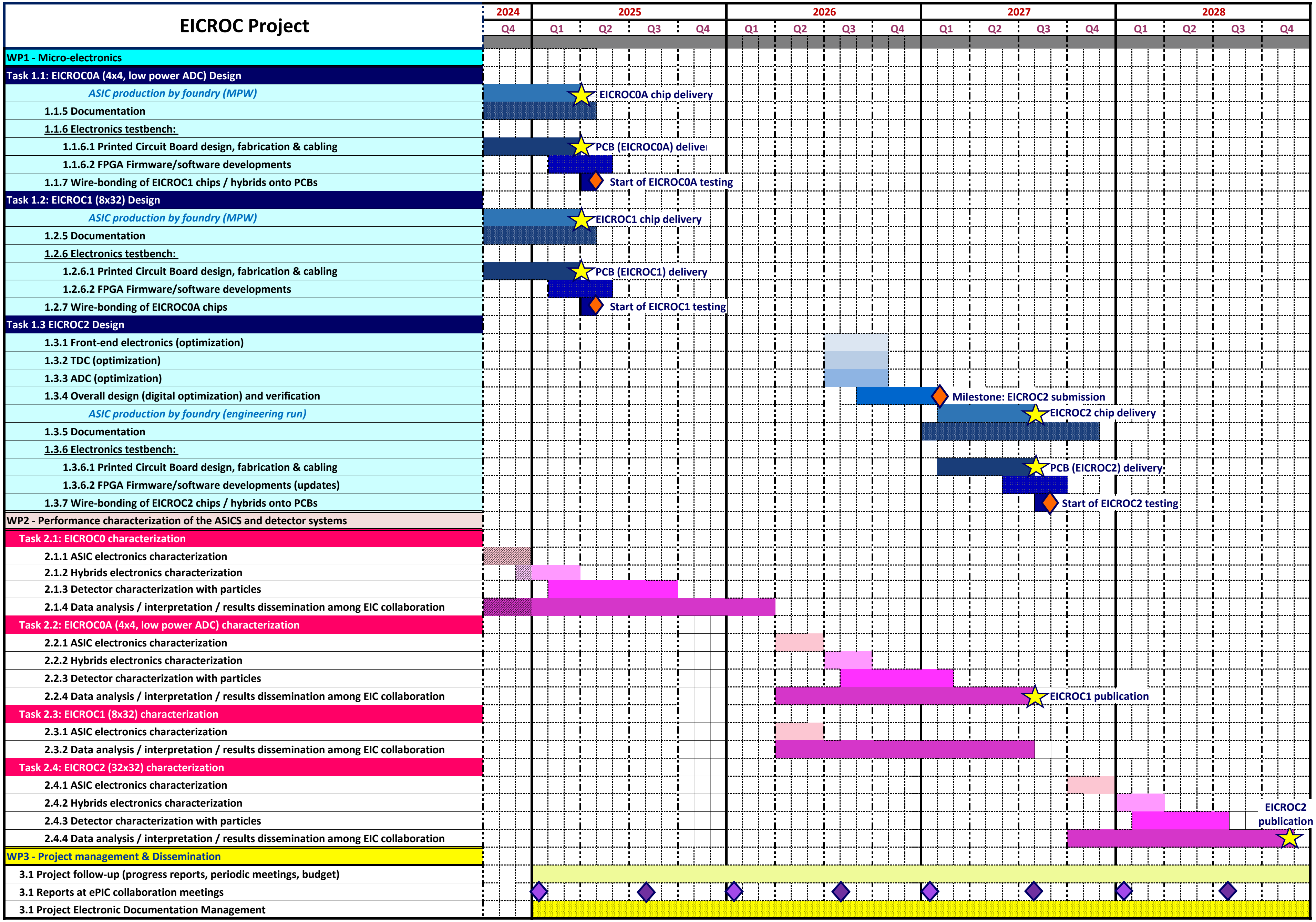
EICROC Project

Dominique Marchand (IJCLab)
Scientific coordinator

- **WP #1 : "Micro-electronics design"** — Christophe de la Taille (OMEGA) - coordinator
  - EICROC0, EICROC0_v1, EICROC1/2
    - Front-End Electronics — 1.1.1: C. de la Taille, N. Seguin-Moreau, A. Verplancke
    - Low power ADC — 1.1.2: C. de la Taille, A. Verplancke
    - TDC (TOT) — 1.1.3: F. Bouyjou, E. Delagnes
    - Overall design Documentation — 1.1.4: C. de la Taille, N. Seguin-Moreau, G. Martin-Chassard, L. Serin, A. Verplancke
    - Test bench + "firmware" — 1.1.5: P. Dinaucourt, C. de la Taille, B.-Y. Ky, A. Verplancke
- **WP #2 : "Characterization and performance evaluation"** — Dominique Marchand (IJCLab) - coordinator
  - EICROC0, EICROC0_v1, EICROC1/2
    - Functional response ASIC alone — 2.1.1: L. Serin, P.-K. Wang (2023), B.-Y. Ky, D. Marchand, C. Munoz-Camacho, C. de la Taille, N. Seguin-Moreau, A. Verplancke
    - Functional response ASIC + AC-LGAD — 2.1.2: L. Serin, P.-K. Wang (2023), B.-Y. Ky, D. Marchand, C. Munoz-Camacho, C. de la Taille
    - Source Beta IR laser Beam test — 2.1.3: A.-S. Torrento, L. Serin, P.-K. Wang (2023), E. Rauly, D. Marchand, C. Munoz-Camacho, C. de la Taille
    - Data analysis / interpretation — 2.1.4: L. Serin, P.-K. Wang (2023), D. Marchand, C. Munoz-Camacho, E. Rauly, A.-S. Torrento, C. de la Taille

IJCLab members — IJCLab Irène Joliot-Curie
OMEGA members — ΩMEGA Microelectronics
CEA/Irfu/DEDIP members — cea Dedip Irfu

+ 1 year postdoctoral position IJCLab (01/07/24 ->)
+ A. Tricoli's team Brookhaven National Laboratory
synergy with Japanese & Taiwanese teams


EICROC Project
2024
2025
2026
2027
2028
Q4
Q1
Q2
Q3
Q4
WP1 - Micro-electronics
Task 1.1: EICROC0A (4x4, low power ADC) Design
ASIC production by foundry (MPW)
1.1.5 Documentation
1.1.6 Electronics testbench:
1.1.6.1 Printed Circuit Board design, fabrication & cabling
1.1.6.2 FPGA Firmware/software developments
1.1.7 Wire-bonding of EICROC1 chips / hybrids onto PCBs
Task 1.2: EICROC1 (8x32) Design
ASIC production by foundry (MPW)
1.2.5 Documentation
1.2.6 Electronics testbench:
1.2.6.1 Printed Circuit Board design, fabrication & cabling
1.2.6.2 FPGA Firmware/software developments
1.2.7 Wire-bonding of EICROC0A chips
Task 1.3 EICROC2 Design
1.3.1 Front-end electronics (optimization)
1.3.2 TDC (optimization)
1.3.3 ADC (optimization)
1.3.4 Overall design (digital optimization) and verification
ASIC production by foundry (engineering run)
1.3.5 Documentation
1.3.6 Electronics testbench:
1.3.6.1 Printed Circuit Board design, fabrication & cabling
1.3.6.2 FPGA Firmware/software developments (updates)
1.3.7 Wire-bonding of EICROC2 chips / hybrids onto PCBs
WP2 - Performance characterization of the ASICS and detector systems
Task 2.1: EICROC0 characterization
2.1.1 ASIC electronics characterization
2.1.2 Hybrids electronics characterization
2.1.3 Detector characterization with particles
2.1.4 Data analysis / interpretation / results dissemination among EIC collaboration
Task 2.2: EICROC0A (4x4, low power ADC) characterization
2.2.1 ASIC electronics characterization
2.2.2 Hybrids electronics characterization
2.2.3 Detector characterization with particles
2.2.4 Data analysis / interpretation / results dissemination among EIC collaboration
Task 2.3: EICROC1 (8x32) characterization
2.3.1 ASIC electronics characterization
2.3.2 Data analysis / interpretation / results dissemination among EIC collaboration
Task 2.4: EICROC2 (32x32) characterization
2.4.1 ASIC electronics characterization
2.4.2 Hybrids electronics characterization
2.4.3 Detector characterization with particles
2.4.4 Data analysis / interpretation / results dissemination among EIC collaboration
WP3 - Project management & Dissemination
3.1 Project follow-up (progress reports, periodic meetings, budget)
3.1 Reports at ePIC collaboration meetings
3.1 Project Electronic Documentation Management
EICROC0A chip delivery
PCB (EICROC0A) delive
Start of EICROC0A testing
EICROC1 chip delivery
PCB (EICROC1) delivery
Start of EICROC1 testing
Milestone: EICROC2 submission
EICROC2 chip delivery
PCB (EICROC2) delivery
Start of EICROC2 testing
EICROC1 publication
EICROC2
publication

EICROC Project summary& Perspectives

- **Design of an updated PCB (improved testability, grounds); 10 pieces**
  - Cabled at IJCLab
  - EICROC0 wire-bonded onto updated PCB (IPHC, France): 2 boards (April ‘24)
  - Characterization of electronics responses (PA, TDC, ADC) on-going
  - Wire-bonding of an AC-LGAD sensor (IPHC France) by end of June ‘24
  - Beta Source (evaluation of charge sharing), IR laser (evaluation of spatial resolution)

- **Perspectives:**
  - EICROC0 bump-bonded to an AC-LGAD sensor (to be provided by BNL)
  - Wire-bonding of hybrids onto uodated PCBs (IPHC, prestation)
  - Characterization of electronics responses (PA, TDC, ADC)
  - Beta Source (evaluation of charge sharing), IR laser (evaluation of spatial resolution)
  - Test beam

- **Next foreseen ASIC iterations:**
  - **EICROC0A**: 4x4 (idem EICROC0) including 8-bit low power ADC
  - **EICROC1**: 8x32 pads to study floor planning, ground distribution

Design underway
Submission Autumn ‘24

Thank you for your attention

The EICROC Project French team:

F. Bouyjou, S. Conforti, E. Delagnes, P. Dinaucourt, F. Dulucq, B.-Y. Ky, C. de La Taille, D. Marchand, C. Munoz, N. Seguin-Moreau, L. Serin, A. Verplanck

Support from DOE/eRD109

BACKUP

ePIC TOF
Readout and DAQ

Tonko Ljubicic
BNL

July 5-6, 2023

Presentation Overview

- The ePIC TOF Readout Board(s)
  - One of the main components of the Readout Chain
    - Often called “Service Hybrid” in silicon detectors
  - Interface PCB between the ASICs (electrical) and DAQ (fiber)
  - Requirements
  - Different form factors for ETOF vs BTOF
- Integration and Common Features with the ePIC DAQ Group

Readout Board ("RDO")

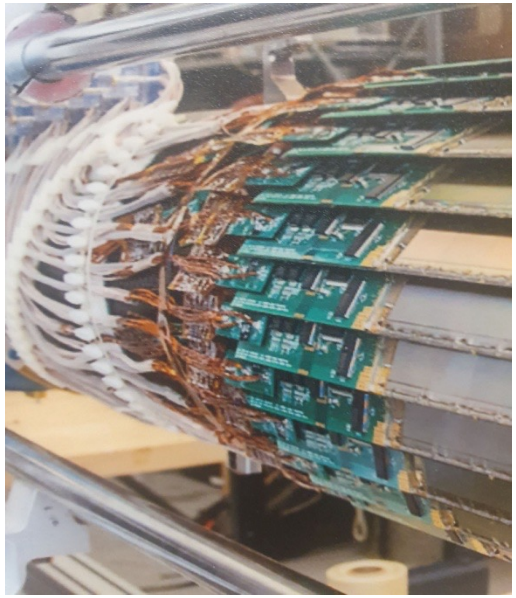
- **Main Readout Electronics Component**
- **Requirements**
  - interfaces to the readout ASIC (E.g. EICROC)
    - provides the data path <u>to</u> the ASIC for configuration/control
    - provides the data path <u>from</u> the ASIC for data/status
    - provides low jitter clock(s) to the ASIC: **5 ps jitter**
      - very low jitter to be able to maintain a 30ps timing resolution
  - interfaces to ePIC DAQ via high speed fiber links
    - downlink
      - ASIC configuration data
      - clock recovery
    - uplink (in streaming mode)
      - ASIC data (and status)
  - small, cheap, low power
- **Components**
  - FPGA + associated configuration PROM
  - SFP+ fiber interface (~10 Gbs; likely asymmetric up/download)
  - PLLs and clock cleaners
  - connectors to the ASICs

Readout Board Design Stages

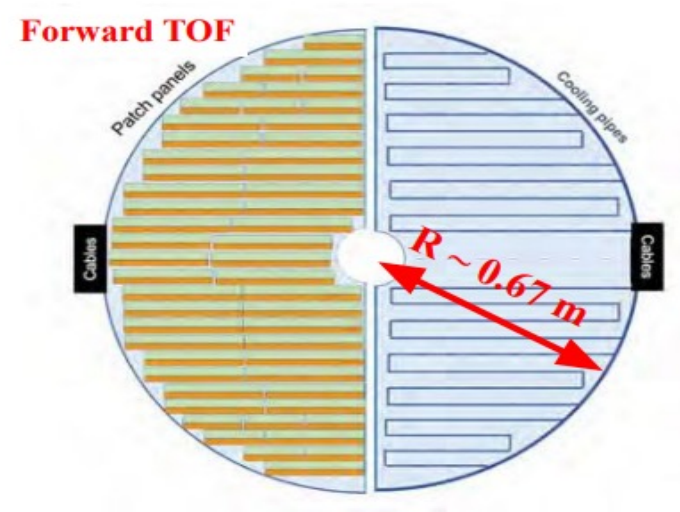
- **Stage 1** (now)
  - The RDO is prototyped with a Xilinx Development Kit (e.g. Xilinx ZCU106)
  - The sensor and EICROC ASIC is mounted on a separate PCB (“FEB”) for prototyping
  - FEB and RDO are connected via the FMC connector of the dev-kit as shown by Dominique in her presentation
- **Stage 2**
  - The RDO is custom crafted using the FPGA and other components expected to be used for the “final” version (in concert with ePIC DAQ)
    - current FPGA choice is a Xilinx Artix Ultrascale+
  - FEB (with ASIC & sensor) prototype continues to be connected via the FMC connector as in 1)
- **Stages 3+**
  - The RDO is similar to Stage 2) but TOF-specific with the “final” choice of connectors and their numbers
  - connected with TOF-specific cables to a TOF-specific invocation of the sensor+ASIC package
  - at this Stage we will likely split the RDO into 2 flavors: ETOF & BTOF

RDO Form Factors & Channel Counts

- **BTOF Readout Board**
  - 64 ASICs per RDO
  - RDO is located at the end of the staves
    - similar to the STAR IST detector ➔
  - **288 RDOs total**
    - 2.36M channels
  - expected data rate is <0.6 Gbs/fiber



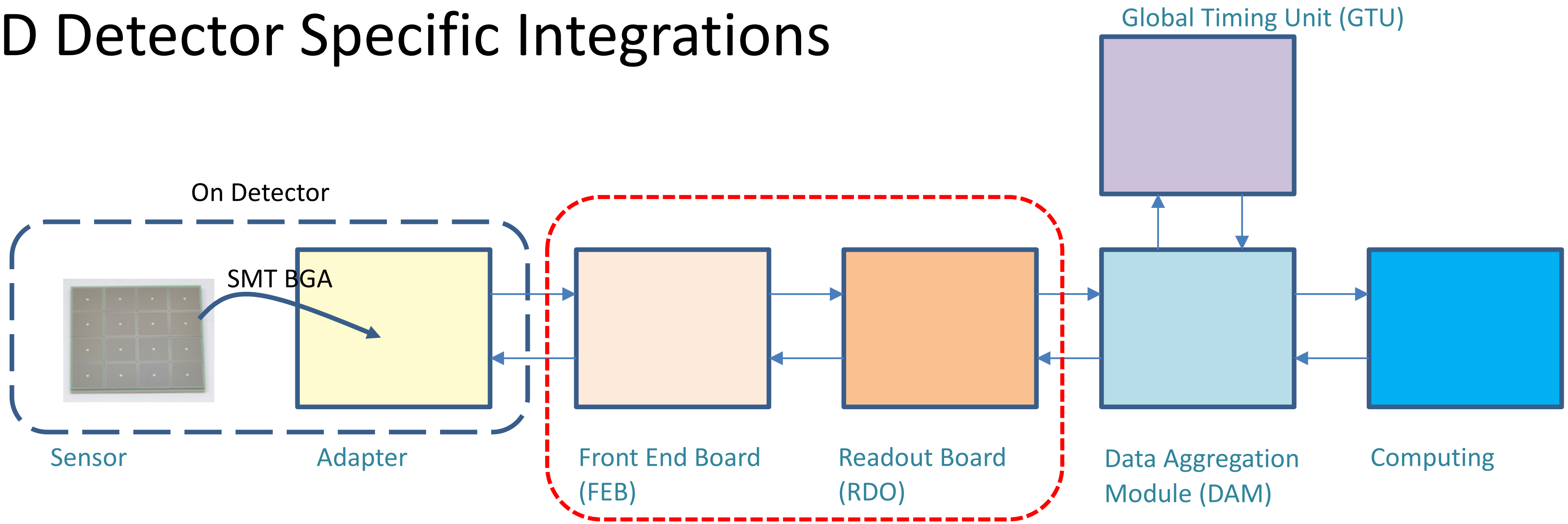
- **ETOF Readout Board**
  - from 24 to 48 ASICs per RDO
  - RDO is situated in the plane of the Detector clam-shells (see Wei's presentation) ➔
  - **212 RDOs total**
    - 8.9M channels
  - expected data rate is ~3 Gbs/fiber



Interfaces with ePIC DAQ

- **We maintain a tight integration with the ePIC DAQ Group both for prototyping and later for final versions**
  - choice of FPGA and configuration PROM
  - type, speed & protocols of the fiber links
  - clock recovery scheme (very important for TOF!)
  - design stages and use of FPGA development kits/boards
  - general philosophy and approach
- **Actual design blocks (VHDL code) of the FPGA will be shared and/or developed within ePIC DAQ**
  - general infrastructure & framework of the VHDL blocks
  - fiber to/from interfacing
    - including configuration/status
  - clock recovery blocks
  - I2C blocks (e.g. Temperature/Id chip readout)
- **Only the ASIC-specific readout blocks will be provided by TOF and "glued" to the FPGA framework**
- **➔ This approach provides maximum cost savings and risk reductions through commonalities across subsystems in ePIC DAQ**

PID Detector Specific Integrations

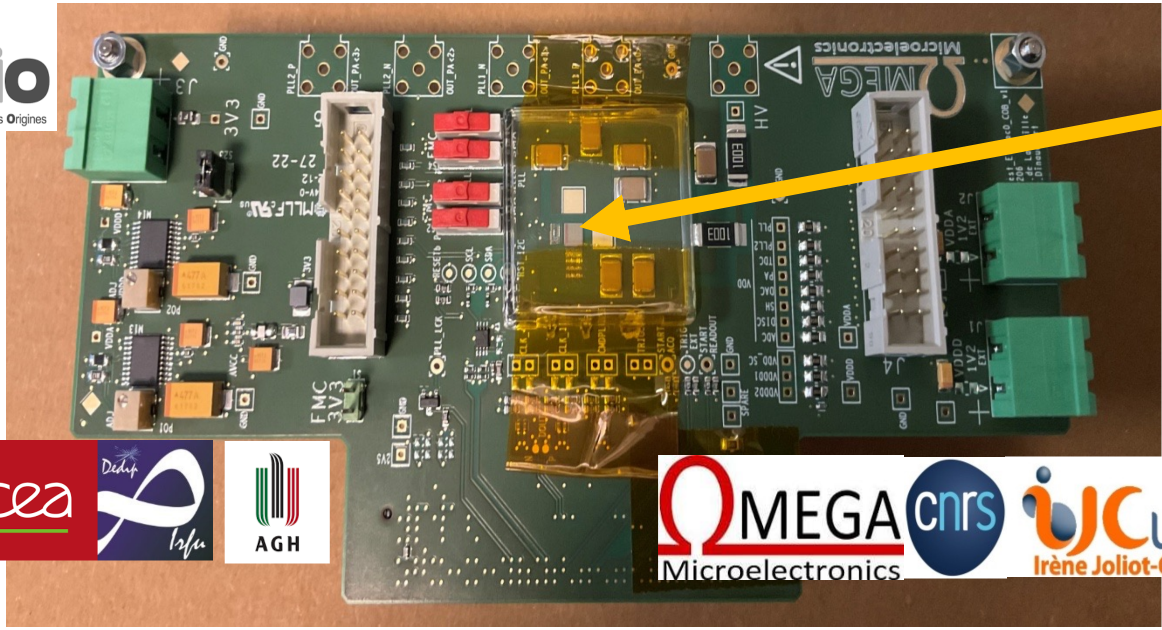


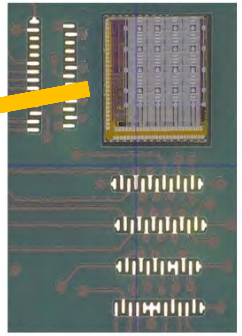
Detector	ASIC	RDO/Fiber	DAM	Data rate	Det. Tech
pfRICH	EICROC	17	1	15Gbs	LAPPD/HRPPD
dRICH	ALCOR	1252	30	1800Gbs	SiPM
hpDIRC	EICROC	288	6	11Gbs	LAPPD/HRPPD
TOF (B) TOF (FEC)	EICROC	240-500	12	6Gbps	LAPPD/HRPPD

EICROC0: EIC Roman Pots 4x4 AC-LGAD readout test chip

- Submitted through a Multi Project Wafer (**130 nm** CMOS technology) in March 22
  EICROC0 chips delivered mid-July 22
- **Test board** (PCB) designed by OMEGA, 10 pieces **delivered end of July 22**
  - test board partially cabled by IJCLab
- **Wire-bonding** of EICROC0 to test boards by **BNL collaborators**
- Delivery at IJCLab of 3 test boards w/ EICROC0 chip in **Oct. 22**
- Interface board (Xilinx ZC 706): (I^2C communication)firmware/software developments (IJCLab)

EICROC0
Test board





EICROC0 chip

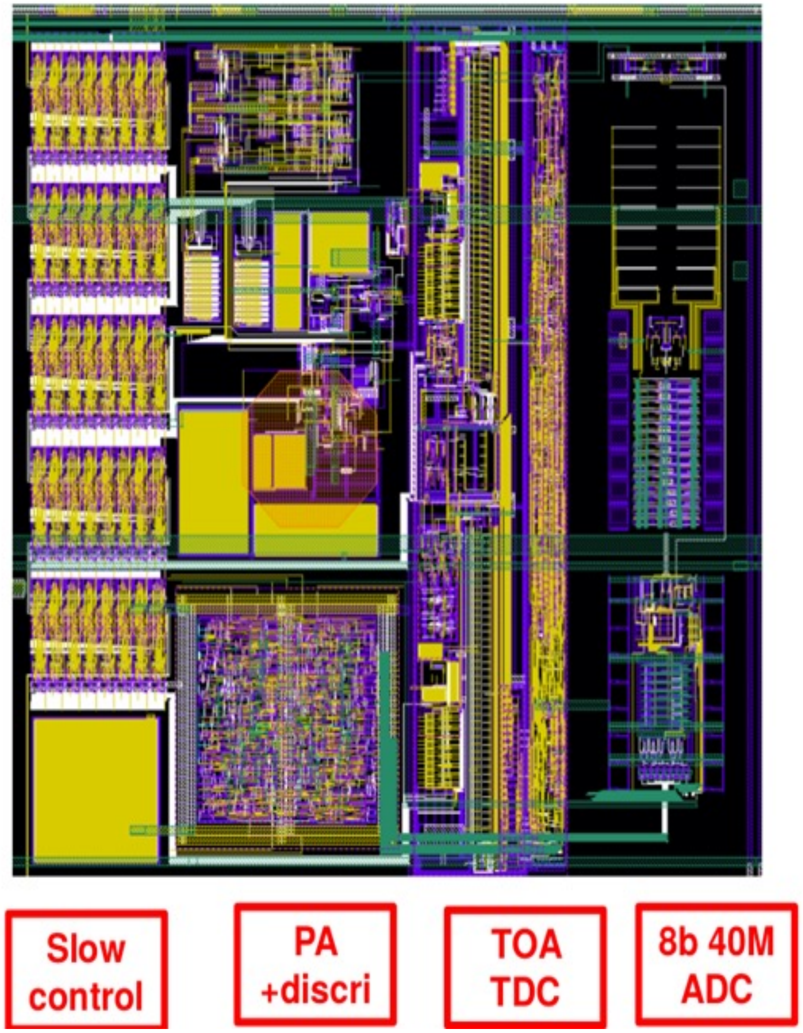
EICROC0: overview

- High speed TZ PA and discriminator (from ALTIROC)
- I^{2}C slow control (from CMS HGCROC)
- 8 bits 40 MHz ADC (adapted from HGCROC 10 bits ADC, M. Idzik *et al.*, AGH Krakow)
- Digital readout FIFO (depth 8, 200 ns)
- 10 bits **TDC** (TOA) designed by **CEA Irfu/DEDIP**:

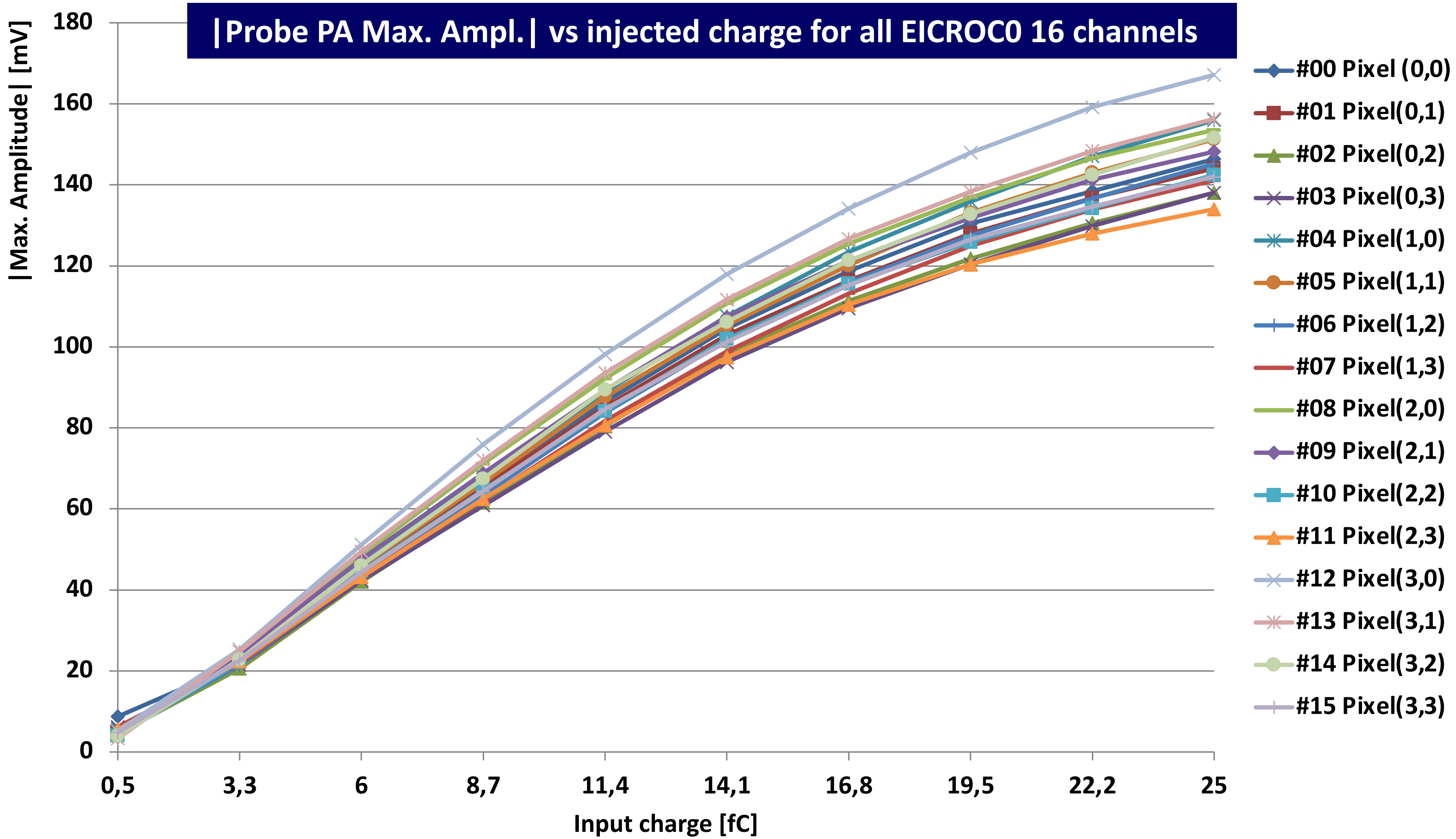
HGCROC TDC (1 mm x 120 µm):
- spatially adapted to fit in a pixel of 0.5 x 0.5 mm^2
- optimization in terms of dynamic range and resolution (10 ps rms) as well as power consumption
- common block for calibration of all TDC channels

✸ <u>5 slow control bytes/pixel:</u>
- 6 bits local threshold
- 6 bits ADC pedestal
- 16 TDC calibration bits
- Various on/off and probes

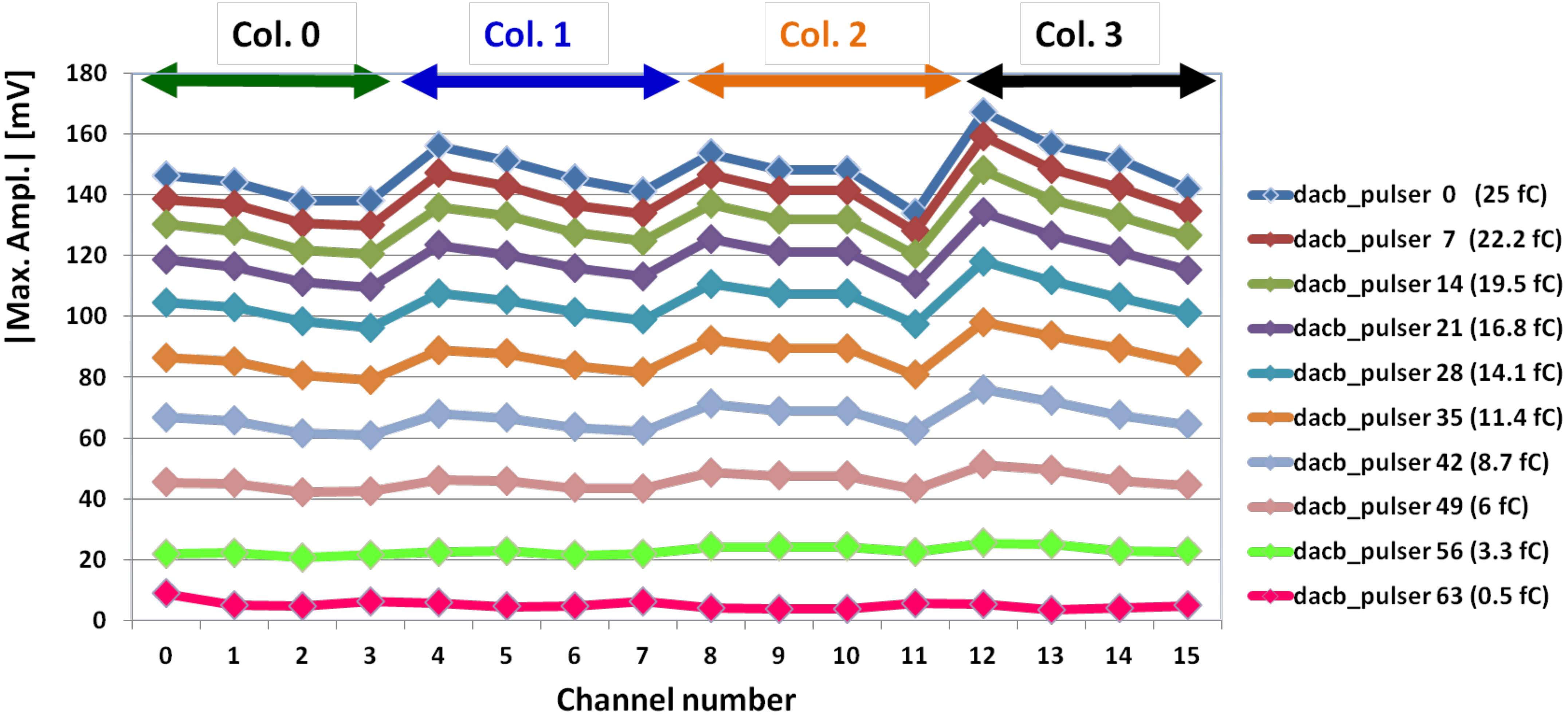
EICROC0 layout (1 pad = 1 channel)



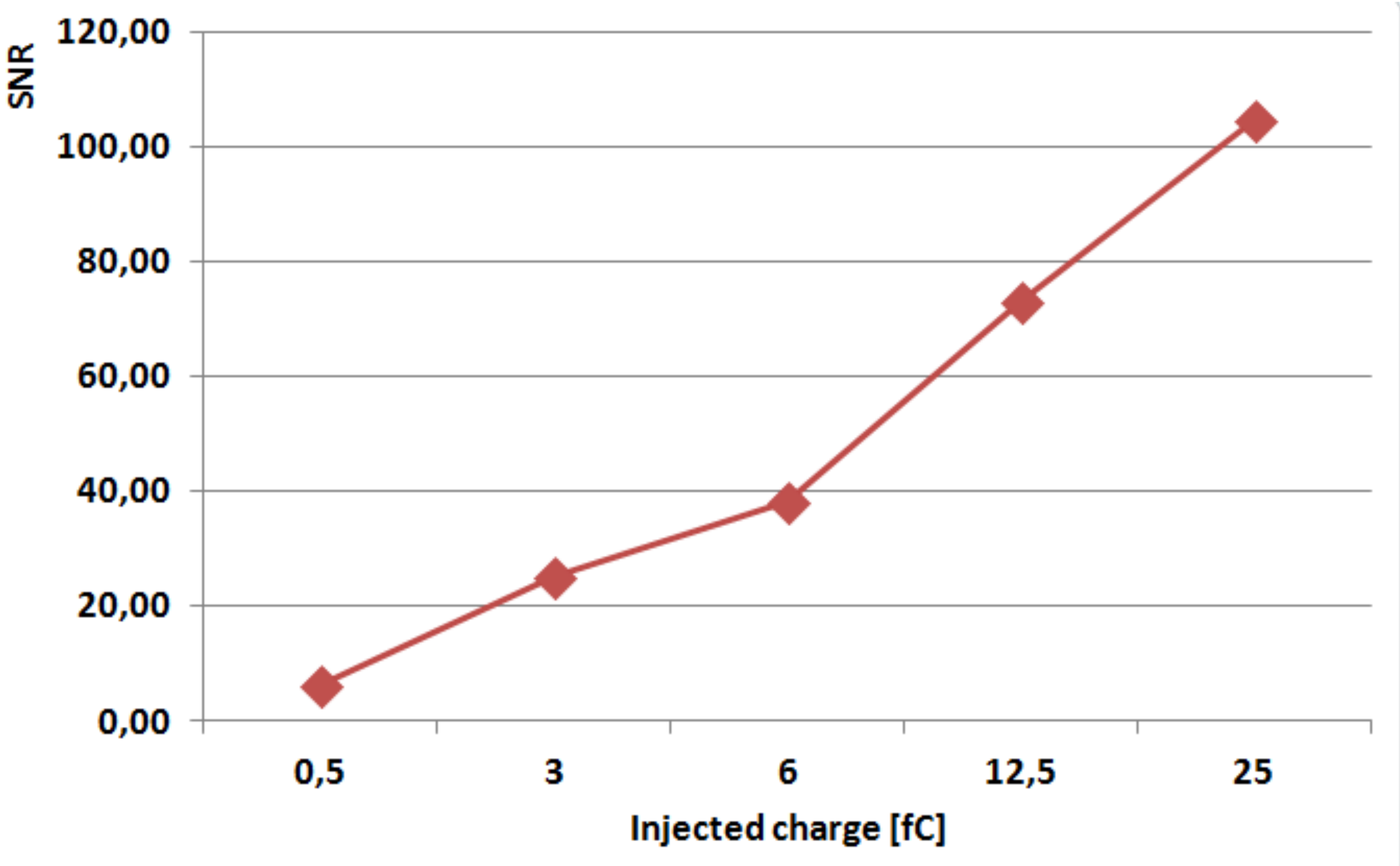
EICROC0 TZ Pre Amplifier Probe output signal amplitudes



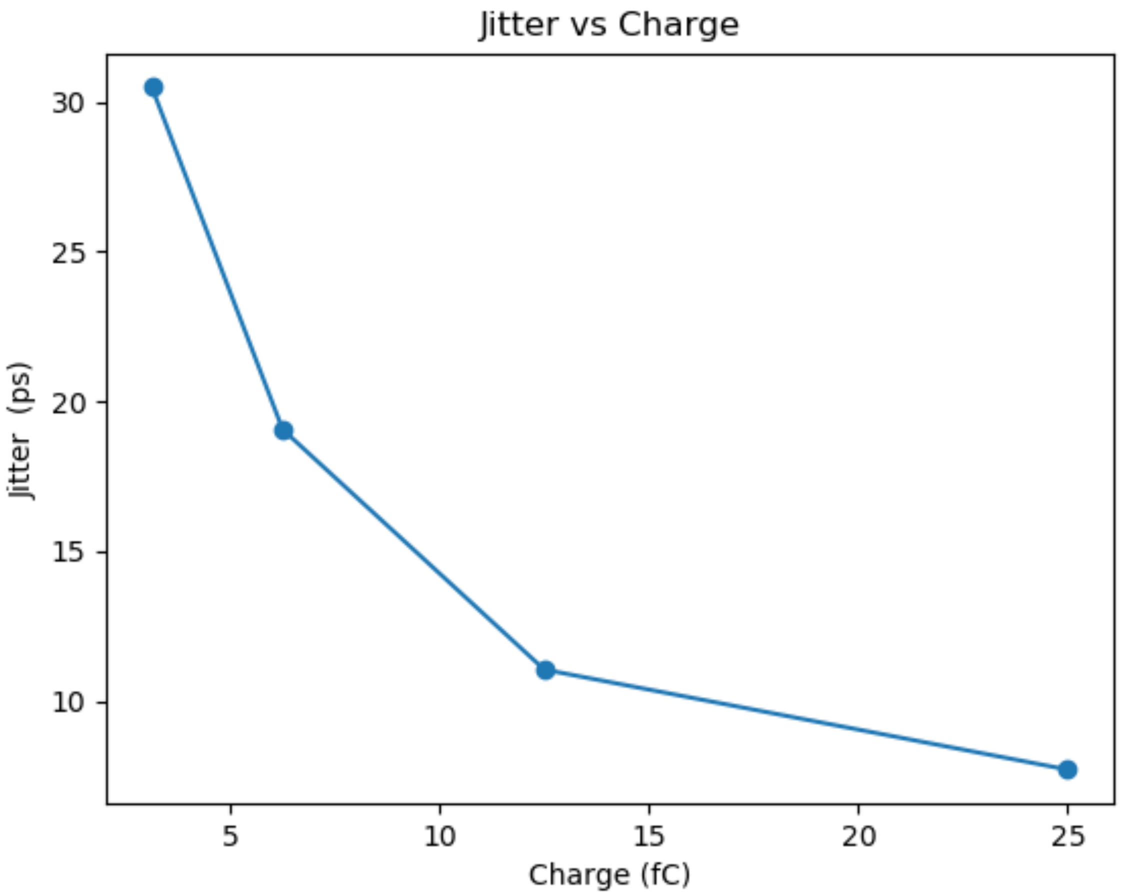
EICROC0 TZ Pre Amplifier Probe output signal amplitudes



EICROC0 Probe PA output Signal to Noise Ratio (SNR)

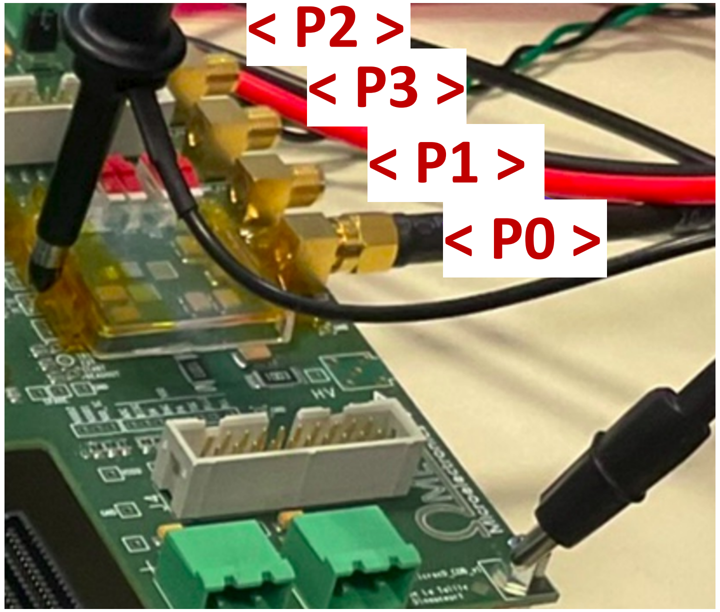


EICROC0 Probe PA output jitter

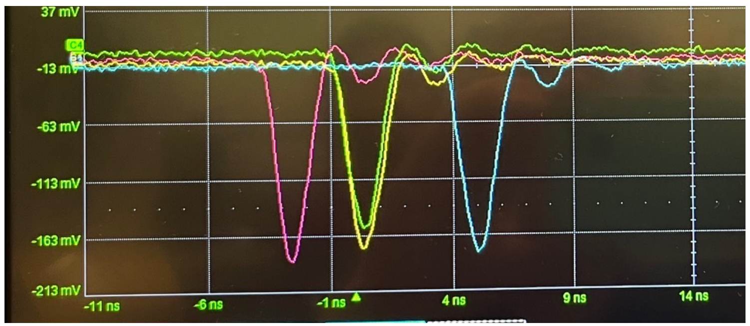


EICROC0 TZ Pre Amplifier Probe output signals

Pixel / Channel Mapping	Column 0	Column 1	Column 2	Column 3
Line 0	Pixel (**0**,0) **#00**	Pixel (**1**,0) **#04**	Pixel (**2**,0) **#08**	Pixel (**3**,0) **#12**
Line 1	Pixel (**0**,1) **#01**	Pixel (**1**,1) **#05**	Pixel (**2**,1) **#09**	Pixel (**3**,1) **#13**
Line 2	Pixel (**0**,2) **#02**	Pixel (**1**,2) **#06**	Pixel (**2**,2) **#10**	Pixel (**3**,2) **#14**
Line 3	Pixel (**0**,3) **#03**	Pixel (**1**,3) **#07**	Pixel (**2**,3) **#11**	Pixel (**3**,3) **#15**



PA output signals through SMA connector s (PCB back plane)



Feature of EICROC0 test board:

Observation of 4 Probe PA channels simultaneously

1 Probe PA per column

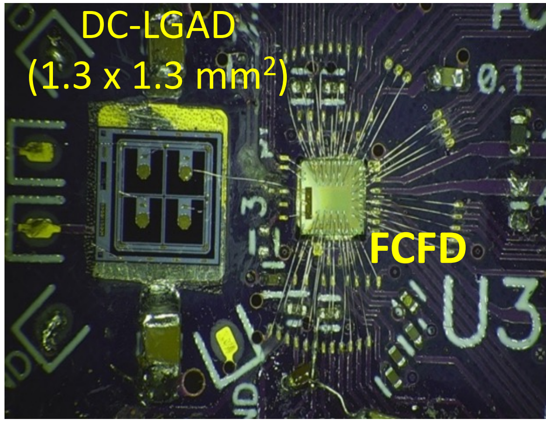
Ex.: #00, #04, #08, #12

FCFD: Forward Constant Fraction Discriminator

From Artur Apresyan (FermiLab)

Goals:

- Develop a robust fast-timing measurement technique for fast detector
- 30 ps time resolution or better
- easy to use & stable: no corrections, no calibration or threshold adjustement
- very low dead time after a hit (< 25 ns)



Methodology:

✸« A simulation model of front-end electronics for high precision timing measurements with LGAD », C. Peňa *et al.*, NIM A 940 (2019) 119.

⇨ CFD outperforms Leading edge Discriminators
for low amplitude signal (**preferred** for AC-LGAD charge sharing capability)

FCFI

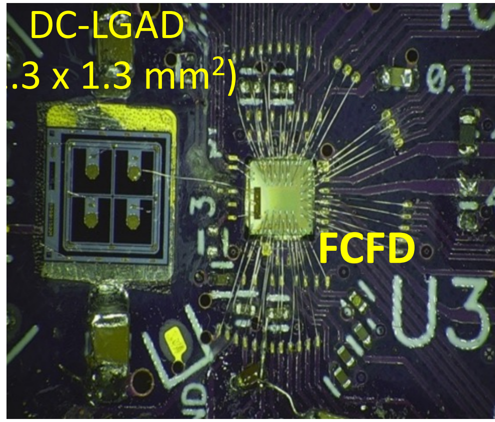
FCFDv0 (TSMC 65 nm CMOS technology)

1 single channel, only analog blocks to test CFD approach

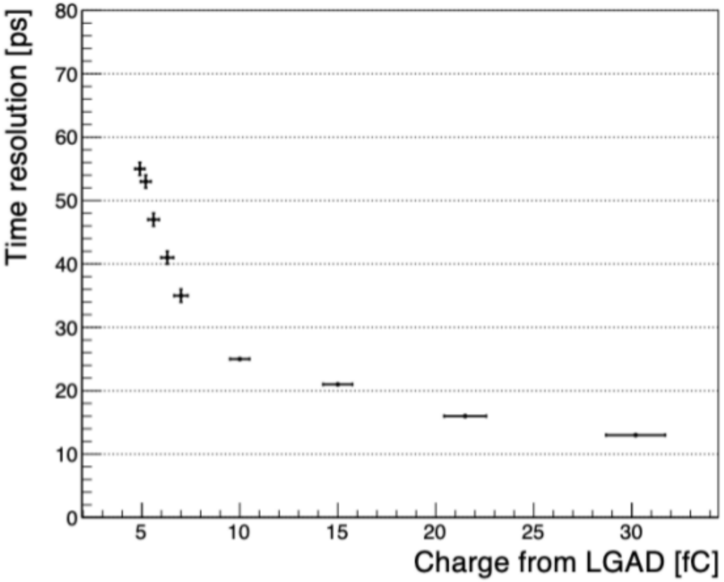
- Chip performance characterization with internal charge injection circuit
  Jitter: **~30 ps** (5 fC); < 10 ps (30 fC)
- + DC-LGAD (CMS-size pixel:1.3 x 1.3 mm^2) 1 # wire-bonded
  IR Laser, Beta source ⇨ confirmation of expected time resolution: **~30 ps**
- *measurements at test beam facility will follow*

From Artur Apresyan (FermiLab)

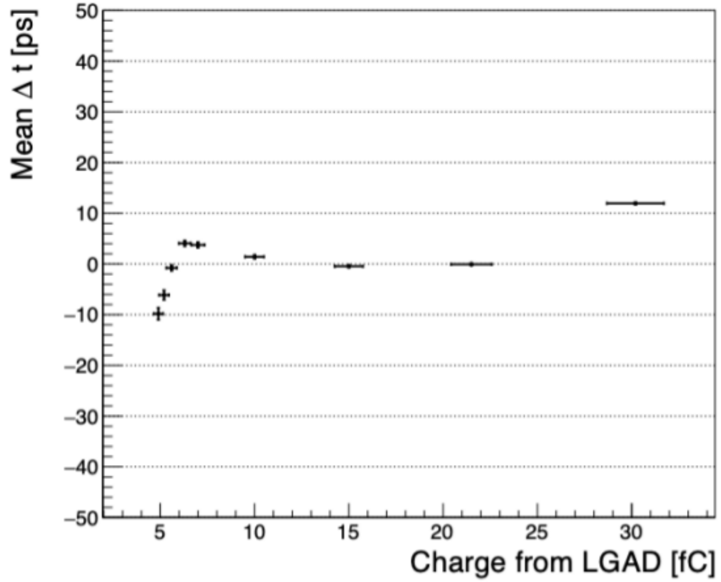
Timing ASIC with CFD FCFDv0



- Measurements with laser confirm the excellent intrinsic performance of the ASIC in time resolution and low jitter



Time resolution with 1.3x1.3 mm^2 LGAD sensor



Jitter with 1.3x1.3 mm^2 LGAD sensor

FCFD perspectives

From Artur Apresyan

✷**FCFDv1 (TSMC 65 nm CMOS technology): design finalized, expected delivery from TSMC summer 2023**
10 channels, analog blocks + ADC (charge measurement)
- optimized for EIC AC-LGAD strips (500 μm pitch, 1 cm length)
- development of associated PCB test board
- characterization: late summer '23 ->
- + AC-LGAD sensor < BNL

  IR Laser & Beta source: fall '23; Test beam: fall-winter '23

✷**FCFDv2 (TSMC 65 nm CMOS technology): design FY24, characterization FY25**
10 channels, + digital readout
- development of associated PCB test board
- + AC-LGAD sensor < BNL

  IR Laser, Beta source, Test beam

FCFD presentations at eRD112 meetings:

https://indico.bnl.gov/event/17999/ **(01/04/23)**
https://indico.bnl.gov/event/17084/ **(09/14/22)**
https://indico.bnl.gov/event/19471/ **(05/16/23)**

UCSC/SCIPP effort: 3rd party ASIC characterization

Objective: closely collaborating with 3rd party **institutions** and **companies** to **guide** ASIC developments **targetting EIC requirements** developing **PCB test boards** and performing **thorough characterization** (calibration ; laser, 90Sr source with LGAD wire-bonded) allowing for ASIC performance comparison

Lead institution	Name	Tech	Output	n channels	Funding
INFN Torino	FAST	110 nm CMOS	TDC	20	INFN
NALU Sci.	HPSoC	65 nm CMOS	Waveform	5 ($\geq$ 81 final)	DoE SBIR
Anadyne Inc.	ASROC	SiGe BiCMOS	Discrim.	16	DoE SBIR

Name	Specific goal	Status
FAST	Large cap TDC	Testing, new version soon
HPSoC	Max timing precision, digital back-end	Testing
ASROC	Max timing precision, low power	Simulations finalized, Layout board

- optimized (EIC) **HPSoC 4-ch prototype** *(High Pitch digitizer System on Chip):* tapeout expected summer '23
- **ASROC:** chip ready, waiting for delivery. Associated test board in fabrication
- **INFN FAST:** characterization of FAST-2 digital part; waiting for FAST-3 availability

SCIPP presentations at eRD112 meetings: https://indico.bnl.gov/event/17999/ (01/04/23)
https://indico.bnl.gov/event/16767/ (09/06/22)
https://indico.bnl.gov/event/19471/ (05/16/23)