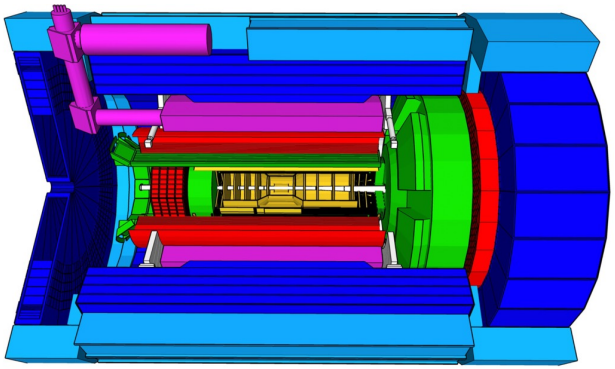
Istituto Nazionale di Fisica Nucleare

with eRD109 support



The dRICH RDO

P. Antonioli , D. Falchieri, G. Torromeo (INFN Bologna)
on behalf of the dRICH DSC

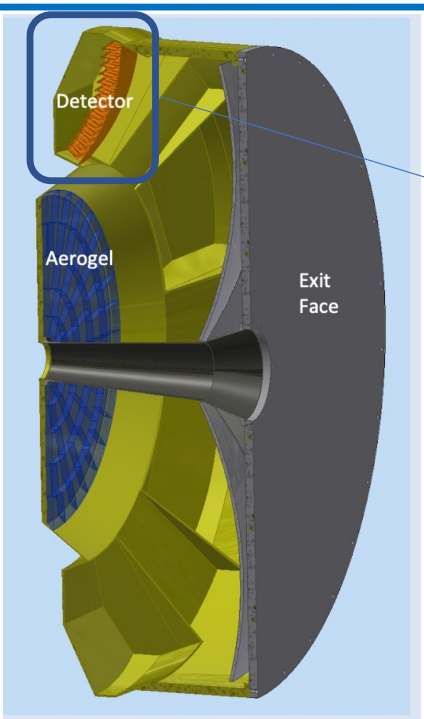
Incremental Preliminary Design and Safety Review
of the EIC Detector DAQ and Electronics // June 2024

Charges

Charges

1. Are the technical performance requirements appropriately defined and complete for this stage of the project?
2. Are the plans for the various detector electronics and data acquisition systems appropriately documented and complete for this stage of the project?
3. Are the current plans from front-end electronics to data acquisition for the detector likely to achieve the technical performance requirements, with a low risk for cost increases, schedule delays, and technical problems?
4. Are the schedule assumptions for the fabrication of the various electronics and data acquisition systems and assembly plans reasonable and consistent with the overall detector schedule?
5. Have ESH&Q and QA considerations been adequately incorporated into the plans at their present stage?

1. Technical performance requirements



dRICH RDOs… are **here** inside sector “detector box”

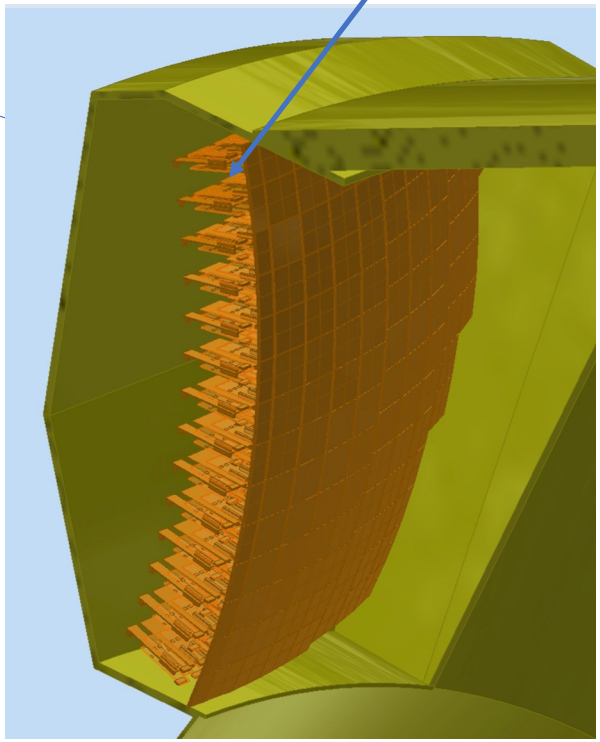
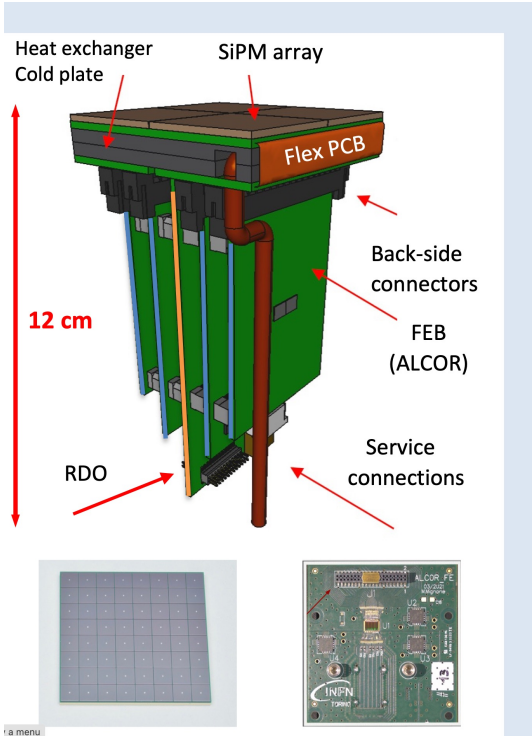


PHOTO DETECTOR UNIT (PDU)

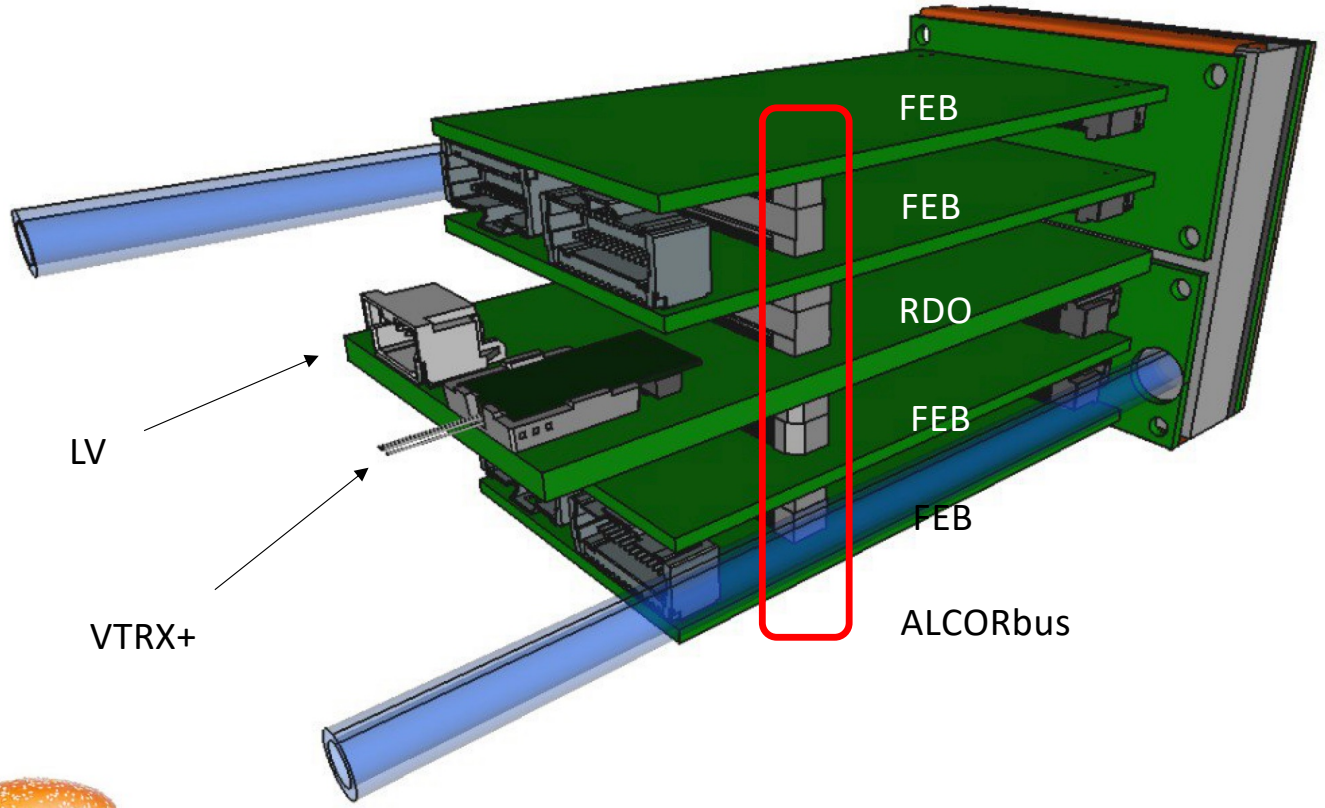


First RDO requirement is **space**: 40 x 90 mm area
RDO not accessible: **remote firmware upgrade** must be possible

requirements (2): interface with FEB

dRICH RDO must handle readout of dRICH ALCOR ASIC (see F. Cossio report)

In 4x9 cm2 the RDO must:
- provide interface with ePIC DAQ
- provide readout of 4 ALCOR v3 (64 channel each)



- The dRICH electronic - burger :

requirements (2): ALCORbus

- for each ALCOR64 (64 channels)
  - 8 DOUT signal (8 lanes per chip)
  - 1 CLKIN
  - 1 TP/SHUTTER
  - 1 RESET
  - 4 SPI

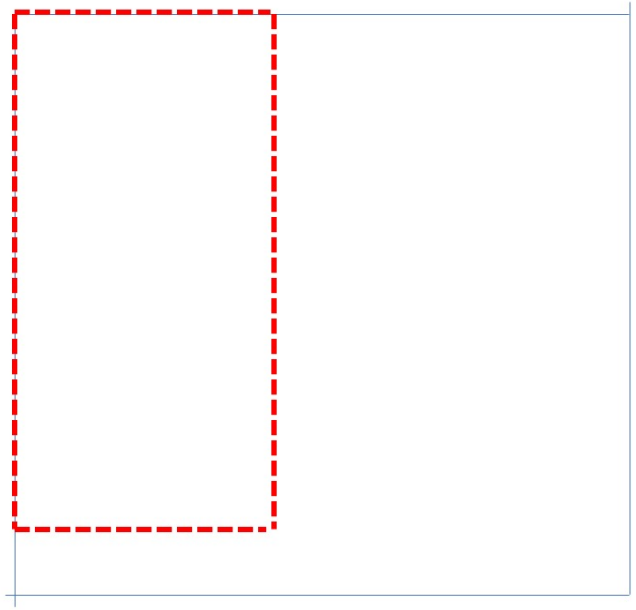
  } all differential pairs
- for each ALCOR Bus Connector (serving 2 ALCOR64)
  - 30 differential pairs
  - I/O requirements for FPGA: 120 pins devoted to ALCOR
- connectors toward 2 FEB must have 60 pins + 30 GND (“100” pin connector)
- candidate connector: Samtec ERF5-050-05.0-L-DV-K-TR

RDO FPGA need high speed (“high performance”) I/O pins to implement ALCOR bus (for TOP/BOTTOM FEB)

ALCOR v1 and v2 working at 320 MHz, tested already at 394 MHz
ALCOR v3 will work at 394 MHz (4 times EIC frequency)

RDO must implement clean clock multiplication by factor 4
RDO must reconstruct clock via optical link
RDO must produce clean clock (minimize jitter)

Optical link and RDO dimensions



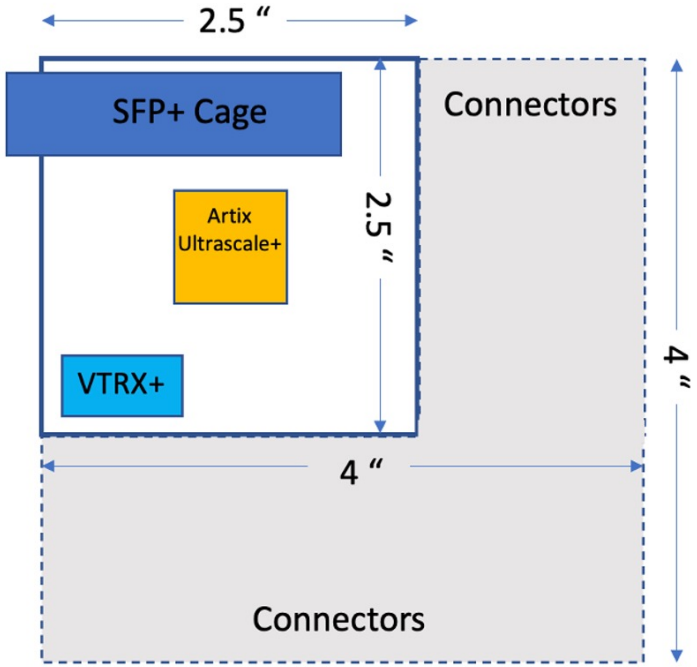


Table 1. Dimension Table for Drawing of SFP Transceiver

Designator	Dimension (mm)	Tolerance (mm)	Comments
A	13.7	± 0.1	Transceiver width, nosepiece or front that extends inside cage
B	8.6	± 0.1	Transceiver height, front, that extends inside cage
C	8.5	± 0.1	Transceiver height, rear
D	13.4	± 0.1	Transceiver width, rear
E	1.0	Maximum	Extension of front sides outside of cage, see Note 2 Figure 1B
F	2.3	Reference	Location of cage grounding springs from centerline, top
G	4.2	Reference	Location of side cage grounding springs from top
H	2.0	Maximum	Width of cage grounding springs
J	28.5	Minimum	Location of transition between nose piece and rear of transceiver
K	56.5	Reference	Transceiver overall length
L	1.1x45°	Minimum	Chamfer on bottom of housing
M	2.0	± 0.25	Height of rear shoulder from transceiver printed circuit board
N	2.25	± 0.1	Location of printed circuit board to bottom of transceiver
P	1.0	± 0.1	Thickness of printed circuit board
Q	9.2	± 0.1	Width of printed circuit board
R	0.7	Maximum	Width of skirt in rear of transceiver
S	45.0	± 0.2	Length from latch shoulder to rear of transceiver
T	34.6	± 0.3	Length from latch shoulder to bottom opening of transceiver
U	41.8	± 0.15	Length from latch shoulder to end of printed circuit board
V	2.5	± 0.05	Length from latch shoulder to shoulder of transceiver outside of cage (location of positive stop).
W	1.7	± 0.1	Clearance for actuator tines
X	9.0	Reference	Transceiver length extending outside of cage, see Note 2 Figure 1B
Y	2.0	Maximum	Maximum length of top and bottom of transceiver extending outside of cage, see Note 2 Figure 1B
Z	0.45	± 0.05	Height of latch boss
AA	8.6	Reference	Transceiver height, front, that extends inside cage
AB	2.6	Maximum	Length of latch boss (design optional)
AC	45°	± 3°	Entry angle of actuator
AD	0.3	Maximum	Radius on entry angle of actuator
AE	6.3	Reference	Width of cavity that contains the actuator
AF	2.6	± 0.05	Width of latch boss (design optional)
AG	0.40	Minimum	Maximum radius of front of latch boss, 2 places (design optional)

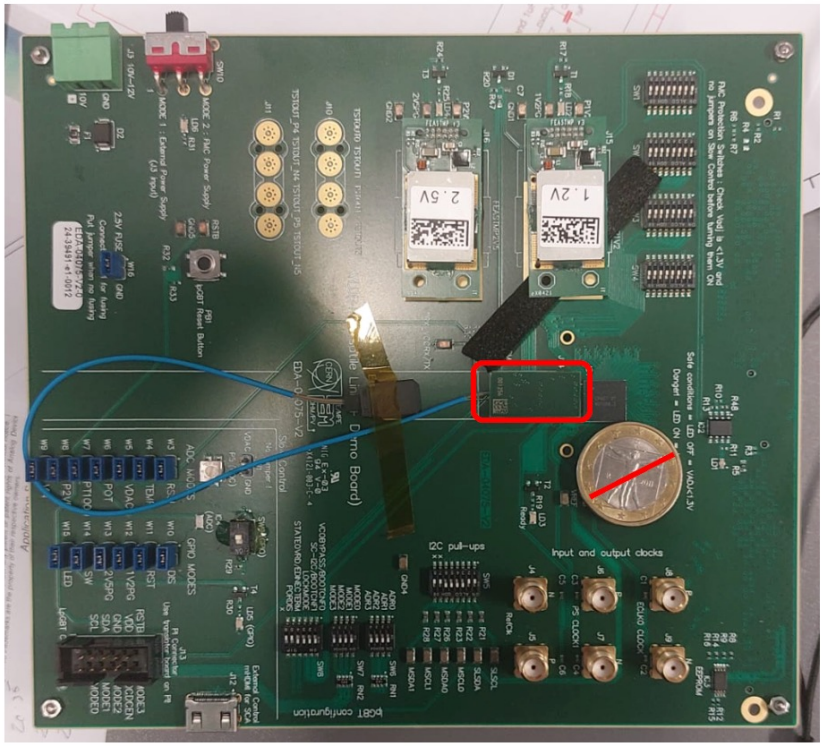
4” x 4 “ standard RDO

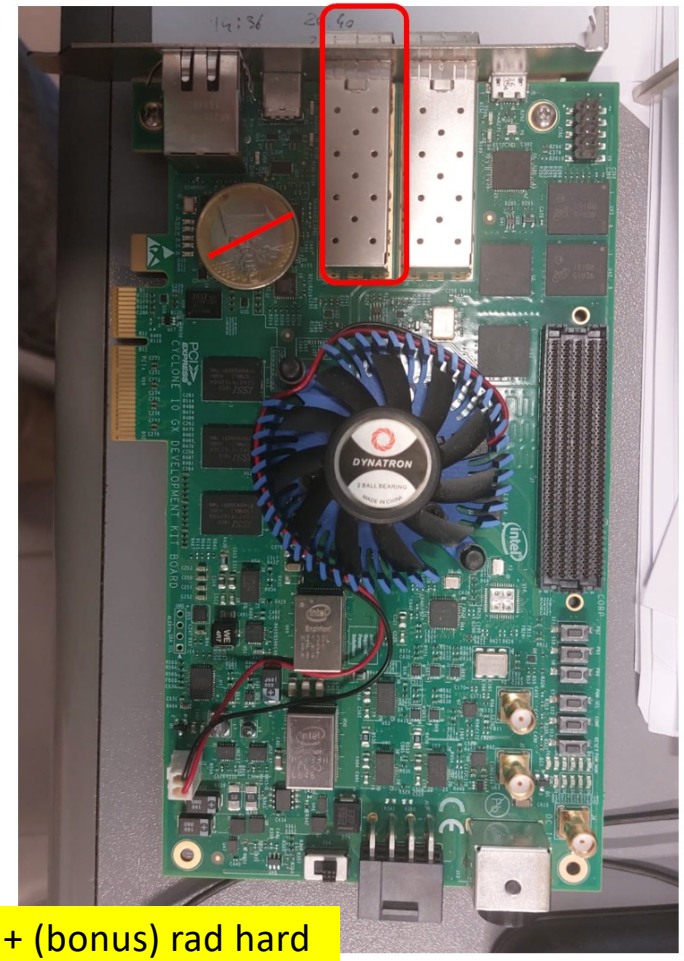
1.57” x 3.45” dRICH RDO

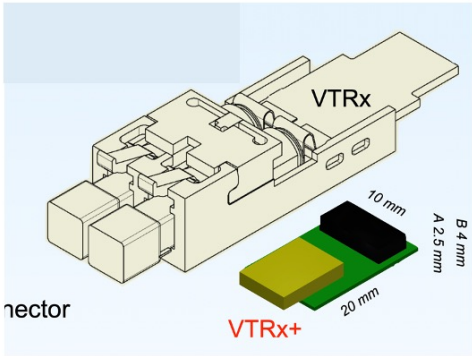
Obvious interest on trying to use a very compact optical link
1 SFP takes a lot of space!

VTRX+ and SFP comparison by images…

VLDB+ CERN card (VTRX+ “demo board”)

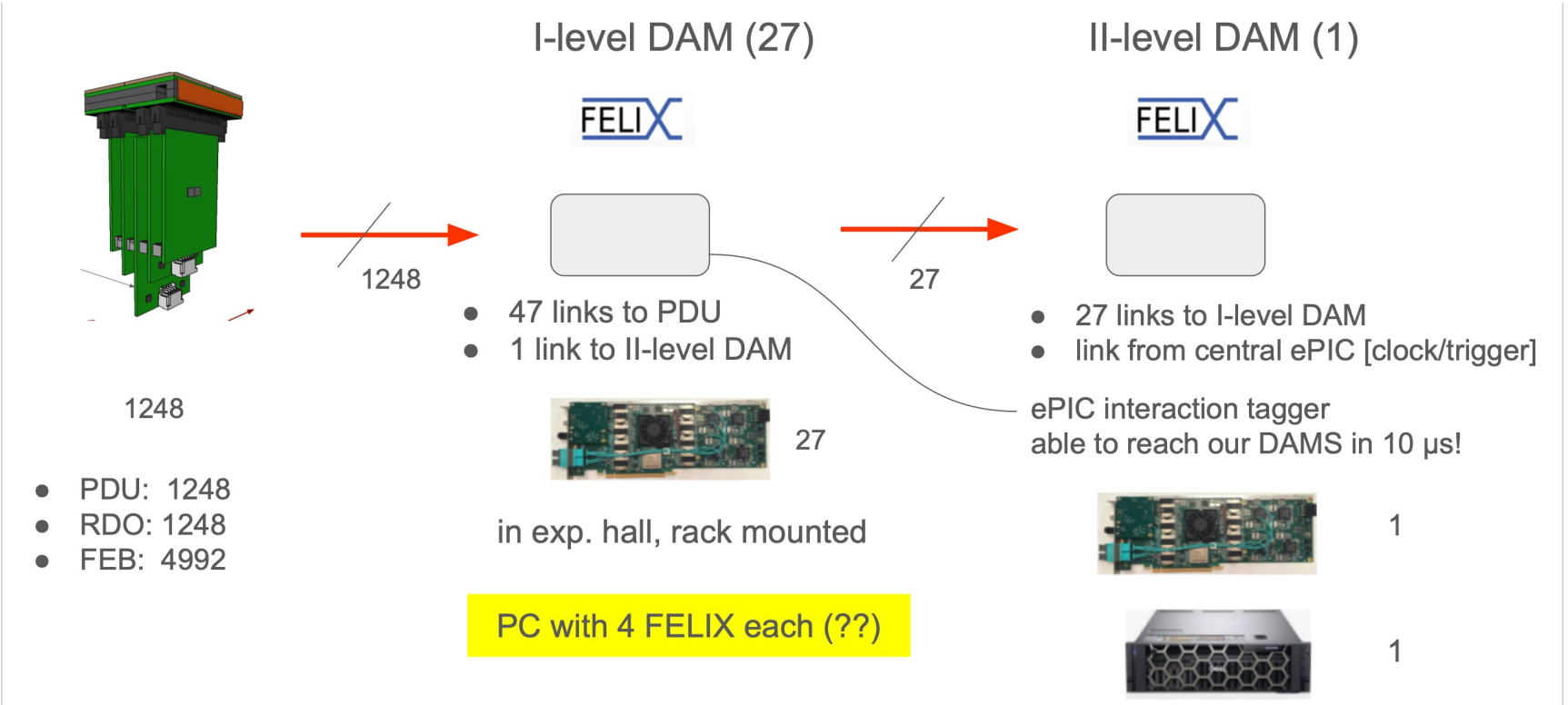






Identified VTRX+ as compact optical transceiver solution + (bonus) rad hard

Reminder: dRICH DAQ



requirement: DAQ throughput modeling

dRICH DAQ parameters	
RDO boards	1248
ALCOR64 x RDO	4
dRICH channels (total)	319488
Number of DAM L1	27
Input link in DAM L1	47
Output links in DAM L1	1
Number of DAM L2	1
Input link to DAM L2	27
Link bandwidth [Gb/s] (assumes VTRX+)	10
Interaction tagger reduction factor	200
Interaction tagger latency [s]	2,00E-03
EIC parameters	
EIC Clock [MHz]	98,522
Orbit efficiency (takes into account gap)	0,92

ALCOR parameters		Notes
Front end limit [kHz]	4000	
ALCOR Clock [MHz]	394,08	It will be 394.08 MHz or 295.55 MHz
Channels/serializer	8	
Bits per hit	64	2 32-bit words per hit (also TOT)
Bits per hit encoding 8/10	80	
Serializer band limit [Mb/s]	788,16	
Theoretical Serializer limit/ channel [kHz]	1231,5	this would be with 0 control words
Serializer limit single ch [kHz]	800	this is expected to improve with ALCOR v3
Number of serializer per chip	8	
Channel/chip	64	
Shutter width (ns)	2	

	Bandwidth analysis		Limit	Comments
INPUT	Sensor rate per channel [kHz]	300,00	4.000,00	
	Rate post-shutter [kHz]	55,20	800,00	
	Throughput to serializer [Mb/s]	34,50	788,16	
	Throughput from ALCOR64 [Mb/s]	276,00		limit FPGA dependent: with RDO prototype we will have something
	Throughput from RDO [Gb/s]	1,08	10,00	based on VTRX+
	Input at each DAM I [Gbps]	50,67	470,00	
	Buffering capacity at DAM I [MB]	12,97		to be checked but seems manageable
	Throughput from DAM I to DAM II [Gbps]	0,25	10,00	this might be higher (from FELIX to FELIX)
	Output to each DAM II [Gbps]	6,84	270,00	

Aggregated dRICH data		Comments	
Total input at DAM I [Gb/s]	1.368,14	This is only "inside" DAM, not to be transferred on PCI	1345,5
Total input at DAM II [Gb/s]	6,84	This is based on aggregation above + reduction factor of the interaction tagger	
Total output from DAM II [Gb/s]	6,84	Further reduction possible to be investigated (FPGA level?)	

detailed modeling of data throughput via:

ALCOR bus
FPGA
VTRX+ link
DAM (L1)
DAM (L2)

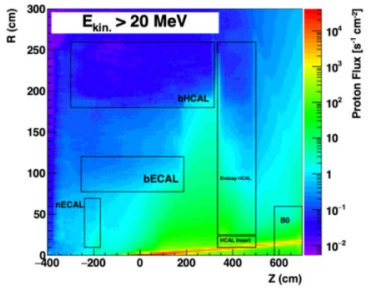
Note data bandwidth
on VTRX+ not an issue
(1 Gbps at maximum sensor rate)

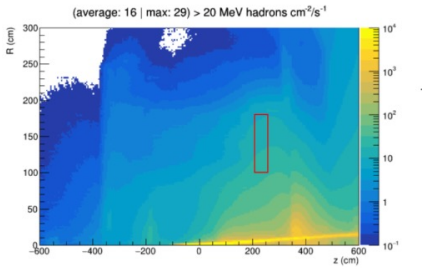
RDO FPGA requirement: able to implement optical link/Multigigabit transceiver up to 10 Gbps

other requirements:

radiation tolerance: moderately radiation hostile environment

dRICH flux (hadrons > 20 MeV): 20 $cm^{-2}s^{-1}$





TID: 0.2 krad after 10 years – not an issue

mechanisms of protection against SEU in particular must be in place in addition to TMR in key firmware registers etc.

power management:
- robust on board prevention of SEL must be implemented: current monitor / etc.
- possibility to act as power manager (via additional pins on ALCORbus) also on FEB cards

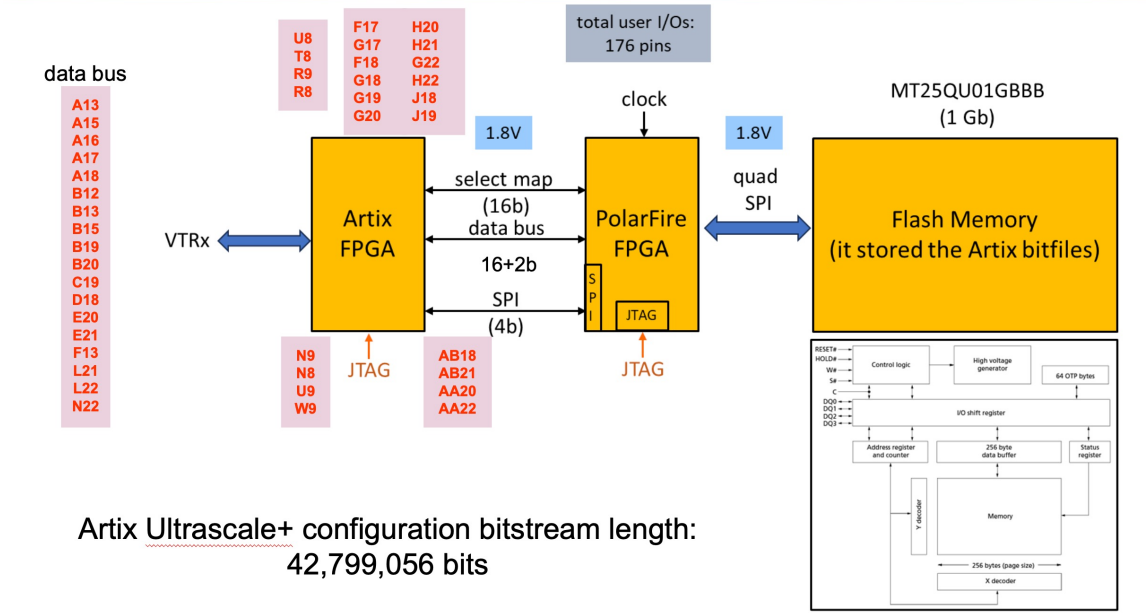
Implementation: main components

Component function	QTY	Baseline option/producer	V	Comments/hyperlinks to datasheets
uC power manager	1	ATtiny416	VDH	Watchdog on current monitor for RDO and FEB Datasheet
Main FPGA	1	Xilinx AU15P-SBVB484	0.85, 0.9, 1.2, 1.8 , 2.5	Artix Ultrascale+ Overview
Scrubber FPGA	1	Microchip MPF050T-FCSG325	1.0 1.2 1.8	Polarfire overview
QSPI Flash	1	MT25QU01	1.7 - 2.0 V	package W9 6x8 mm Datasheet
VTRX+	1	CERN	1.2V, 2.5V	https://edms.cern.ch/ui/file/2149674/1/VTRxPlusApplicationNote.pdf
ALCORbus connector	2	Samtec ERF5-050-05.0-L-DV-K-TR	N/A	
LDO	2	LTM4709	VDH VDL	6x12 mm Datasheet link, Demo board link
Step-Up Charge Pump	1	LTC3203	VDH	Provides VBIAS to LDO from VDH Datasheet
Temperature sensors	2	TMP119NAIDRVT	2.5	Close to LDO and VTRX datasheet
Clock multiplier/ jitter cleaner	1	SkyWorks SI5326	1.8 or 2.5 V	6x6 mm, 2 input - 2 output Family Datasheet and Si5326 Datasheet
3OT Crystal for Si5236	1	Abracon ABM8 -114_255MHZ-D2X-T	N/A	3.2 x 2.5 mm SkyWorks guidance
Crystal oscillator	1	SkyWorks 511JCA40N0000BAG	1.8	A 40 MHz crystal + an additional one for VTRx

Implementation: FPGA choice(s)

- Artix Ultrascale+ architecture guarantees high speed, I/O MTG implementation, clock reconstruction
- Artix Ultrascale+ AU15P-SBVB484 (see backup) good compromise between physical size 1.9x1.9 cm^2, resources (5.1 Mb RAM), I/O pins (204)
- Polarfire architecture (Flash based) used for scrubbing to cope with SEU on Artix configuration bits
- Smallest available Polarfire (MPF050T) as rad-tolerant scrubber seems effective choice. Add extra-resources

FPGAs - FLASH memory configuration scheme

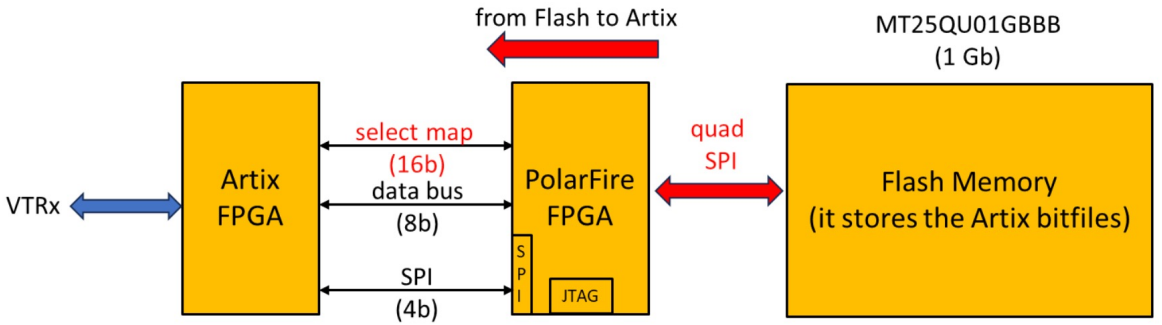


Artix Ultrascale+ configuration bitstream length:
42,799,056 bits

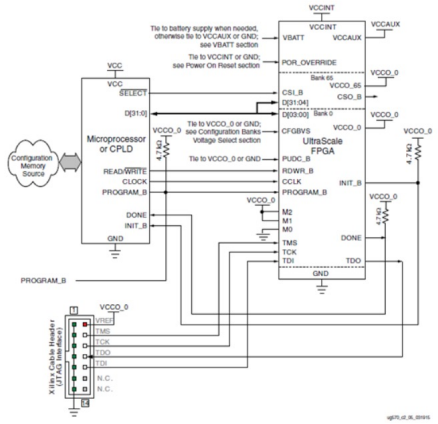
Implementation: remote programming

FPGAs - Artix programming from Flash

Step 1: Artix Ultrascale+ programming from Flash

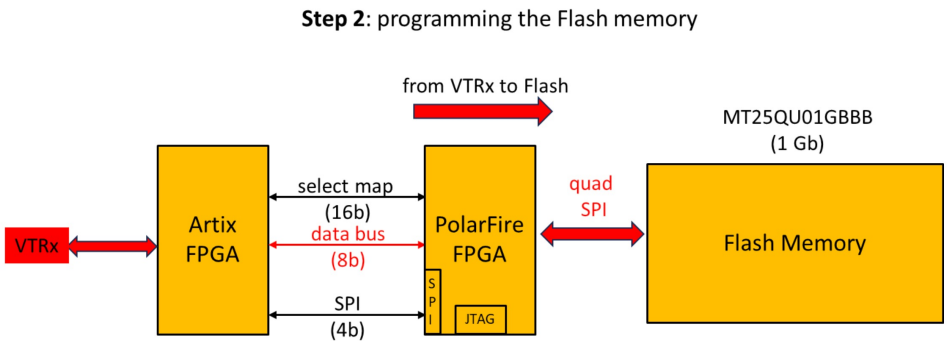


from Xilinx ug570

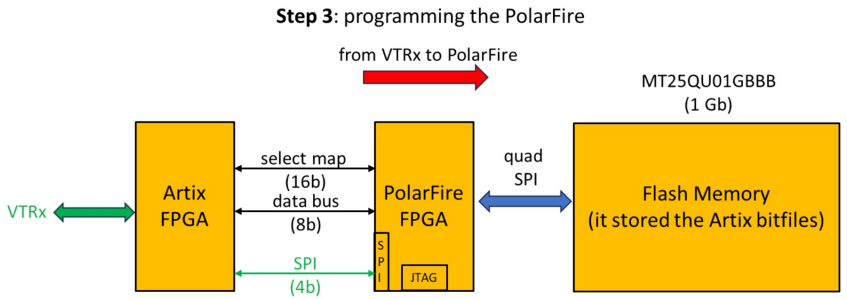


Implementation: remote programming

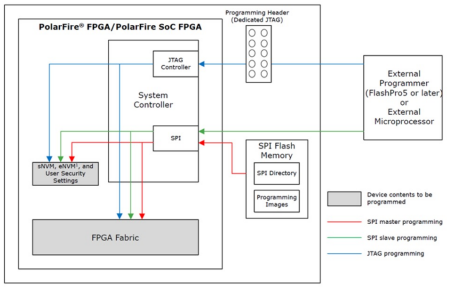
FPGAs - FLASH programming



FPGAs - Polarfire remote programming



from "PolarFire and PolarFire SoC FPGA programming User guide"



Implementation: radiation tolerance issues

Xilinx declares 2.67 × 10^{-16} cm^2/bit cross-section for CRAM bits
AUP15 has 42.8 × 10^{+6} configuration bits
dRICH flux (hadrons > 20 MeV): 20 $cm^{-2}s^{-1}$

1 SEU every 4.3x10^6 s/FPGA

↓

1 SEU every 3.5x10^3s/dRICH

↓

1 SEU every hour in whole dRICH

Main references:

https://docs.xilinx.com/r/en-US/ug116/SEU-and-Soft-Error-Rate-Measurements
A. Scialdone, "FPGA qualification for the LHC radiation environment" ,
Master Thesis, Politecnico di Torino -→ results on PolarFIre and NanoXplore

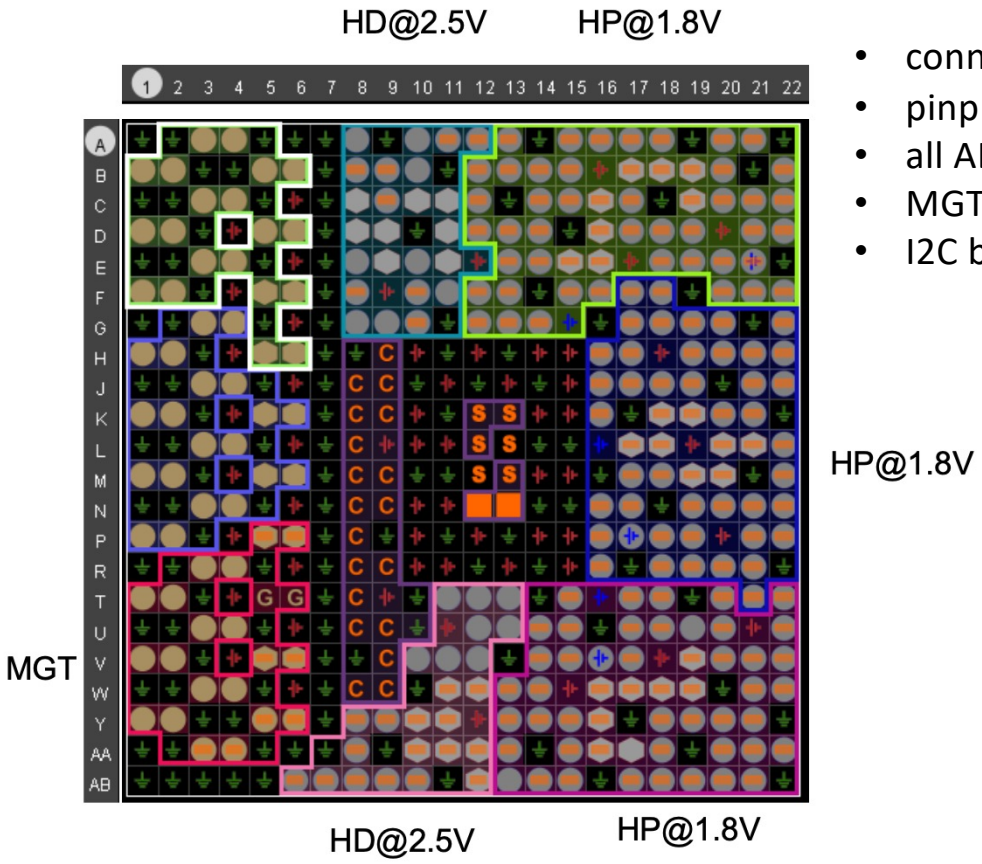
Strategy

- select as much as possible components already tested in radiation
- key PLL on separate IC (not on FPGA)
- radiation tests in December 2024 (Protontherapy Center Trento, O(100) MeV proton line
- test selectively different components. if needed second round in 2025
- possibility to implement "radiation monitor" on Polarfire (as ALICE TPC Readout Board in RUN2 with Microsemi FPGA)

Expertise

- the core team has experience on design to protect against SEL
- scrabber technique used in ALICE (in contact with INFN-PD, the expert P. Giubilato is an ePIC member too

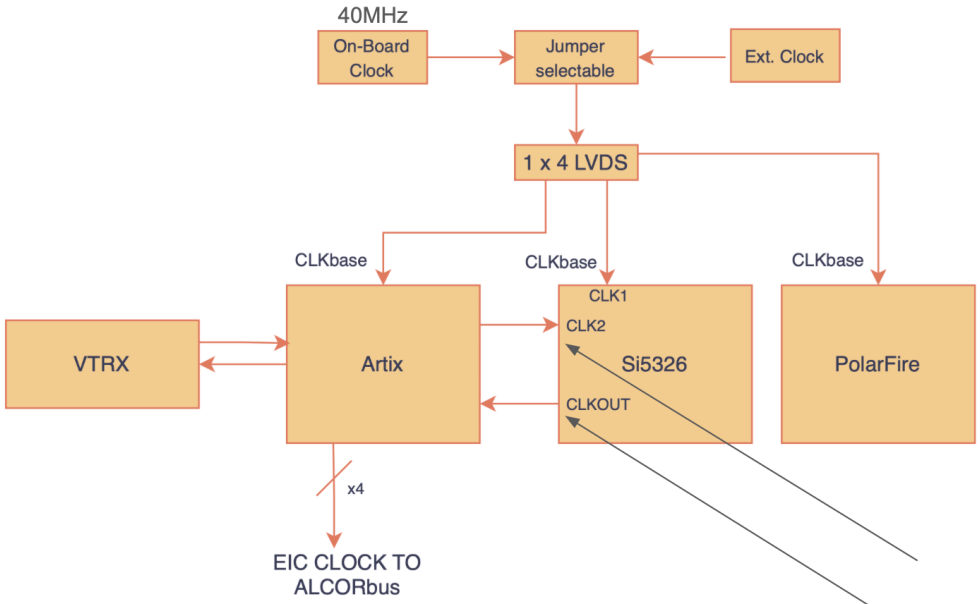
Implementation: Artix pinplan



- connections assigned on all pins (ALCORbus/vs Polarfire/I2C branches)
- pinplan – firmware verification on-going
- all ALCORbus I/O managed on HP blocks
- MGT section for VTRX+
- I2C branches designed (T sensors, jitter cleaner, etc.)

Still a few pins available: 23@HDs + 3@HPs

Implementation: clock management



Ext. clock used for sync during test beams when EIC clock not yet available from VTRx link

CLKbase (from on-board clock or ext. clock) is clock source for PolarFire.

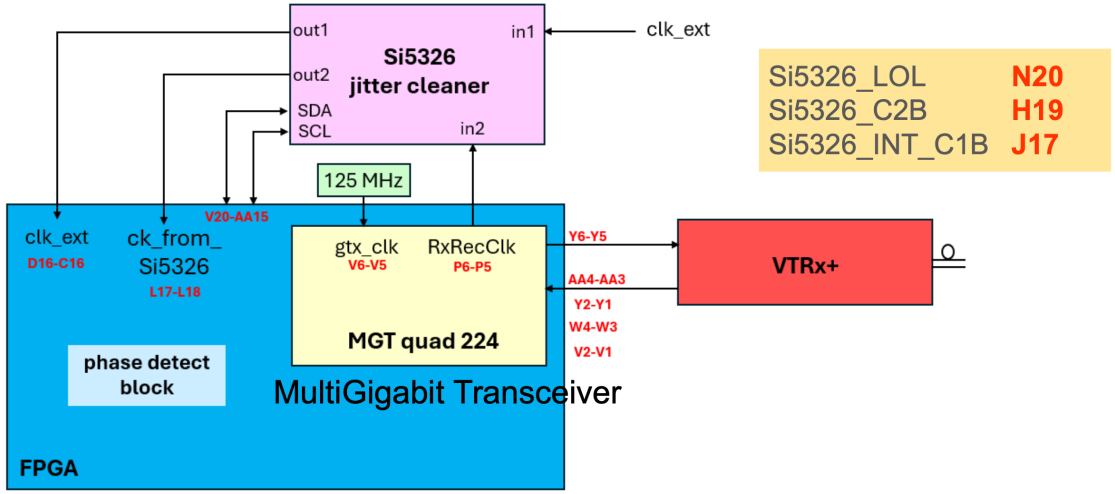
Artix-Polarfire-Flash bus works with this clock. This ensures Artix programming at boot, even if VTRx link is down.

reconstructed EIC clock from VTRx @ 98.5 MHz

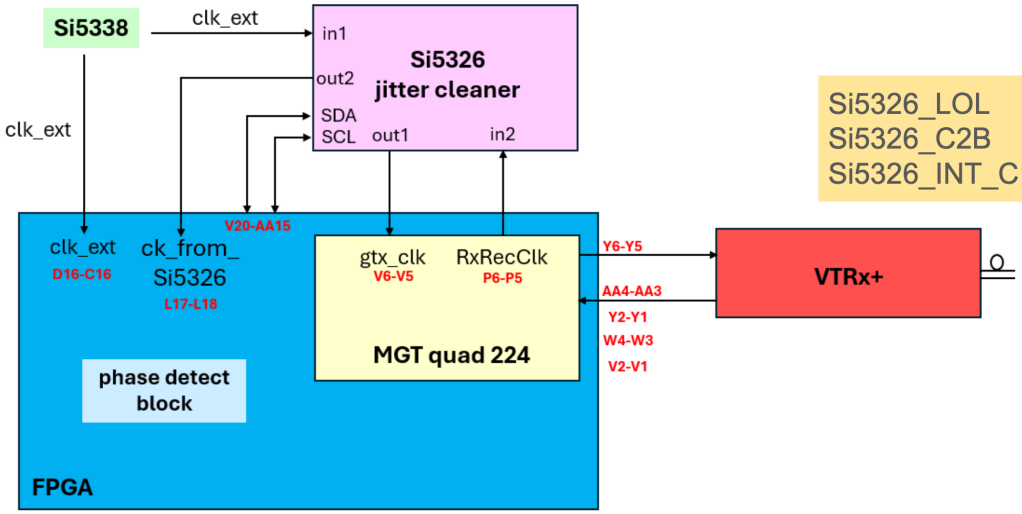
jitter cleaned + x4 EIC cloc at 398 MHz. Phase can be adjusted via Si5326

All clock signals (single-arrow) are differential pairs

Implementation: VTRX+ connection/clock



Si5326_LOL	N20
Si5326_C2B	H19
Si5326_INT_C1B	J17

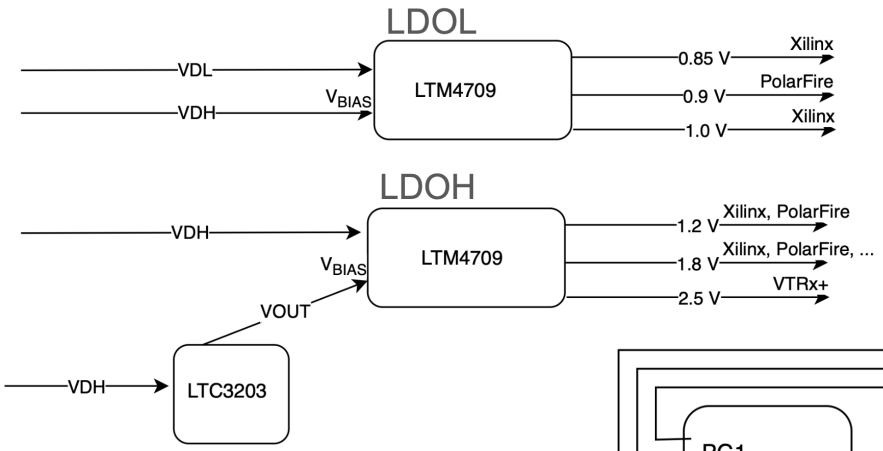


Si5326_LOL	N20
Si5326_C2B	H19
Si5326_INT_C1B	J17

- still discussing two alternatives for the clock to be connected to MGT block of Artix
- feedback from review panel is welcome

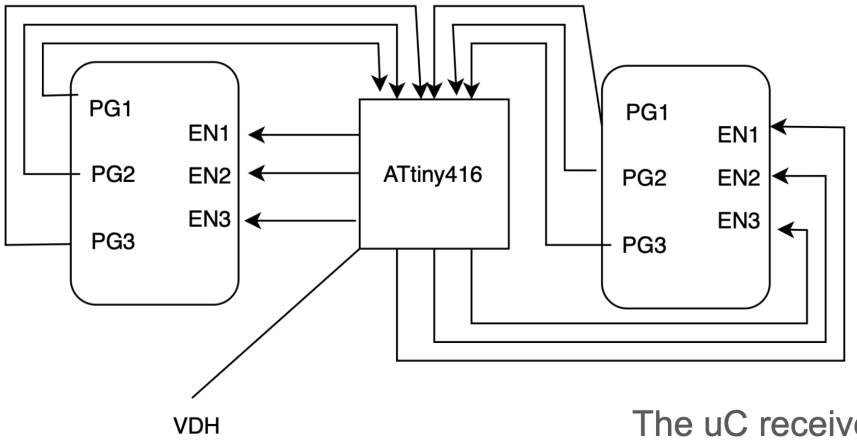
Implementation: power management

VDH: the high primary digital V: 2.7 V
VDL: the low primary digital V: 1.4 V
VOUT needs to be 3.7 V



LTC3203 https://www.analog.com/en/products/ltc3203.html

- Low-drop + compact LDO selected
- The selected LDO provides built-in current monitor, monitored by a uC.
- This mechanism ensures correct power-up sequencing + watchdog on SEL



The uC receives the current monitors from the two LDOs and protect against SEL

ATtiny416:
Product Selection Guide
Datasheet

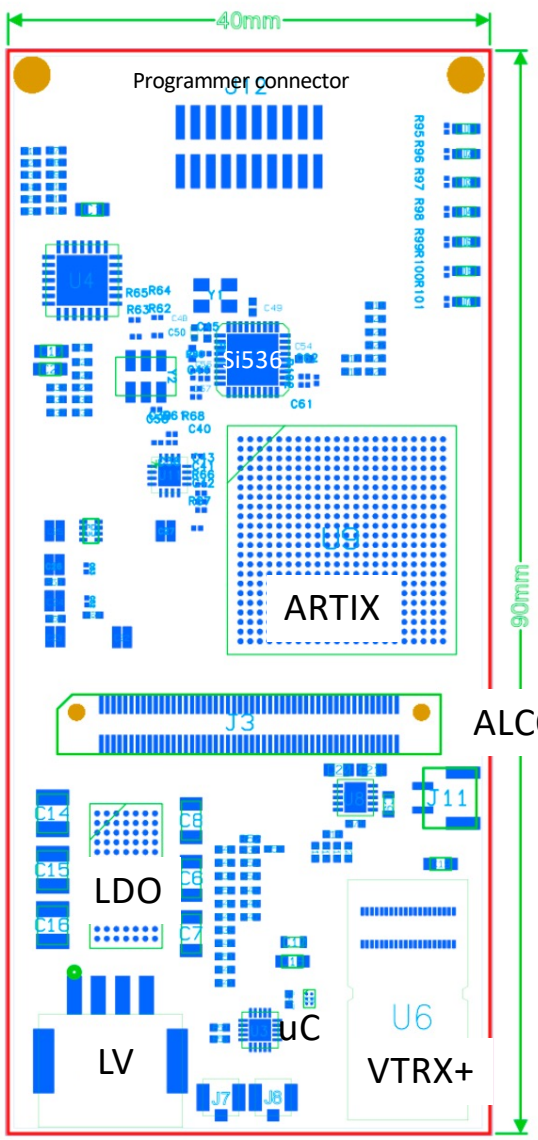
Implementation

- all components in schematics
- schematics in advanced state, all connections on-going
- pre-placement done

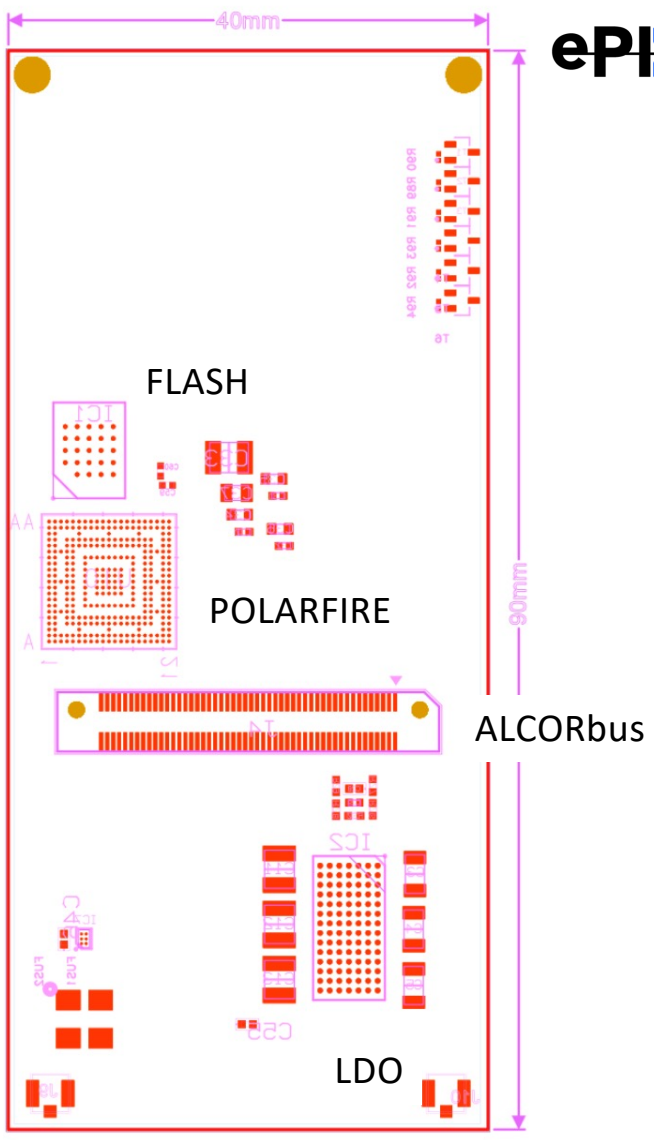
Next steps:

- several details to be still worked out
- integration verification with FEB team (INFN-TO) and PDU coordination (INFN-BO) by June
- layout and production to external company → Summer 2024
- Fall 2024:

a) first basic firmware
b) radiation tests (Dec. 2024)



TOP



BOTTOM

ESH & QA plans

- RDO PCB to be produced RoHS compliant
- RDO will be produced by an external company. We will externalize basic QA as much as possible at production level (ex. JTAG boundary scan check, uC and first firmware programming, power on test…). RX analysis for BGA connections requetsed as part of the tender
- RDO tests and validation before installation in PDU will be done in INFN Bologna
- As described, RDO has built-in protection for overcurrent + fuse on LV input
- Safety norms in INFN Laboratories in Bologna (obviously following EU and Italian laws) are available here
- Test procedure (three main steps envisaged at the moment):
    1. power-on, firmware installation, VTRX+ installation, test of optical link communication (via a FPGA evaluation board mimicking FELIX connection), clock reconstruction test, check of remote programming, Flash memory etc.
    2. connections on ALCORbus are operating correctly (special test board card will be developed)
    3. RDO is then passed to the PDU assembly line. Test 1/2 repeated with the 4 FEB of the PDU as part PDU validation

(further tests on PDU assembly/detector box and their handling out of scope of this review)

Reference documentation, test protocols and special cards for testbenches will be developed in 2026

Schedule

At current timeline (i.e. detector ready by June 2030 that is likely to be postponed given CD-3 shift)

2024: production of 10 RDO prototypes (on-going), first qualitication, radiation tests
2025: firmware development / use of RDO in lab and test beams for dRICH prototype readout
2025: pre-production of 10 RDO rev. 2, additional radiation tests as needed
2026: tendering and production award, start of vendor effort [production: 1248+20% spares → 1500]
2026: development of testbenches / production test protocols
2027-2029: -- QA testing (RDO) and assembly of PDU/detector boxes
-- [note VTRX+ mounting on cards happens in this phase]
2029-2030: shipping to BNL (as part of detector boxes shipping)

components:

- VTRX+ : see presentation, will be delivered end of 2026 by CERN
- we might opt for separate procurement of FPGA components in 2025
- other components part of the tender/card production

- components have been selected not in obsolence and we don't expect availability problems within production time. We might buy extra spares of FPGAs (in addition to 20% spares quota) to keep in case of need of extra production in the '30s when they will be clearly out of market

RDO core team @ INFN-BO: P. Antonioli, D. Falchieri, G. Torromeo (physicist, electronic engineer, electronic technician)

Summary

- dRICH RDO requirements identified
- dRICH RDO implementation (design) addresses requirements
- dRICH RDO prototypes available in 2024
- dRICH RDO design choices will be intensively tested in 2025 (with iteration as needed)
- dRICH RDO procurement, production and QA scheduled according to official EIC schedule