The ALCOR ASIC for the dRICH Detector

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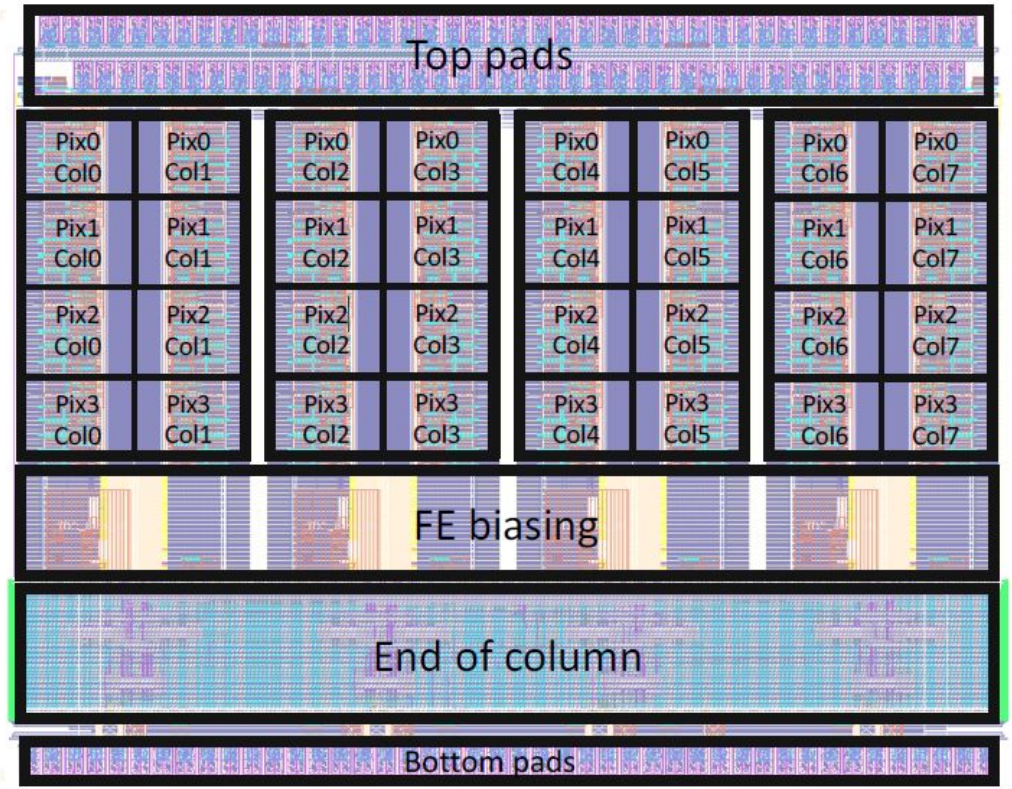
on behalf of the dRICH Collaboration

Incremental Preliminary Design and Safety Review of the
EIC Detector DAQ and Electronics - 31 May 2024

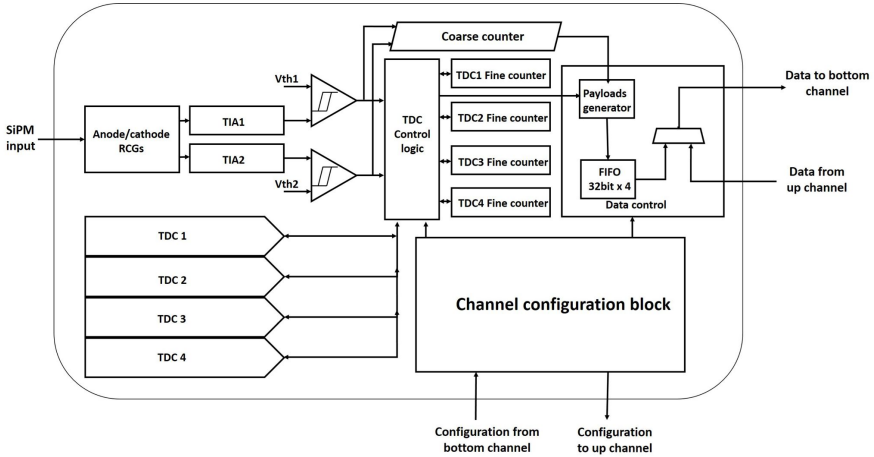
ALCOR (**A** **L**ow Power **C**hip for **O**ptical Sensor **R**eadout)

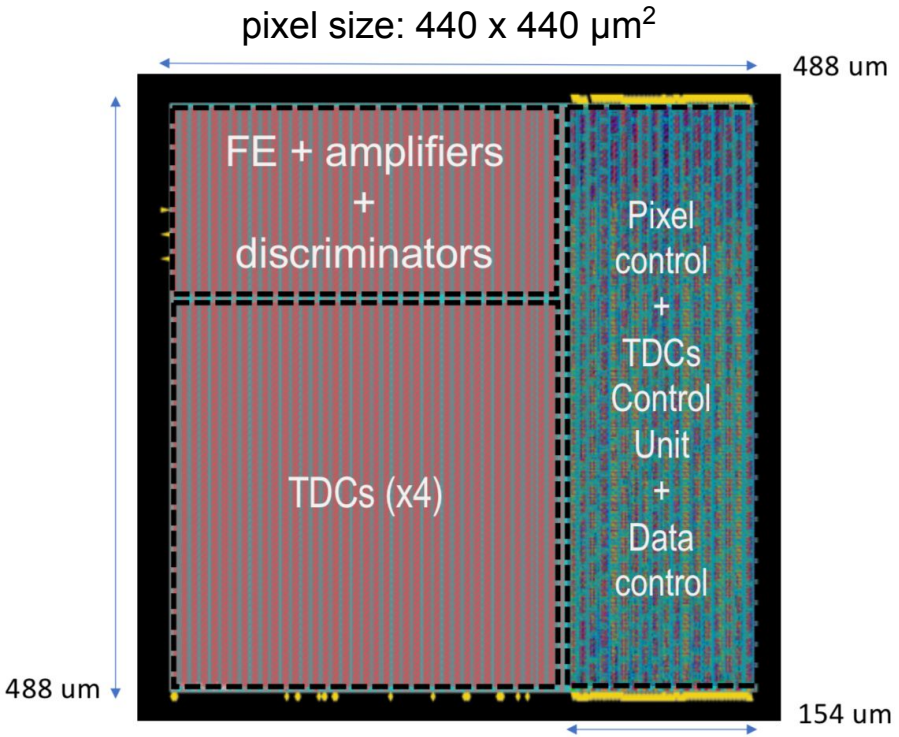
ASIC developed for the readout of the EIC dRICH SiPM sensors

- **32-pixel** matrix (8x4) mixed-signal ASIC (4.95 mm × 3.78 mm)
- **SiPM readout**: single-photon time tagging + Time-over-Threshold or Slew-Rate measurements
- On-chip signal amplification, conditioning and digitization, 32-bit event word
- **Fully digital output**: 4 LVDS 320 MHz DDR Tx links
- Power consumption ~10 mW/channel
- 0.11 µm CMOS technology



Pixel architecture





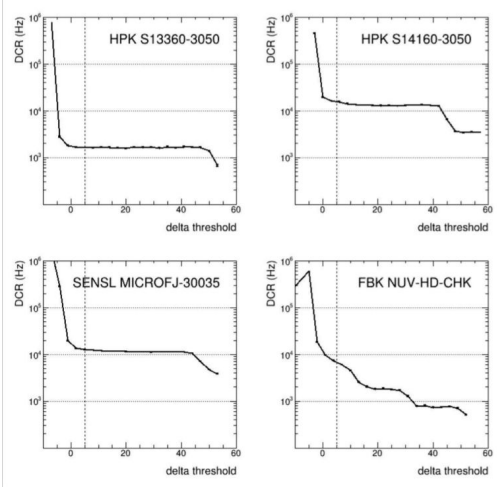
- RCG input stage current conveyor
- 2 independent TIA branches with 4 gain settings
- 2 leading edge discriminators with independent (and per pixel) threshold settings (6-bit DAC)
- 4 TDCs based on analogue interpolation with 25-50 ps time-bin (at 320 MHz clock frequency)
- Pixel control logic handles TDC operation, pixel configuration and data transmission

ALCOR v1

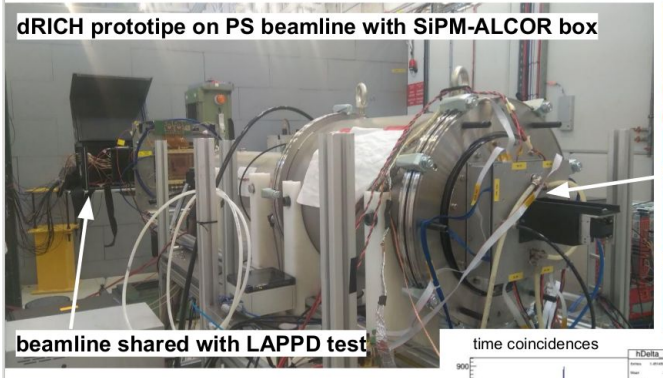
Developed by INFN for the readout of SiPMs at 77K, in the framework of Darkside (Dec 2019)

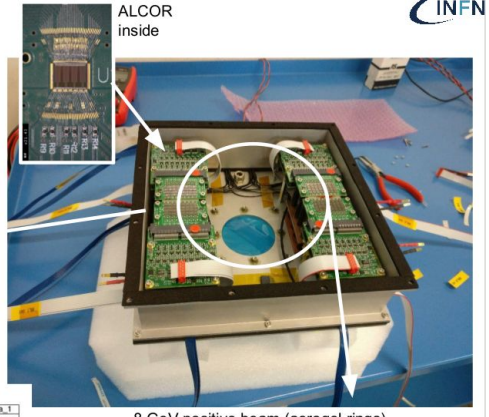
- Pixel matrix layout to explore solutions towards the development of an active silicon interposer for the integration of large area SiPMs for future massive frontier LAr Dark Matter Experiments (3D a-SiPM ”digital tile”)

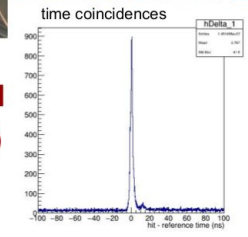
Extensively used within the EIC dRICH Collaboration during 2021-2022

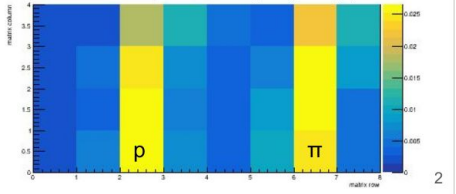


2022 test beam at CERN-PS









successful operation of SiPM irradiated (with protons up to 10^{10}) and annealed (in oven at 150 C)

ALCOR v2

ALCOR v2

- MPW, submitted in Dec 2022
- 60 chips, received in June 2023
- Includes new features targeted for EIC dRICH and bug fixes:
  - ✓ TDC logic critical error at high rates solved also for DCR rate at room temperature
  - ✓ New FE gain settings more suited for single photon applications
  - ✓ On-chip test-pulse also for EIC SiPM polarity
- Successfully validated in 2023 beam test

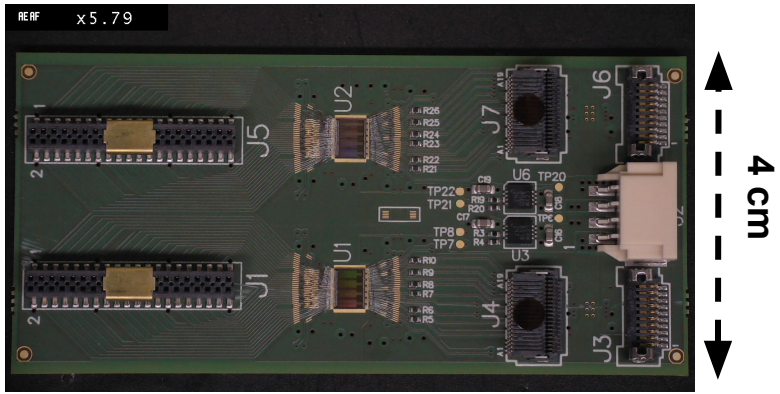
ALCOR v2.1

- INFN internal engineering run
- Submitted in Mar 2023, wafers delivered,
- Include small bug fixes w.r.t. v2
- Very high number of chips available to increase instrumented area for dRICH prototype and assemble other test setups
- Currently used in a beam test to validate ALCOR-based dRICH readout and evaluate its performance

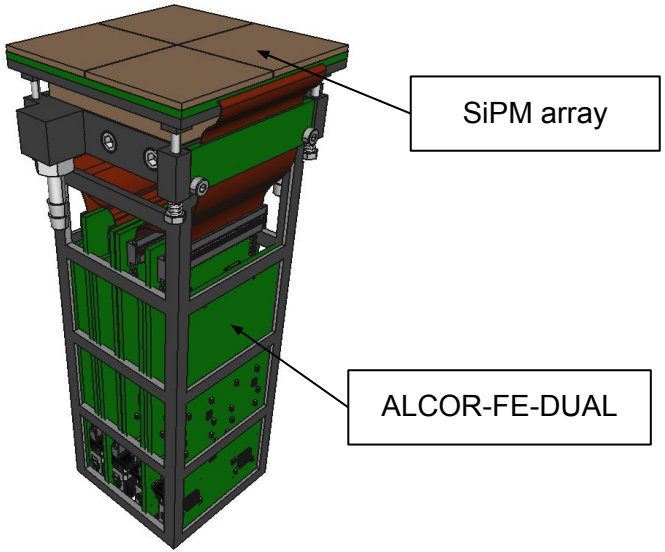
ALCOR dRICH prototype readout system

ALCOR-FE-DUAL

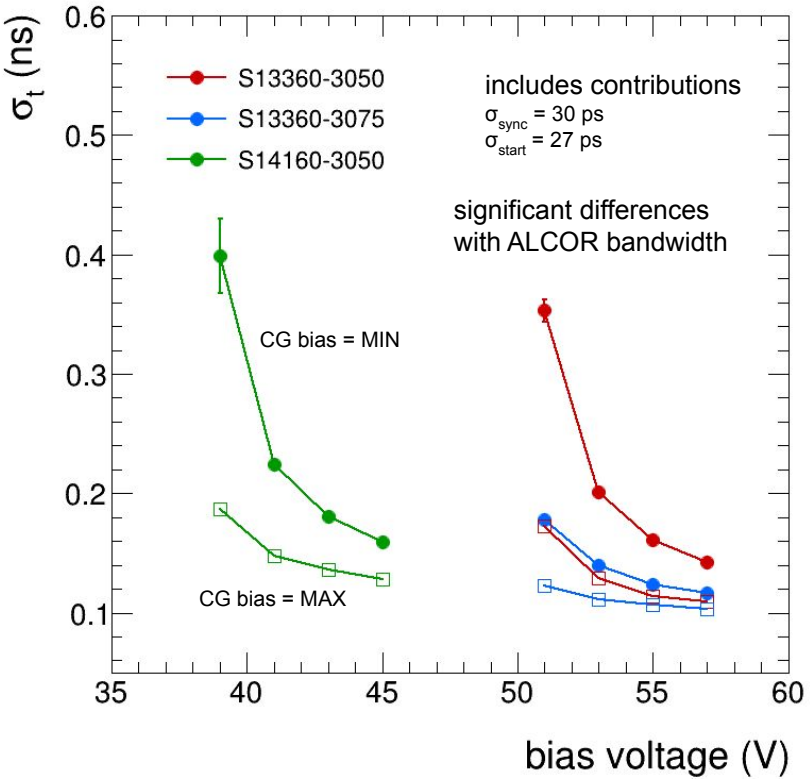
- Two **32-channel** ALCOR ASICs **wire-bonded** on the PCB
- 4 ALCOR-FE-DUAL boards for each PDU (256 channels)
- System used for 2023-2024 ePIC dRICH beam tests

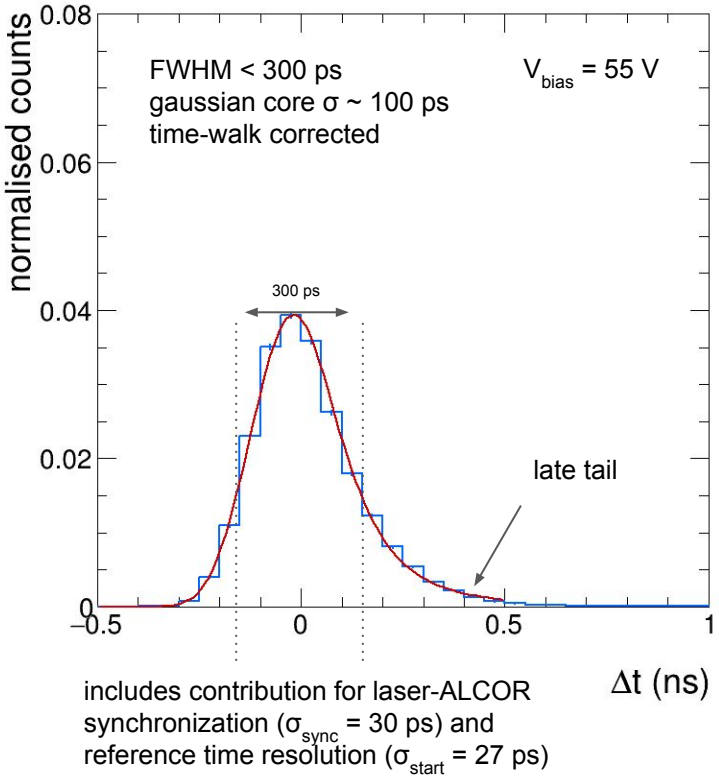


ePIC dRICH Prototype photodetector unit (PDU)



Laser timing measurements



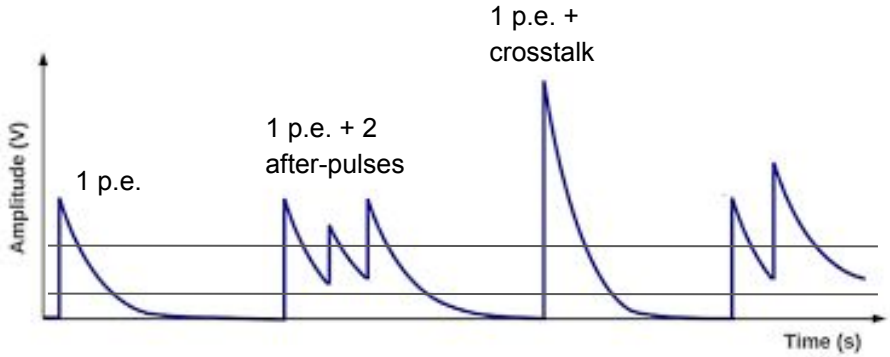


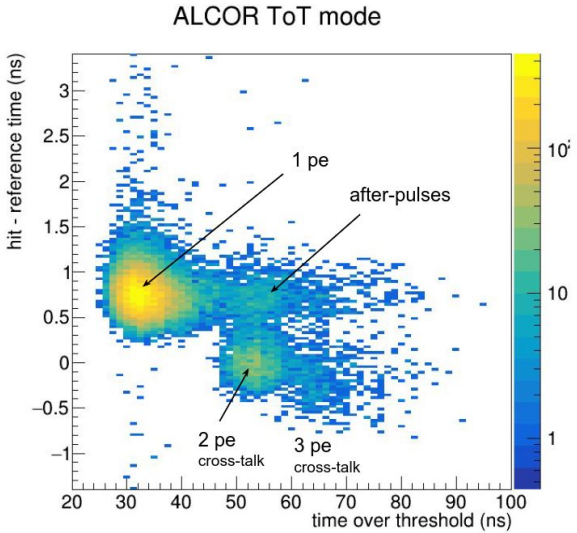
➔ Better time resolution with 75 µm SPADs

➔ Comfortably below σ_t = 150 ps also at low Vbias

Time walk correction

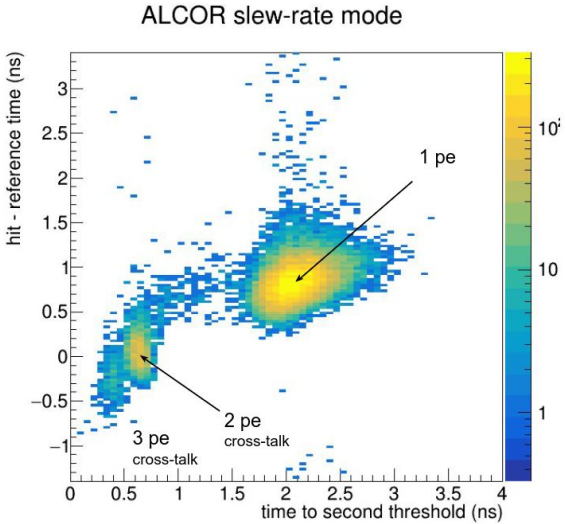
Time walk correction to improve overall time resolution → studies with laser setup using ***ToT*** and ***SlewRate*** measurements





✗ ***ToT mode*** cannot distinguish between afterpulses (slow-rise time, large ToT) and cross-talk (fast rise-time, large ToT)

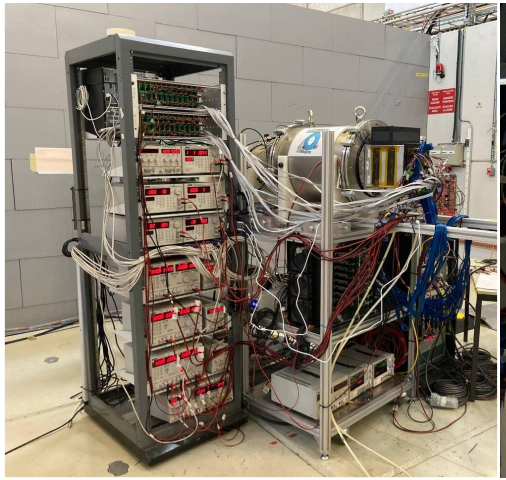
✓ ***SR mode*** provides better separation

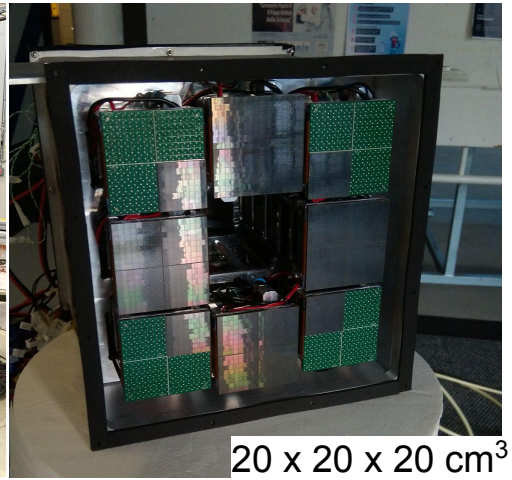


2023 test beam at CERN-PS

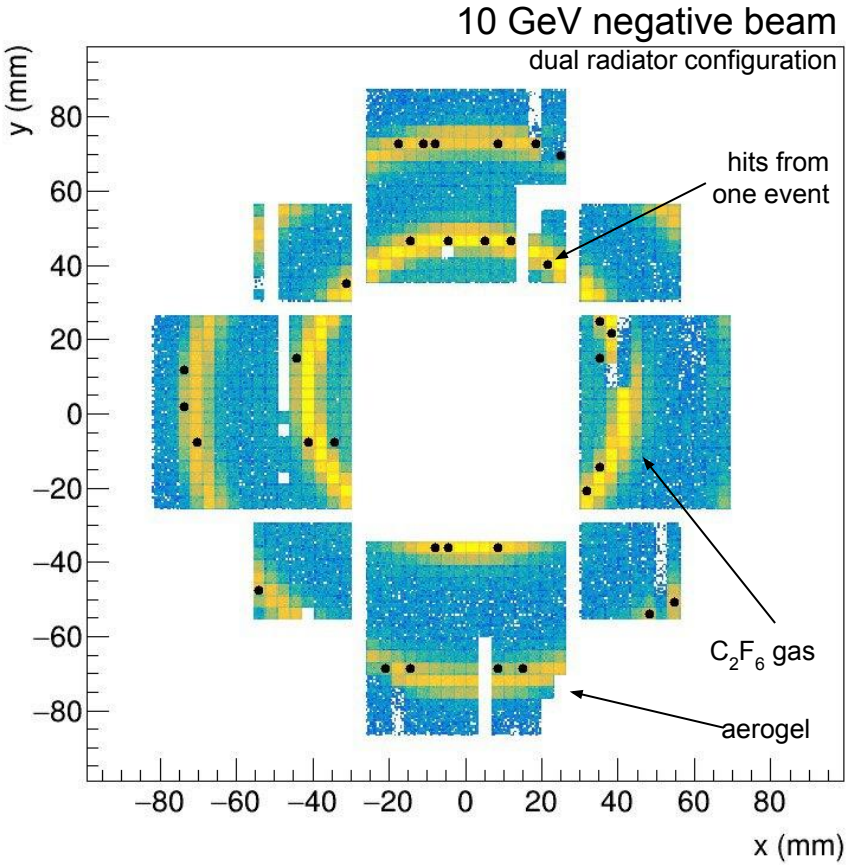
Successful beam test with prototype dRICH and PDUs (CERN-PS, October 2023)

- HPK S13360-3050 (3x3 mm^2, T = -30/-40°C)
- 20 FE-DUAL (40 ALCOR v2.0, 1280 channels)
- DAQ: Xilinx Kintex 7 KC705

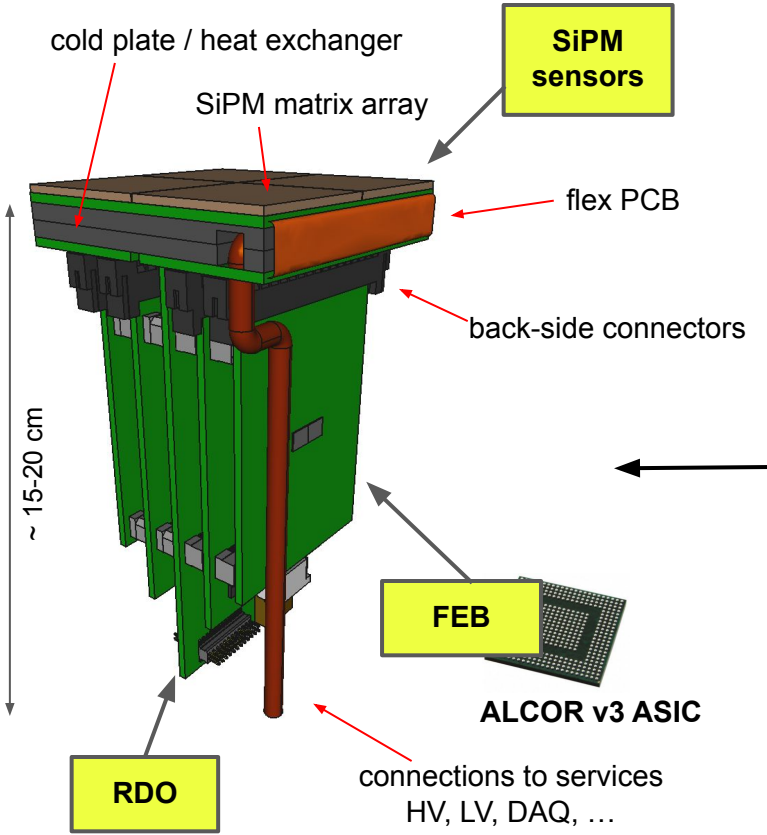




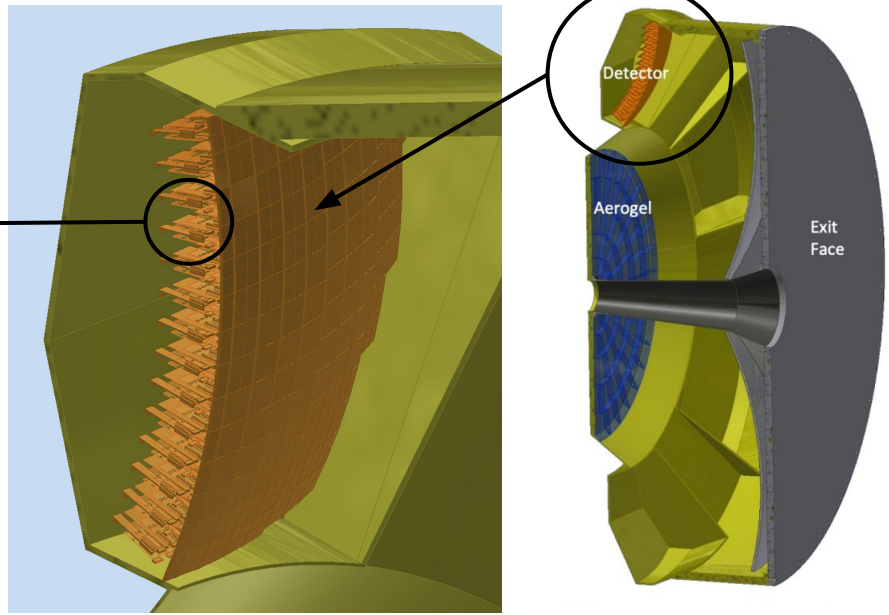
20 x 20 x 20 cm^3



Conceptual design of the final layout



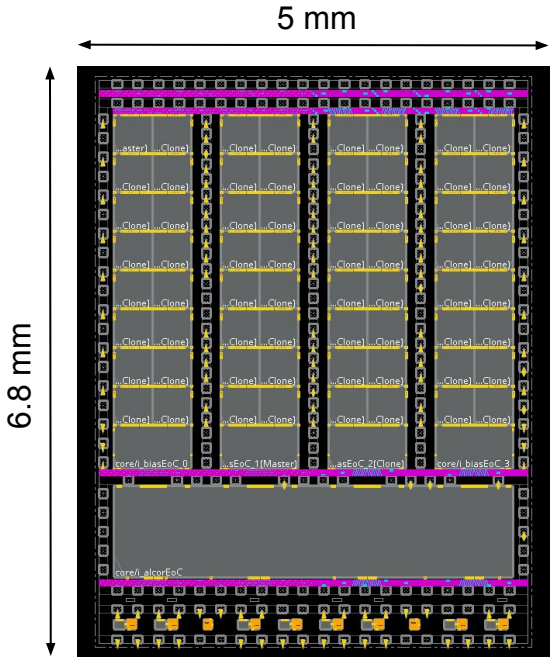
- Each PDU: 4x64 SiPM array device (256 channels)
- 1248 PDUs for full dRICH readout
- 4992 SiPM matrix array (8x8)
- **4992 ALCOR v3**, 64-channel each
- **319488 readout channels**

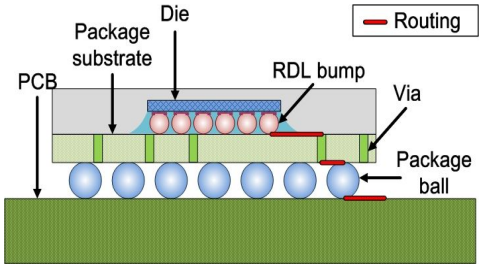


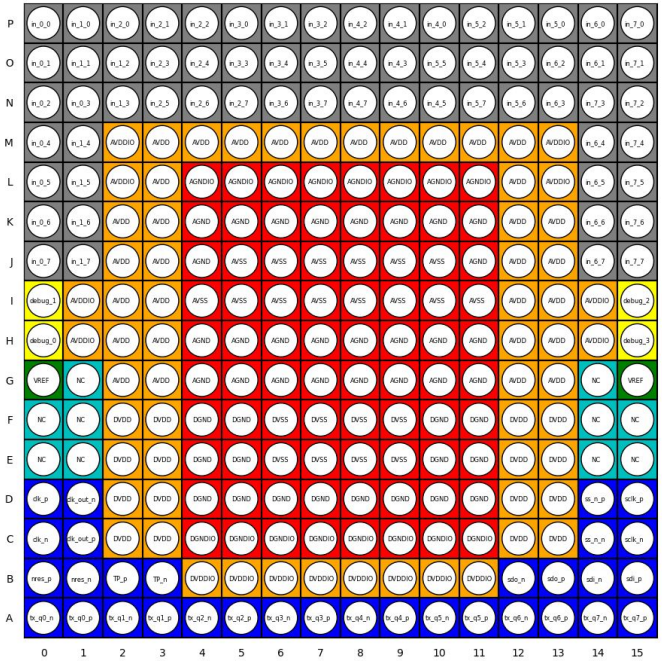
ALCOR v3

ALCOR v2: 32-channel wire bonded ASIC

ALCOR v3: 64-channel ASIC, flip-chip BGA package







8x8 pixel matrix ASIC (64 channels)

- SiPM inputs bump pads between the pixel sectors
- Digital EoC in the bottom part

256 balls, 1mm pitch BGA package

- Power and ground on inner/mid contacts
- I/O on outer contacts

ALCOR v3 new features for EIC

Operation of ALCOR at multiple of EIC clock frequency (98.52 MHz)

- Nominal ALCOR v3 clock frequency: 98.52 MHz x 4 **= 394.08 MHz**
- Digital logic, TDCs and serializers/drivers re-implemented and verified at 394.08 MHz

ePIC **streaming data** acquisition system (no traditional hardware trigger)

- **Digital shutter**: “inhibit” pixel digital logic to suppress out-of-gate DCR hits → reduce data throughput
- ~10.2 ns bunch crossing, ~300 ps bunch length, select 2-3 ns time window → 3x-5x data reduction before ALCOR digitization
- Asynchronous digital shutter implemented in ALCOR v3 pixel logic using external test-pulse signal
- **Programmable delay chain**: 4 configuration bits at channel-level (LSB ≃ 350 ps, TYP corner) and 4 configuration bits in the End of Column (LSB ≃ 100 ps) to adjust offsets between different pixels and columns
- Shutter needed only when DCR becomes higher due to SiPMs taking radiation damage over time → use first period of ePIC data taking to optimize **shutter calibration**

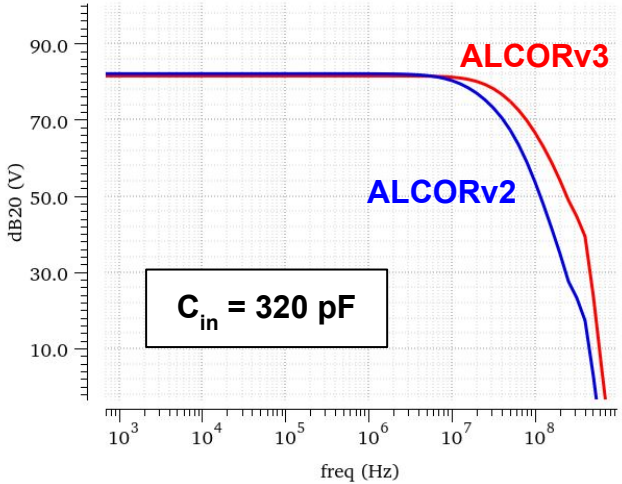
ALCOR v3 front-end

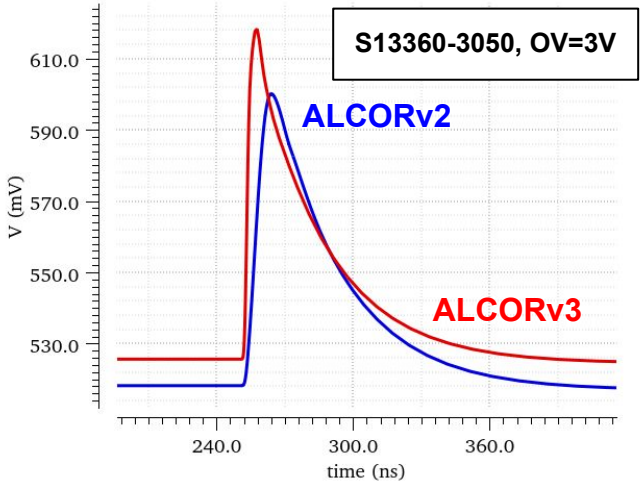
Small revisions on ALCOR FE design

- **Increased amplifier bandwidth** to improve time resolution
  - SR: 10 MV/s → 35 MV/s
  - rise time: 11 ns → 6 ns
  - ampl: 82 mV → 93 mV
  - rmsNoise: 1.6 mV → 2.7 mV
  - jitter: 160 ps → 80 ps

- **Hysteresis discriminator** to avoid re-triggering on slow tail with very low thresholds

Tape-out scheduled for Fall 2024





ALCOR FEB

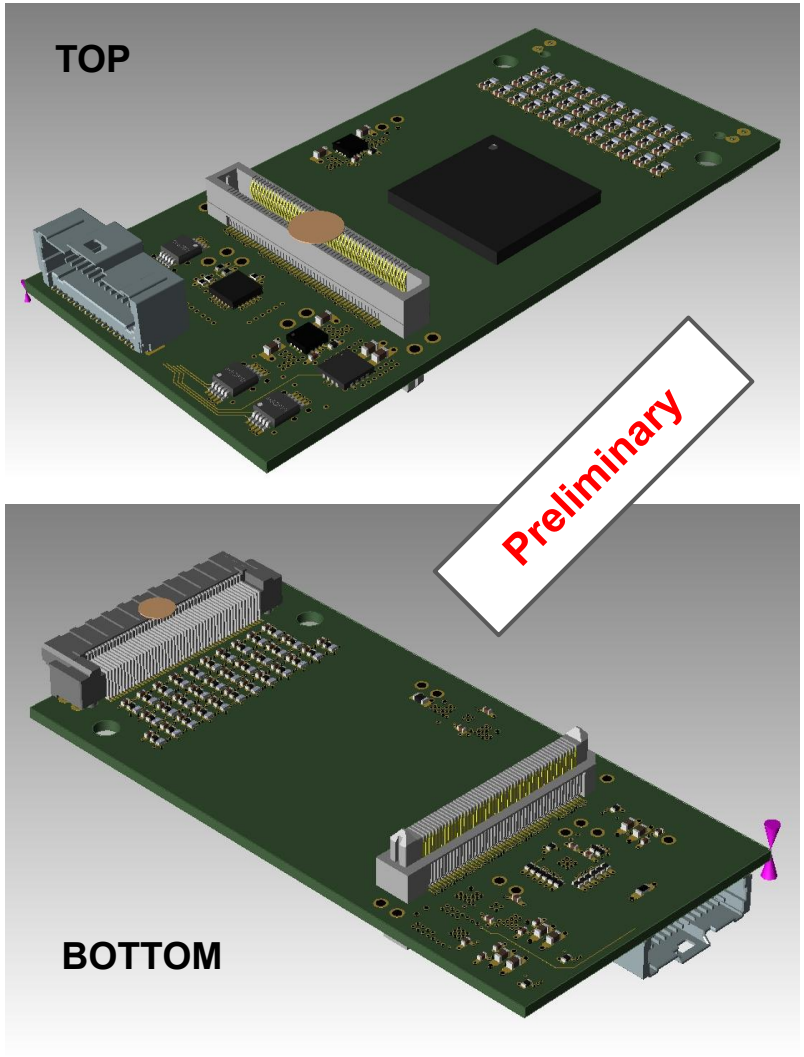
Close cooperation with Bologna colleagues for RDO design, SiPMs requirements and space constraints

Preliminary selection of connectors and components:

- **Master ALCOR bus** (between RDO and first FEB, digital signals): *Samtec ERM5-050-04.0-L-DV-TR*
- **Slave ALCOR bus** (between first and second FEB, digital signals): *Samtec ERF5-050-05.0-L-DV-K-TR*
- **Services connector** (SiPM Vbias and annealing, ALCOR LV): *Molex 2035663007*
- **SiPM connector** (SiPM signals, Vbias and annealing): *Samtec LSHM-150-01-L-RH-A-N-K-TR*

➢ Dedicated PCB section for SiPMs HV routing: 8 Vbias channels, 1 A each (in annealing mode)

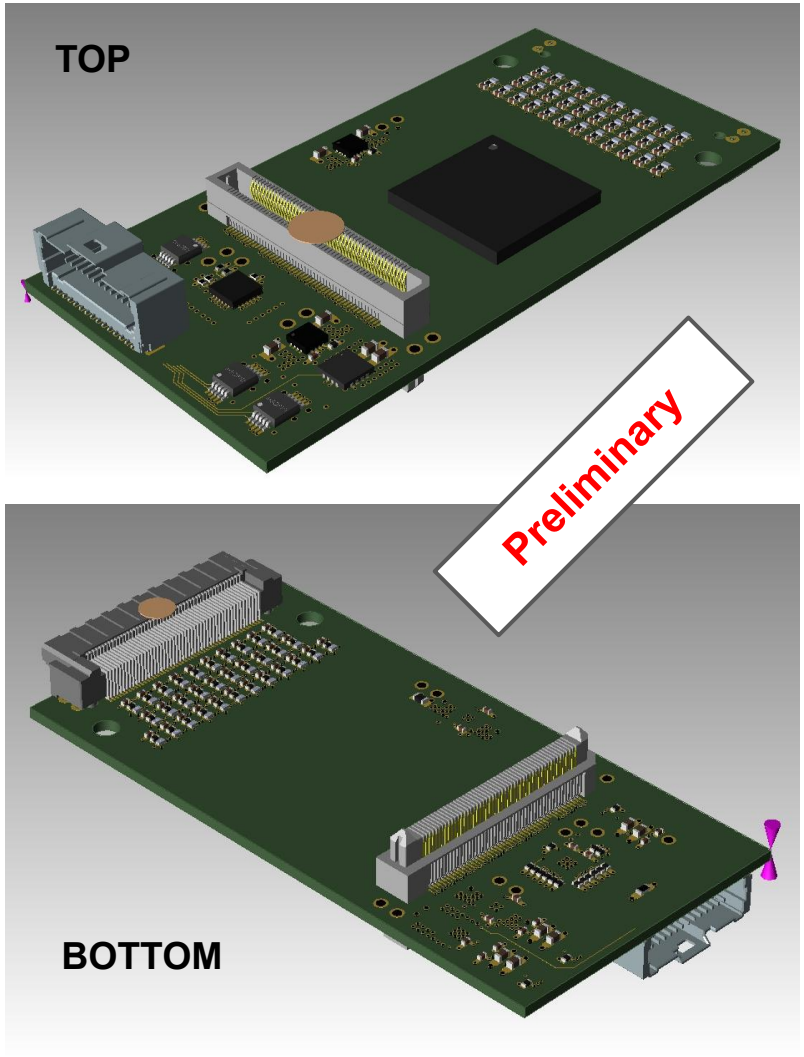
➢ FEB to support T > 100 °C (for annealing mode)



ALCOR FEB

Preliminary selection of connectors and components:

- **Linear Regulators** (2.5 V DVDD_IO, 1.2 V DVDD, 1.2 V AVDD): *Analog Devices ADP1752ACPZ-2.5-R7, ADP1761ACPZ-R7*
- **Current monitors** (before regulators): *Microchip Technology MIC2040-1YMM-TR*
- **I2C to Parallel-Port Expander** (read/control regulators and current monitors): *Texas Instruments PCF8575RGER*
- **RC High Pass Filter** (AC-coupling between SiPMs and ALCOR)
- **Annealing circuit**: to be included

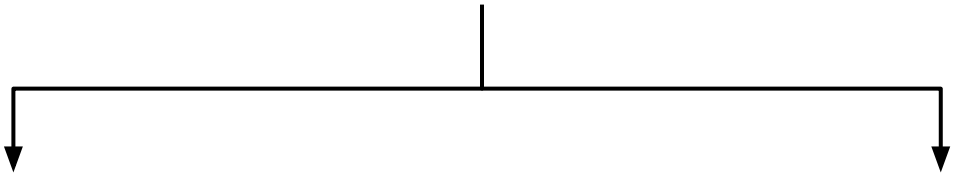


Schedule

Our aim is to have the first FEBs validated by Spring 2027 in order to begin the PDUs assembly

- Fall 2024: ALCOR v3 MPW tape-out and BGA package
- Spring 2025: ALCOR v3 BGA devices received → electrical characterization and integration tests

Evaluate readiness for mass production



- Fall/Winter 2025: ALCOR Engineering Run
- Summer 2026: start ALCOR mass production tests, FEBs assembly and validation

- Summer/Fall 2025: ALCOR v3.1 MPW tape-out
- Spring 2026: ALCOR v3 BGA devices received → electrical characterization
- Summer 2026: ALCOR Engineering Run
- Winter 2026: start tests of ALCOR mass production, FEBs assembly and validation

ALCOR QA → Mass production tests

Different options are currently being evaluated

- N. FEBs: 4992 → N. ALCOR: 4992 (increase to include spares)
- 7500 ALCOR → 85% yield → 6375 ALCOR
- Test time: 5-10 min./ALCOR (to be defined, test procedure used for ALCOR v2.1 as reference)
- 7500 ASIC · 10 min./ASIC = 75000 min. = 1250 h.

<u>Manual handling</u> (in-house testing)

6 h./day · 5 days/week = 30 h./week

1250 h. / 30 h./week = 42 weeks ⇒ **10-11 months**

- ➢ Parallel setups to reduce time for mass testing (contribution from other INFN sections under discussion)
- ➢ After first batch, rest of production can be tested in parallel with PDUs assembly → no schedule delays

<u>Automated handler</u> (external company)

24 h./day · 7 days/week = 168 h./week

1250 h. / 168 h./week = 7-8 weeks ⇒ **2 months**

- ➢ Will require external company to perform the tests (→ **additional costs**)
- ➢ No manpower required for mass tests, but still requires manpower to develop and debug the test system

Summary

- ALCOR fulfills dRICH requirements for SiPM readout
  - Several laboratory and beam tests demonstrated ALCOR-based readout capability to measure single photons, approaching 100 ps time resolution
  - New test beam at CERN-PS ongoing now to validate the full system and evaluate its performance (2048 readout channels)
- Identified technical solutions to meet EIC-driven specifications
  - Digital shutter to reduce data throughput
  - New ALCOR clock frequency: 98.52 MHz x 4 = 394.08 MHz
- Other design revisions for ALCOR new version defined
  - Analogue FE optimization, hysteresis discriminator
  - New chip layout for BGA package
  - TMR SEU protection added also for periphery configuration registers, Hamming code SEU protection for FSMs: Single Error Correction, Double Error Detection codes (SECDED)
  - ASIC tape-out in Fall 2024
- Irradiation tests campaign
  - SEU and TID tests at Centro of Proton-Therapy in Trento with ALCOR current version foreseen in July 2024

Backup Slides

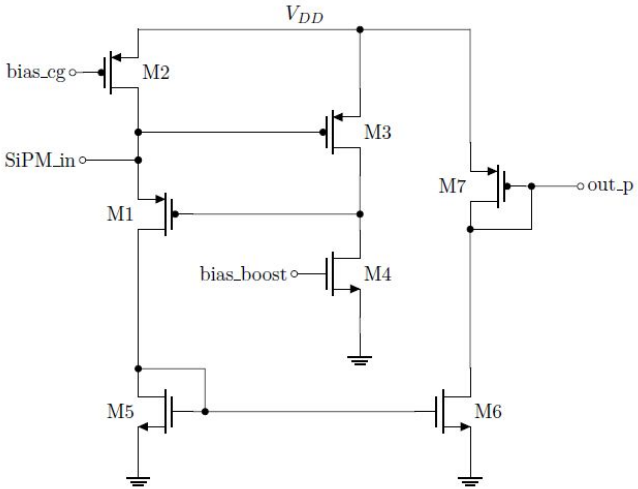
Charges

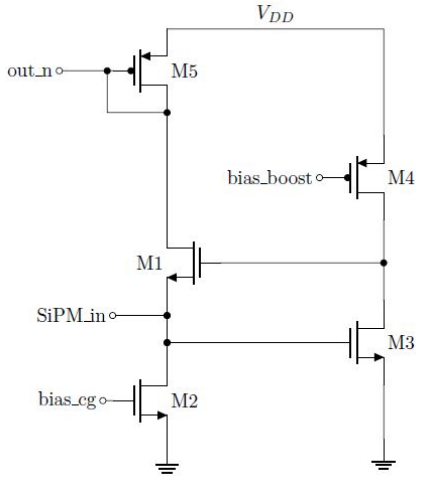
1. Are the technical performance requirements appropriately defined and complete for this stage of the project?
2. Are the plans for the various detector electronics and data acquisition systems appropriately documented and complete for this stage of the project?
3. Are the current plans from front-end electronics to data acquisition for the detector likely to achieve the technical performance requirements, with a low risk for cost increases, schedule delays, and technical problems?
4. Are the schedule assumptions for the fabrication of the various electronics and data acquisition systems and assembly plans reasonable and consistent with the overall detector schedule?
5. Have ESH&Q and QA considerations been adequately incorporated into the plans at their present stage?

ALCOR Front-End

Input stage

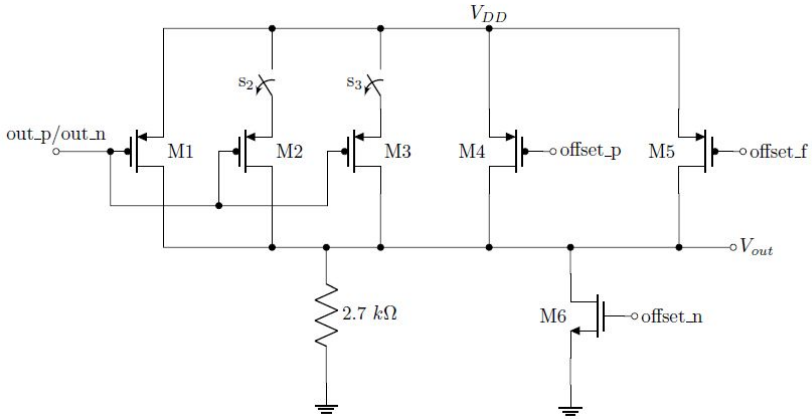
- Dual-polarity RCG current conveyor
- Programmable bias currents: CG (30-100 μA) and BOOST (1-4 mA)
- Z_{in} ~ 10-20 Ω





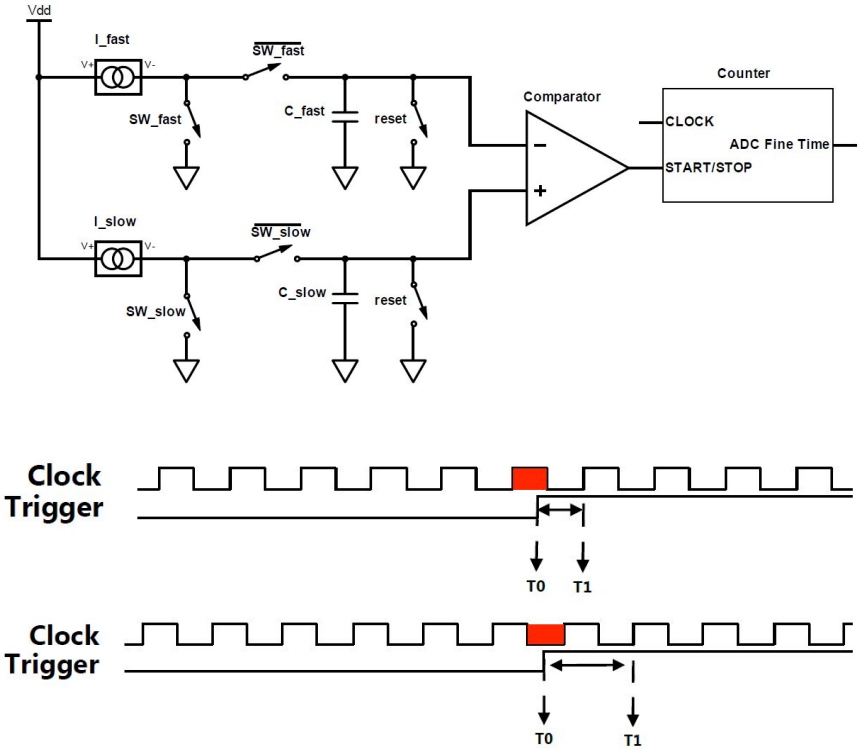
Output stage

- TIA gain: 2.7 kΩ
- 4 gain settings: 1/3, 4/3, 7/3 and 10/3
- DC coupled: baseline compensation based on gain and CG bias current settings + fine offset adjustment (3-bit)

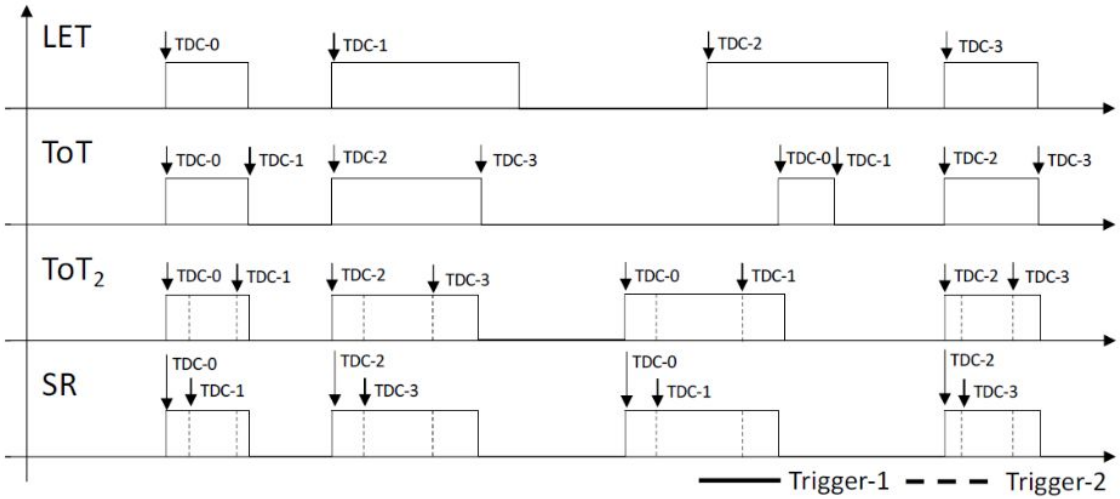


Time to Digital Conversion

- Coarse time: 15-bit clock counter
- Time conversion performed by TDC based on analogue interpolation (9-bit fine time):
  - ***fast ramp***: C_{fast} charged to measure the phase between the event trigger and the clock
  - ***slow ramp***: counts the clock cycles to measure the fine time until C_{slow} and C_{fast} voltages are equal
- I.F. 64 or 128 → LSB = 25-50 ps @320 MHz
- Measured time interval: 0.5 - 1.5 clk period
- TDC conversion time: [200, 600] ns
- 4 TDCs per pixel for event derandomization



ALCOR pixel operating modes



4 operating modes:

- **LET**: leading edge measurement
- **ToT**: Time-over-Threshold measurement using the first discriminator for both edges
- **ToT2**: Time-over-Threshold measurement using both discriminators
- **SR**: slew-rate measurement

Each mode can be set to:

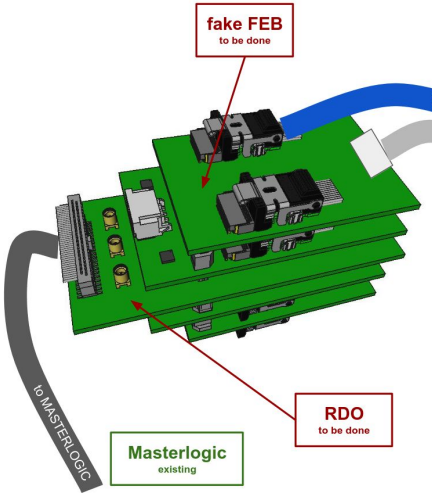
- **FE**: normal operation mode
- **FE_TP**: send test-pulse to analogue front-end
- **TDC_TP**: send test-pulse to pixel control logic to test and calibrate TDCs (bypass front-end)

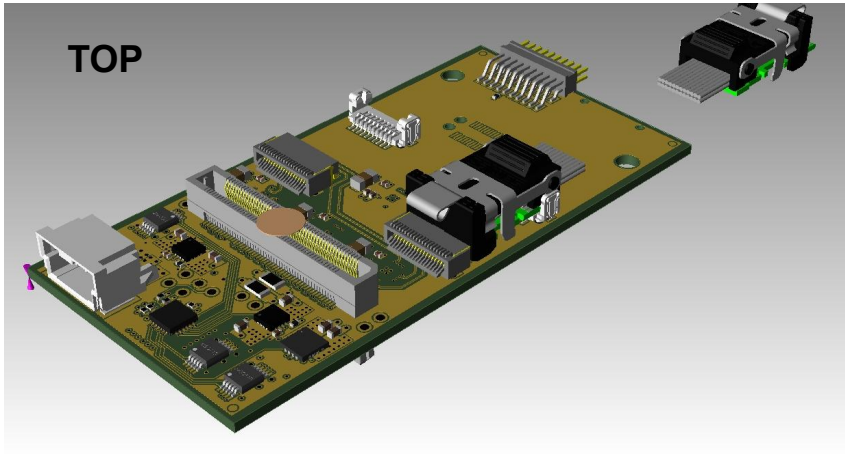
Each pixel can also be disabled

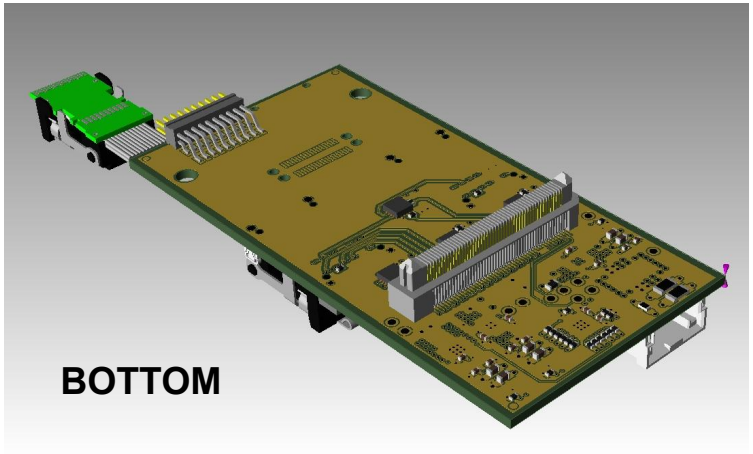
“Fake” FEB

Support 2024-2025 dRICH activities when final FEB and ALCOR v3 are not available yet

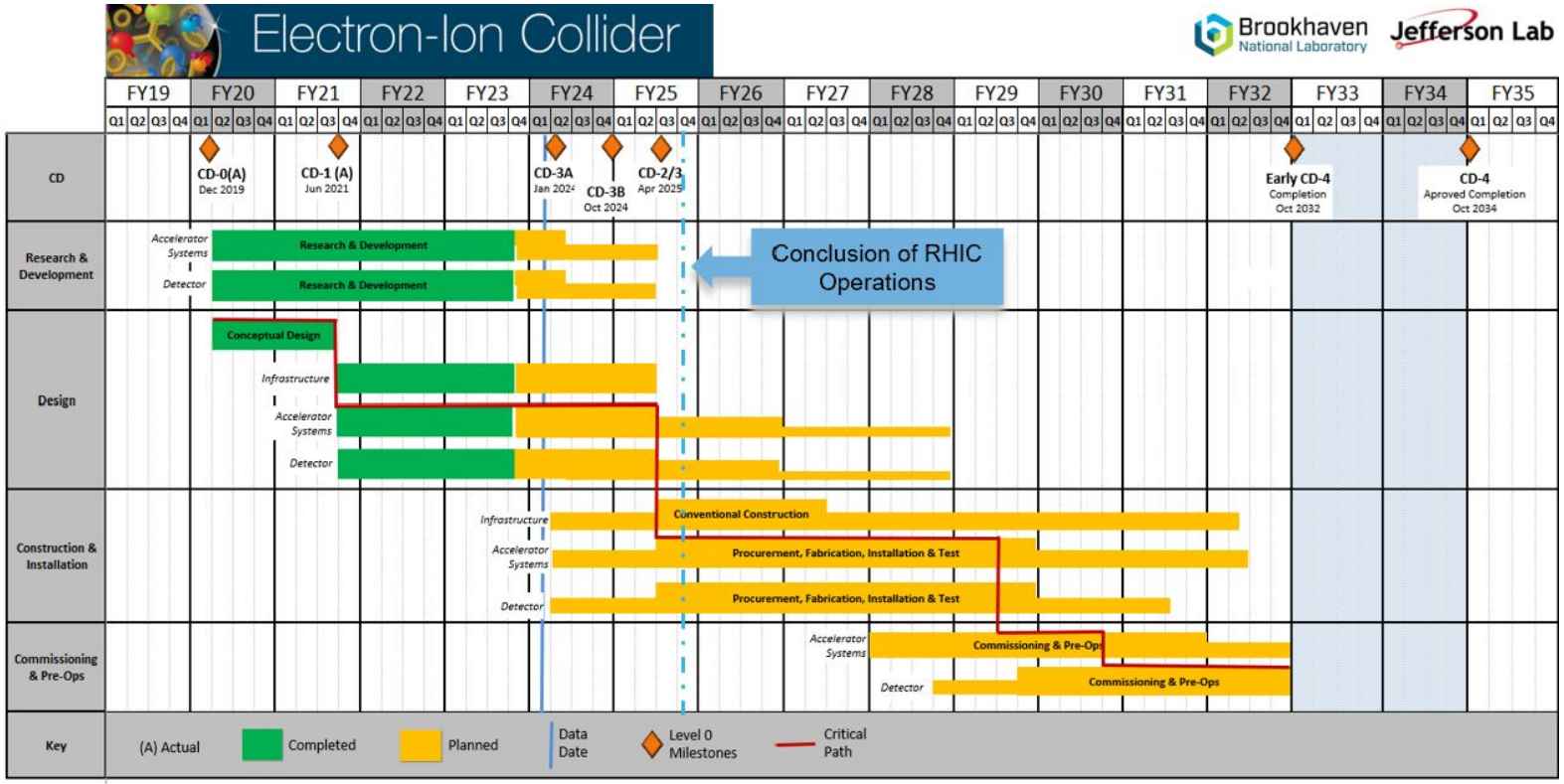
- allows integration tests of RDO with current ALCOR-FE-DUAL boards (already available and validated)
- 4 fake-FEBs + 1 RDO (still off-detector)







The EIC schedule



Current & future plans

Front-end electronics

- developments toward final ASIC version (ALCOR-v3, 64-channels, BGA package)
  - upgrade front-end to improve time resolution
  - include digital shutter, hysteresis to discriminator and other optimisations
  - optimise chip layout for “flip-chip” BGA packaging

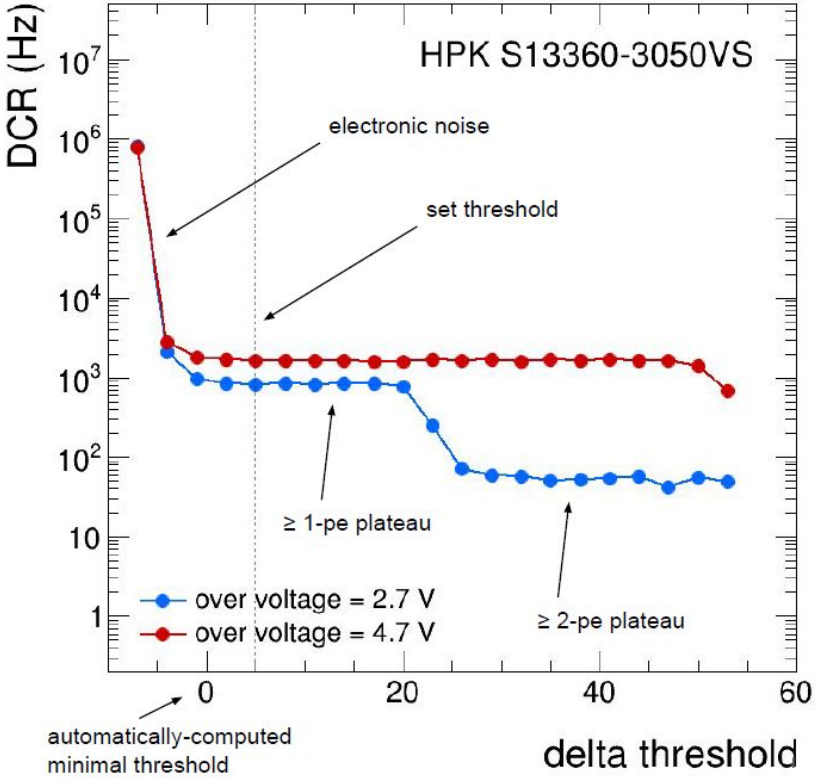
Readout electronics

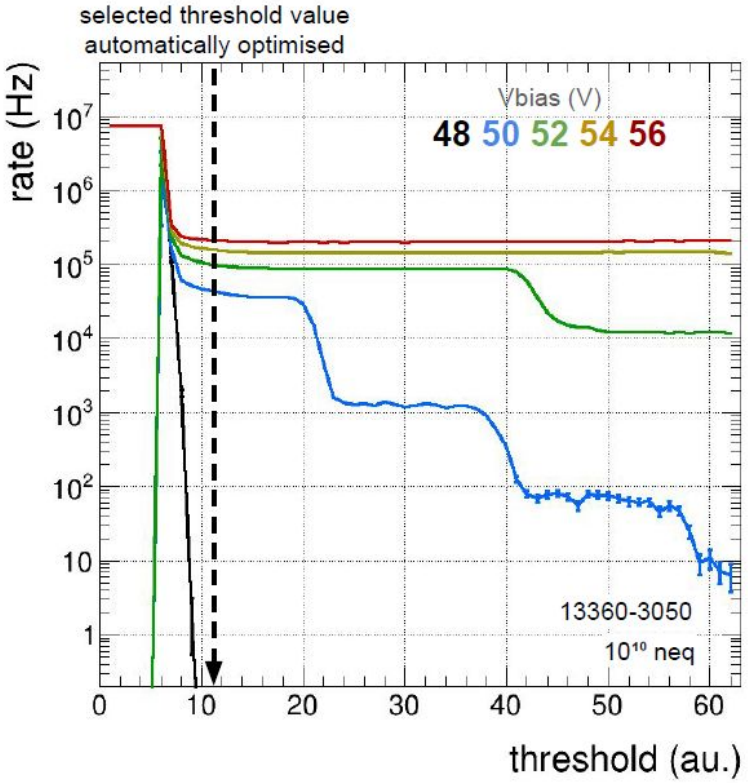
- design of “Fake FEB” to test readout with first prototype RDO already for the end of 2024
  - target is a beam test in 2024

Radiation tolerance

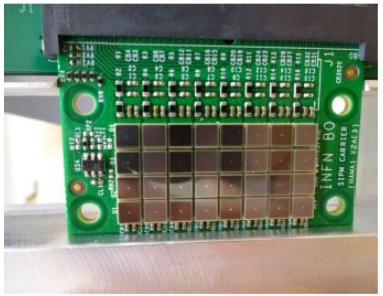
- measure radiation damage / tolerance of susceptible components
  - ALCOR chip
  - PCB components
- measure SEU rates and latch-ups

ALCOR for SiPM characterization measurements





ALCOR for SiPM characterization measurements

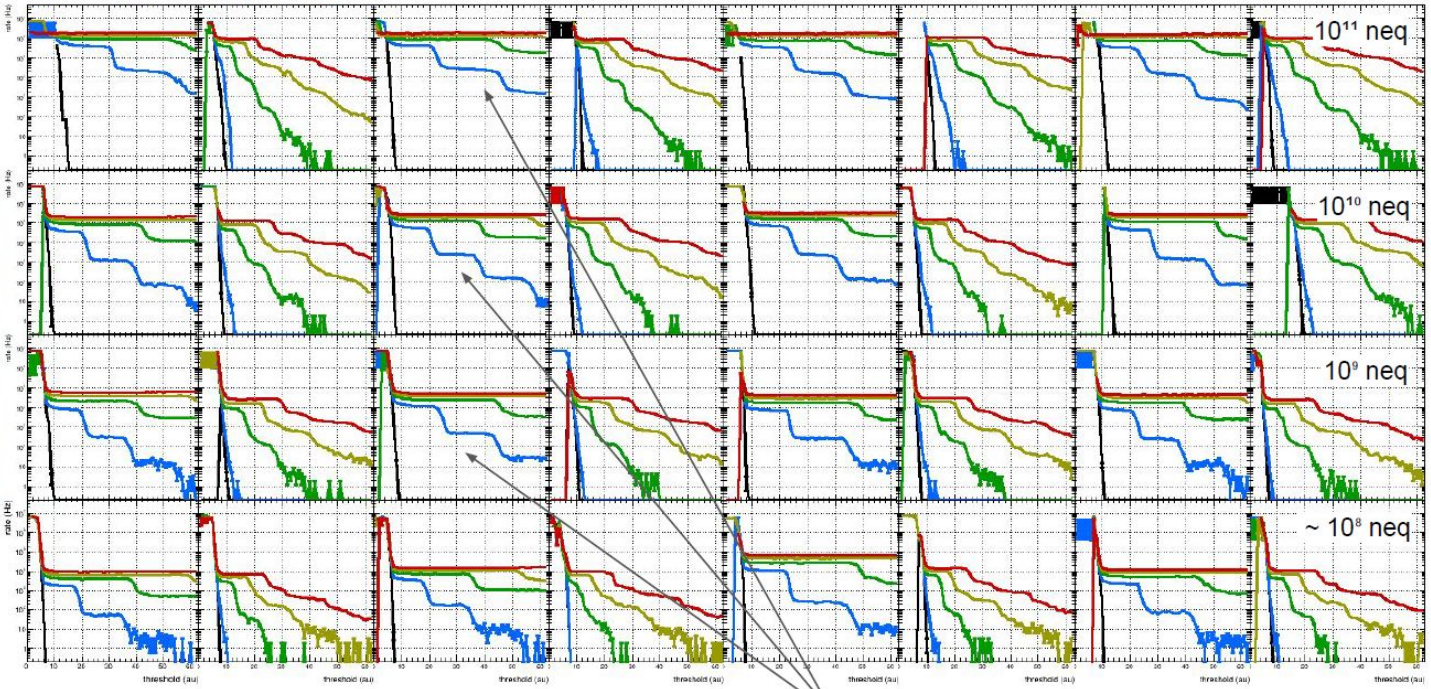


irradiated board
after annealing

still working!

T = -30 C

13360-3050 13360-3025

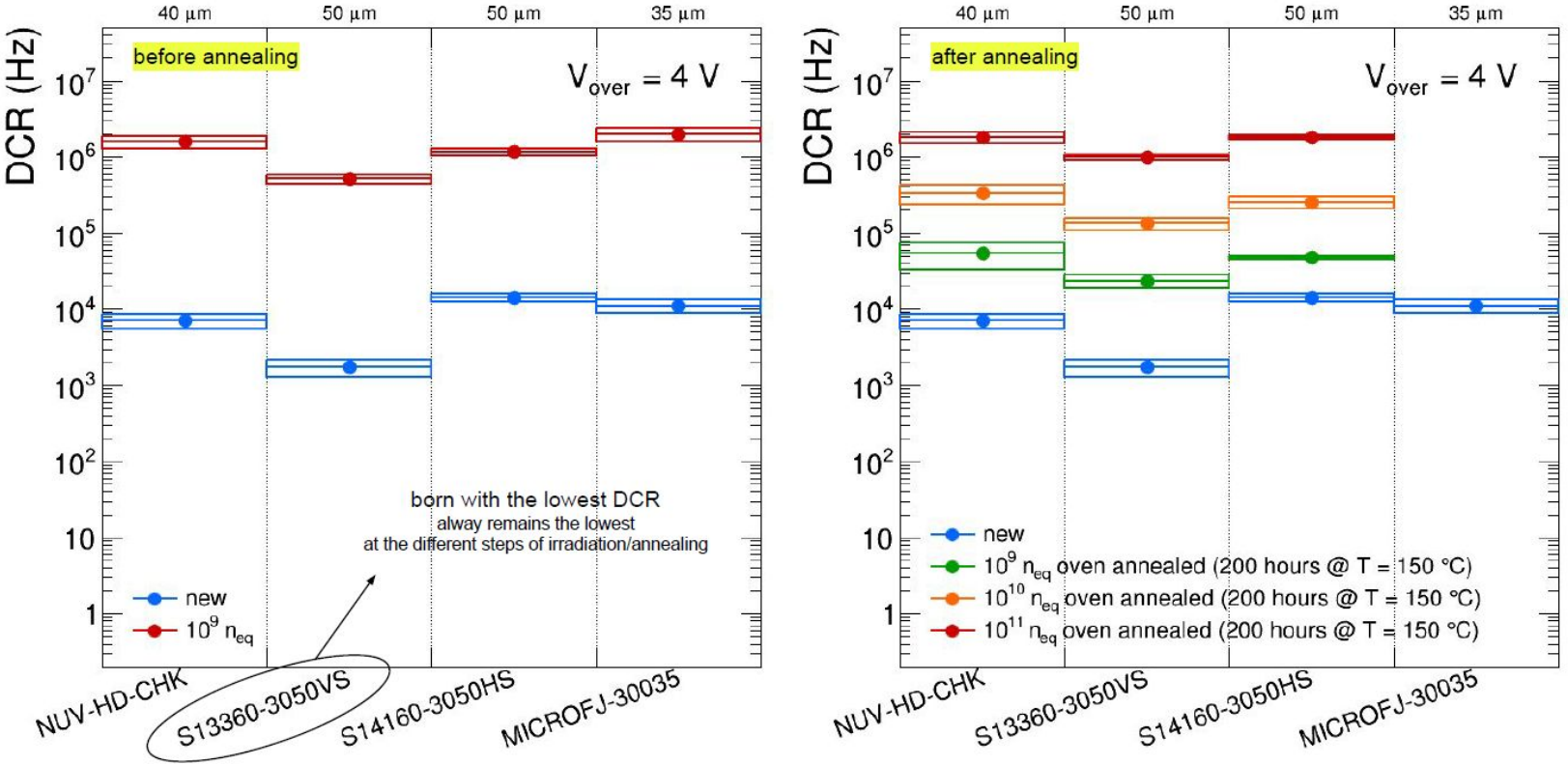


clear single-photon
separation up to 10^{11}

Vbias (V)
48 50 52 54 56

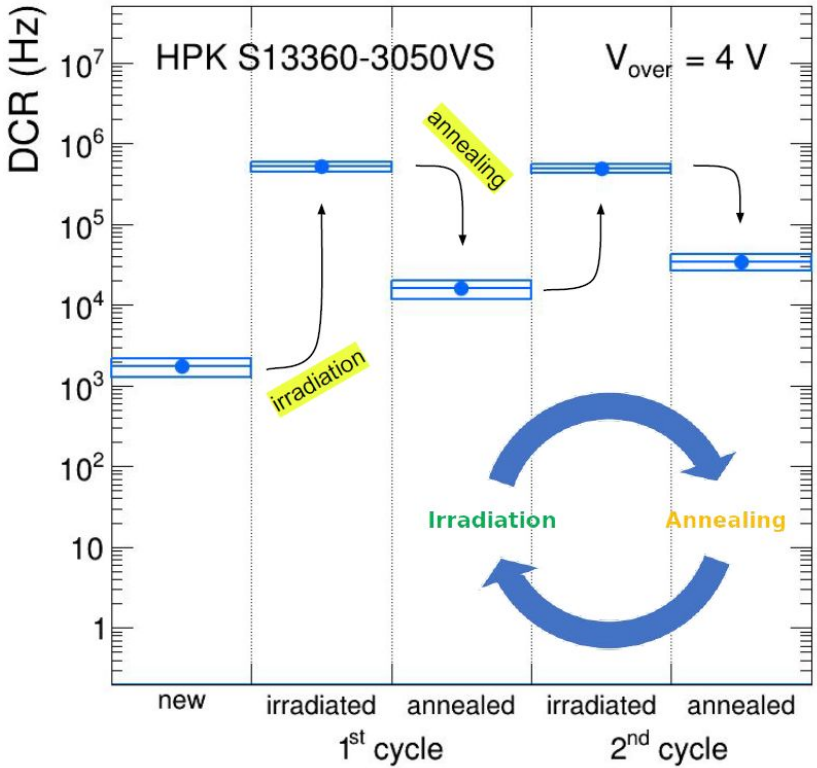
ALCOR for SiPM characterization measurements

DCR after irradiation and annealing



ALCOR for SiPM characterization measurements

Repeated irradiation-annealing cycles



Test reproducibility of repeated irradiation annealing cycles to simulate a realistic experimental situation

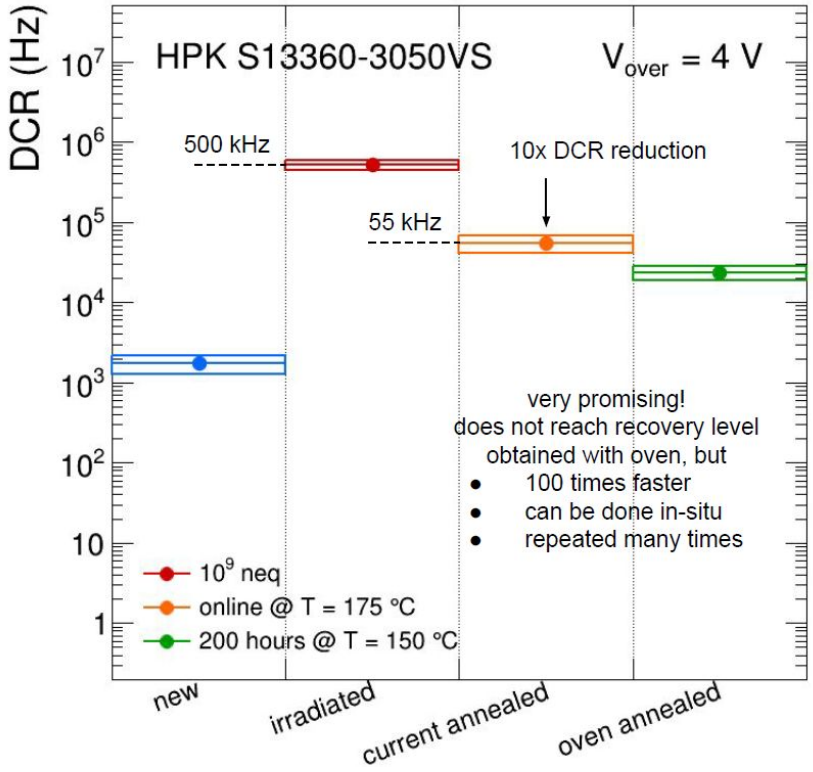
- **irradiation:** fluence/cycle of 10^9 neq
- **annealing:** in oven for 150 hours at 150 °C

Full characterisation at each step:

- new
- after each irradiation
- after each annealing

ALCOR for SiPM characterization measurements

Online annealing



In-situ annealing:

- forward bias, ~ 1 W / sensor
- T = 175 °C, thermal camera monitor
- 30 minutes

ALCOR for SiPM characterization measurements

Light response after irradiation and annealing