DE LA RECHERCHE À L'INDUSTRIE

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The SALSA ASIC for the EPIC MPGD tracker readout

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PDR on EIC DAQ and electronics

11/06/2024

SALSA specifications

Present status

Development plans

CHARGE QUESTIONS ADDRESSED

1) Are the technical performance requirements appropriately defined and complete for this stage of the project?

2) Are the plans for the various detector electronics and data acquisition systems appropriately documented and complete for this stage of the project?

3) Are the current plans from front-end electronics to data acquisition for the detector likely to achieve the technical performance requirements, with a low risk for cost increases, schedule delays, and technical problems?

4) Are the schedule assumptions for the fabrication of the various electronics and data acquisition systems and assembly plans reasonable and consistent with the overall detector schedule?

5) Have ESH&Q and QA considerations been adequately incorporated into the plans at their present stage?

THE MPGD TRACKERS OF EPIC EXPERIMENT

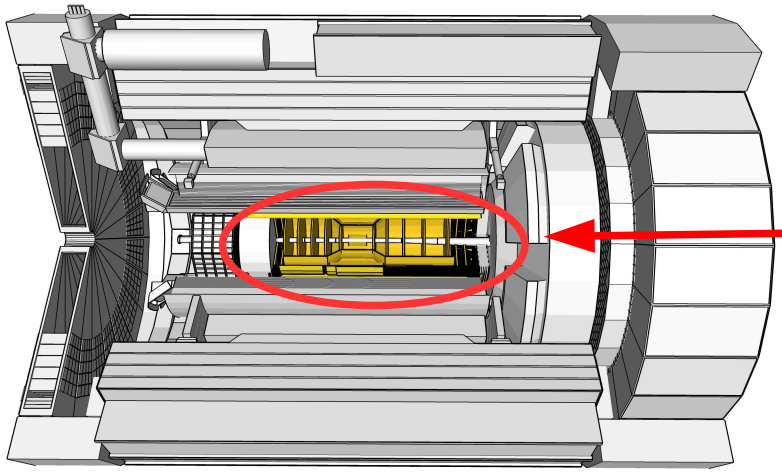
Charge 1

MPGD detectors foreseen in EPIC

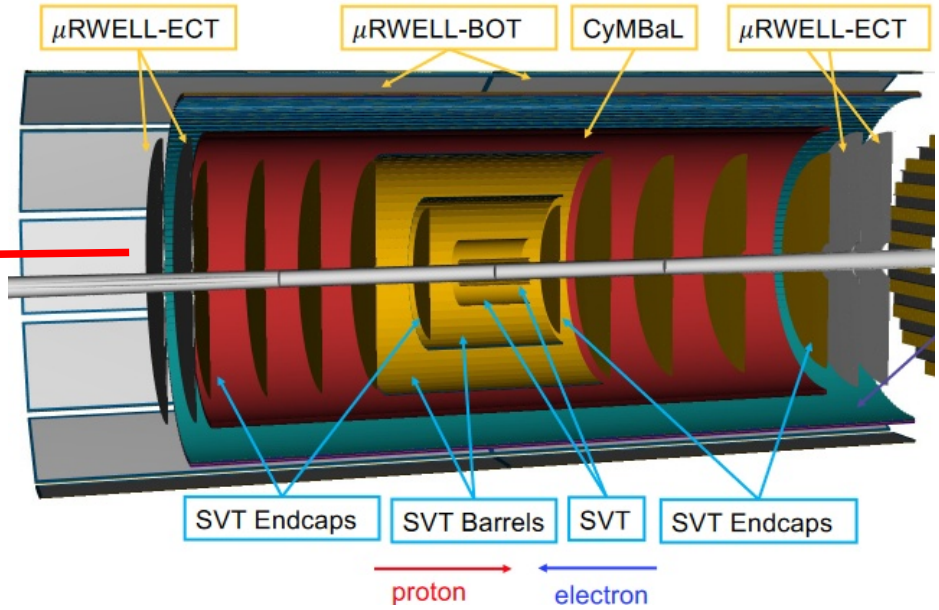
- Cylindrical Micromegas barrel layer (CyMBaL) → ~30 k.channels
- µRWell barrel outer tracker (µRWell-BOT) → ~100 k.channels
- µRWell end cap tracker (µRWell-ECT) → ~30 k.channels

- Same frontend ASIC to read all MPGD trackers → **SALSA**
- Shared frontend board designs between MPGD groups, with some adaptation of form factors

EPIC detector



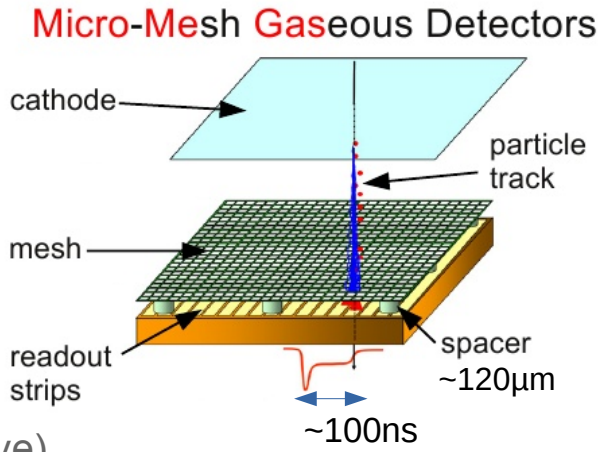
Central trackers



REQUIREMENTS ON MPGD DETECTOR READOUT

Micro-Pattern Gaseous Detector characteristics

- Detection of gas ionization from charged particles
- Small gaseous amplification gap → short signals ~ 100 ns
- Gain 5-10k → typical signal amplitude ~35 fC, max ~200-250 fC

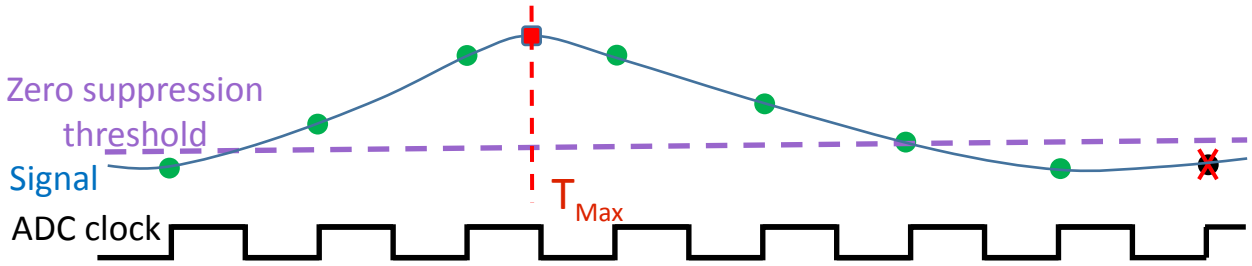


Required readout performance

- Threshold ~3 fC to get factor 10 on signal / threshold
- Noise level ~0.5 fC
- Readout time resolution << detector resolution (~10 ns or above)
- Stand channel occupancy ~10 kHz
- Resistant to mild radiation (10 krad, 10^{11} n_{eq}/cm^2) and magnetic field (1.8 T)

Readout strategy

- Analog amplification and shaping, followed by continuous ADC readout
- Correction of pedestals, common mode noise, baseline variations + digital shaping
- Zero-suppression: selection of samples above threshold + neighbors
- Integrated reconstruction of signal amplitudes, times and widths
- Continuous readout mode, non-ZS samples are sent to DAQ permanently without trigger



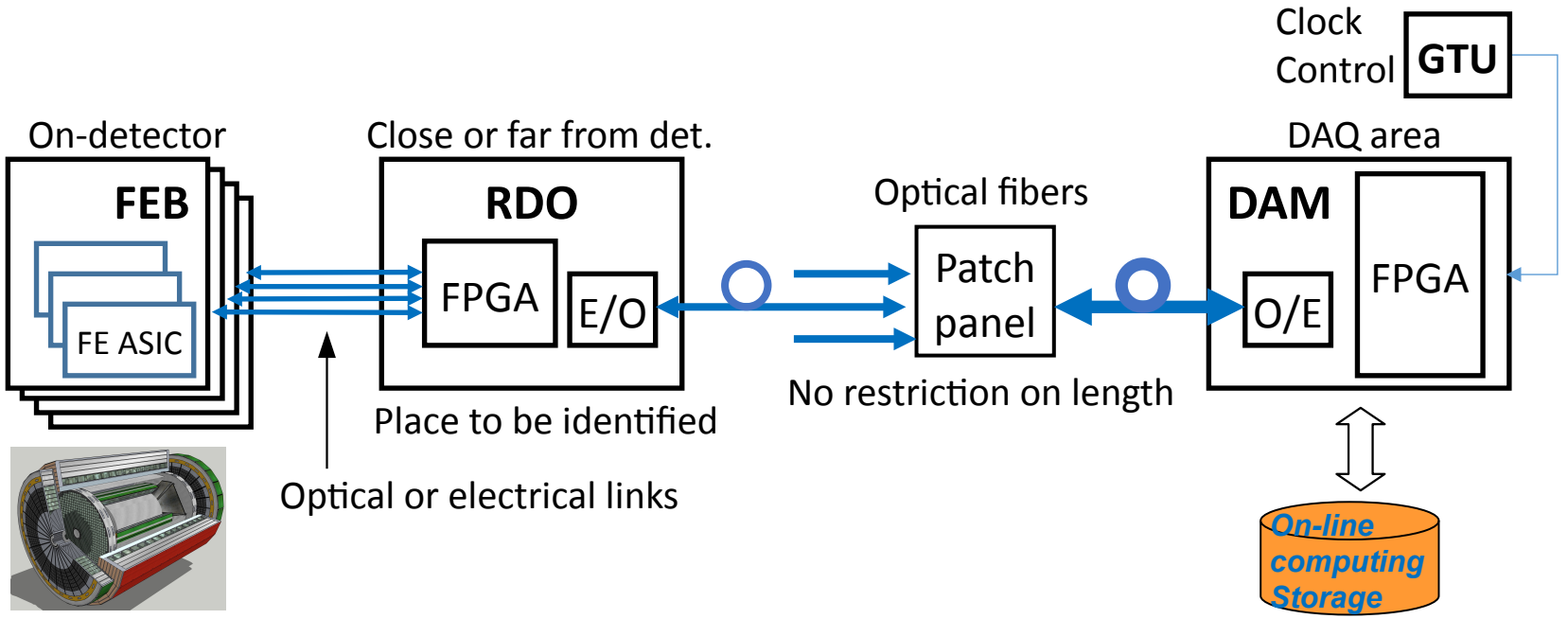
Charge 1

INTEGRATION IN THE EPIC DAQ SYSTEM

Charge 1

EPIC data acquisition chain

- FEB: frontend boards carrying readout ASICs, specific to sub-detectors
- RDO: readout module, 1st data aggregation, clock and control dispatch, common design framework with adaptations between sub-detectors
- DAM: data aggregation module, interface with computing and global timing and control unit, common for all sub-detectors
- Downstream signals: clock, synchronous commands, slow-control
- Upstream signals: physics, calibration and monitoring data



SALSA : VERSATILE READOUT CHIP FOR MPGD

Motivations of the project

- To develop a new versatile multi-channel readout chip in the framework of the EPIC MPGD trackers and beyond
  - for MPGD trackers but not only, also for MPGD TPCs, photon detectors,...
  - with possible future developments for other kinds of detectors (calorimeters, non-MPGD photon detectors) and/or specific constraints
  - adapted to streaming readout DAQs
- Integrated per-channel ADC and digital processing (DSP)
- Large ranges in term of signal amplitudes, electrode capacitances, peaking times, signal rates
- TSMC 65nm technology for improved performances and sustainability

Common initiative of Sao Paulo Universities and CEA Saclay IRFU

- Sao Paulo University (USP) + associated institutes designed the SAMPA chip (ALICE TPC), experts in on-chip ADC and digital processing
- IRFU developed several MPGD front-end chips (AFTER, AGET, DREAM,...) and other kinds of chips (SAMPIC and HGCROC TDC,..), experts in low-noise radiation-hard generic front-ends
- Large amount of complementary competences to collaborate on a common versatile front-end chip including digitization and digital processing
- Blocks developed by CERN in TSMC 65nm technology are also reused

SALSA CHIP TARGET SPECIFICATIONS, COMPARED TO EPIC MPGD REQUIREMENTS

Charge 1

Versatile front-end characteristics → EPIC MPGD needs

- 64 channels
- Large input capacitance range, optimized for 50-200 pF, reasonable gain up to 1 nF → **200 pF**
- Large range of peaking times: 50-500 ns → **100-200 ns**
- Large choice of gain ranges: 0-50, 0-250, 0-500 fC or 0-5 pC → **0-250 pC**
- Large range of input rates, up to 100 kHz/ch with fast CSA reset → **< 25 kHz**
- Reversible polarity (depends on kind of detector) → **negative**

Digital stage

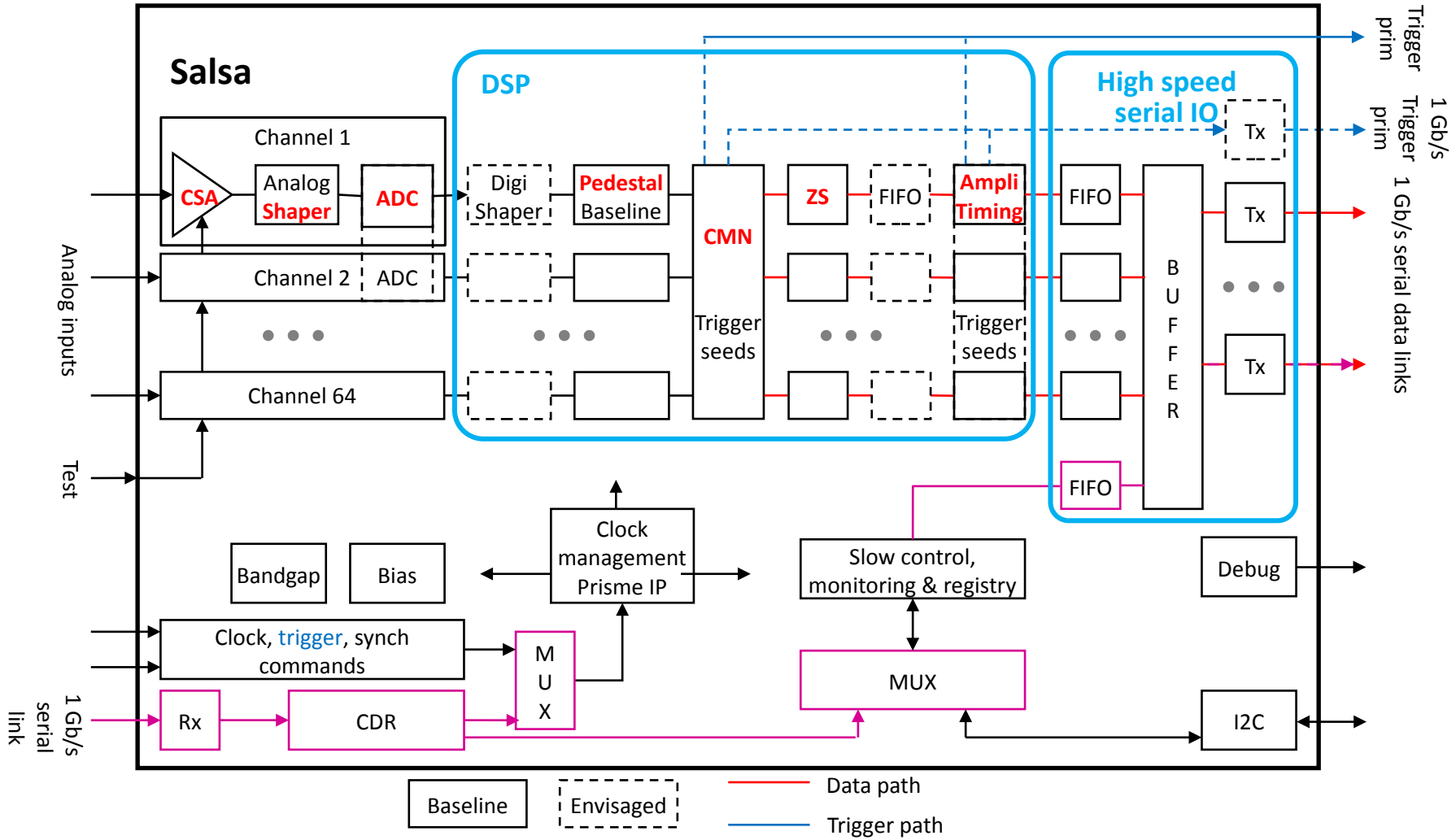
- Fast sampling ADC for each channel on 12 bits (> 10 effective bits) at up to 50 MS/s → **50 MS/s**
- Integrated DSP for internal data processing and size reduction, treatment processes to be configured according to user needs → **all processes**
- Continuous readout, triggered mode also available → **continuous readout**
- Several 1 Gb/s output data links → **1 gigabit link used at EPIC**

General characteristics

- ~1 cm² die size, implemented on modern TSMC 65nm technology
- Low power consumption ~ 15 mW/channel at 1.2V
- Radiation hardened (SEU, > 300 Mrad, > 10^{13} n_{eq}/cm^2) → **10 krad, 10^{11} n_{eq}/cm^2**

SALSA CHIP PRELIMINARY ARCHITECTURE

Charge 2

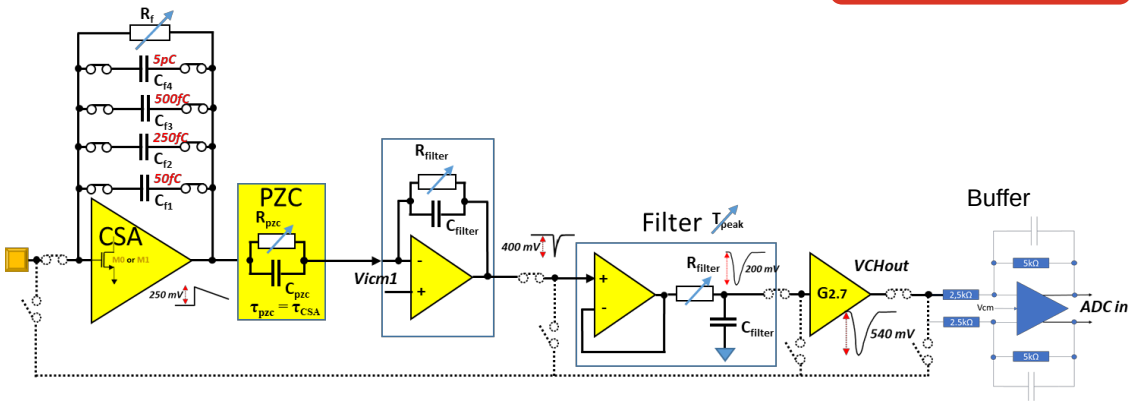


SIGNAL AMPLIFICATION AND DIGITIZATION

Charge 2, 3

Front-end stage

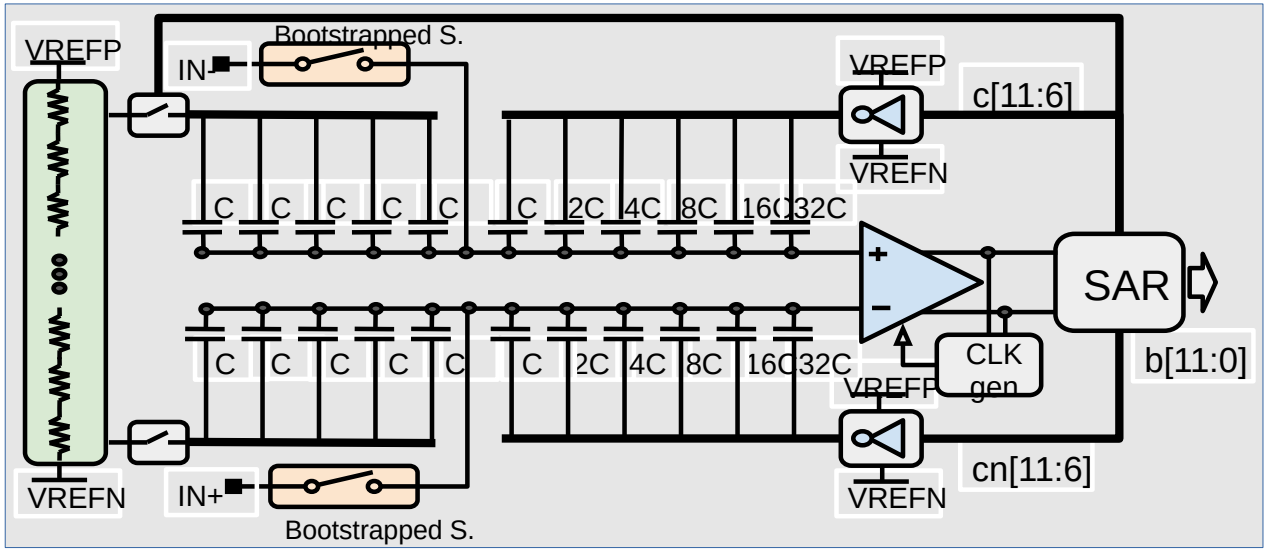
- Charge Sensitive Amplifier + Pole-Zero Cancellation + shaper
- 4 gain ranges: 0-50 fC, 0-250 fC, 0-500 fC and 0-5 pC
- 8 peaking times 50 to 500ns
- 2 input transistor sizes
- 2 polarities
- Integrated anti-saturation circuit
- Front-end elements can be by-passed
- Integrated test pulses



Scheme from P. Baron

ADC block

- 12 bits 5-50 MS/s SAR ADC
- Expected 10-11 ENOB bits



Scheme from H. Hernandez

DSP DATA PROCESSING, PRELIMINARY VERSION

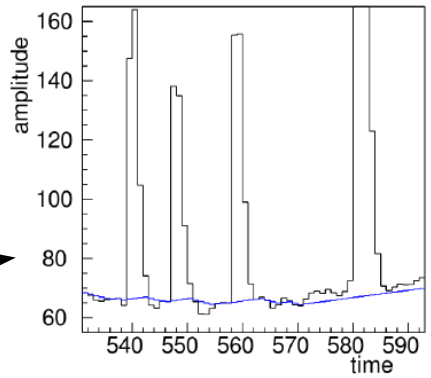
Charge 2, 3

General remarks

- Data processing, reduction and formatting from ADC values to output links
- Each process can be deactivated individually by user
- Process parameters through ASIC registers
- Part of codes from SAMPA chip
- Most of DSP features determined, details still under study

Baseline corrections

- Pedestal subtraction with fixed value per channel
- Common mode correction to reduce common noise impact, based on median value of samples of all channels for each sample time
- Baseline slope following algorithm



Plot from SAMPA doc

Digital shaping

- Cancellation of signal tail or peaking time correction with cascade of 4 first order IIR filters
- Algorithm from SAMPA, 2 x 4 parameters

$$y[n] = a_1 y[n-1] + b_0 x[n]$$

DSP DATA PROCESSING, PRELIMINARY VERSION

Charge 2, 3

Zero suppression

- Keep samples above fixed thresholds
- Tunable algorithm (add neighbor samples, to drop too short set of samples, keep 1 sample over N, etc...)

Feature reconstruction

- To further reduce data flux by extracting reconstructed data → peak finding algorithm, with extraction of amplitude + time + width
- Possible peak finding algorithms under study

Trigger management

- Samples kept when trigger signals received, with configurable latency
- Followed or not by zero suppression, feature reconstruction, etc…

Trigger generation

- Trigger primitives generated when samples above threshold, with conditions on number of samples, multiplicity, etc...
- Possibility to reduce latency by placing trigger generation early in the processing chain
- Nature of trigger primitives to be defined (logic signal, data on specific fast link, etc…)

STRUCTURE OF DATA OUTPUT

Charge 2, 3

Output data stream based on packets

- Packets with different kinds of data
- Packet identification by type, numbering and optionally timestamps
- Each packet buffered and transmitted through one of the Gbit/s links (1 only at EPIC)

Physics data packets

- Header + ADC sample values + reconstructed values
- Includes timestamps, chip address, channel numbers, possibly flags
- Sample data structure channel by channel
- Detail of format under discussion

Calibration data packets

- Same format as physics packets + type of calibration data

Information packets

- Carry information data: ASIC configuration, slow-control feedback, environmental informations, channel counting rates, etc...

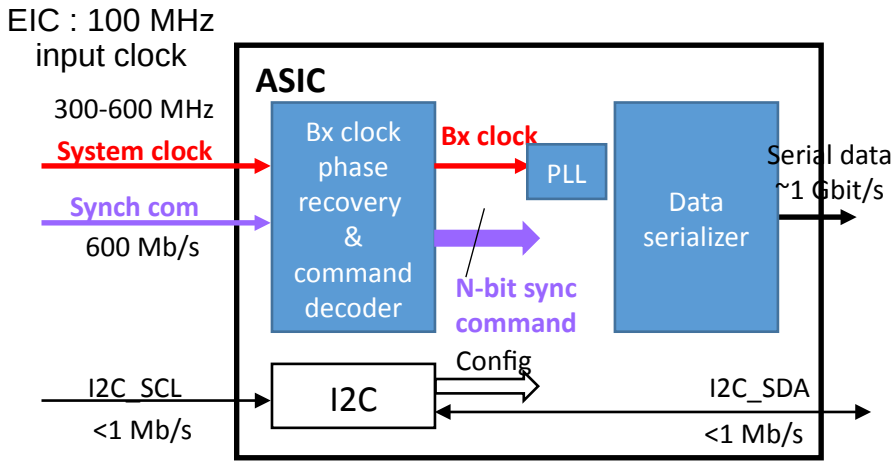
Error packets

- Information packet generated when error or warning encountered in ASIC

CLOCK, FAST COMMAND AND SLOW CONTROL INPUTS

Traditional way

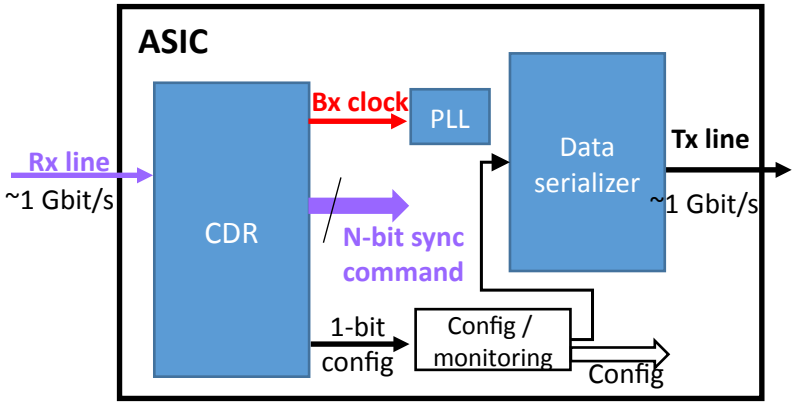
- 1 differential input for clock
- 1 differential input for fast commands
- 1 SDA + SDC I2C input for slow control and configurations
- Will be implemented in SALSA

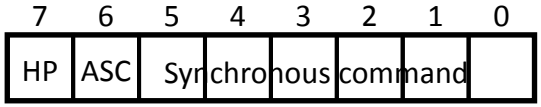


Single encoded line grouping all inputs

- High speed 1Gb/s differential input which carry clock + fast commands + slow-control
- Internal CDR in SALSA to extract the different parts
- 8 bits every 10 ns (EIC): 6 bits for fast command ID, 1 bit for slow-control, 1 parity bit
- Slow control output through information packets
- Simplify connectivity: 1 diff input for everything instead of 4
- Implementation in SALSA in parallel with the traditional way

Schemes from I. Mandjavidze





Charge 2, 3

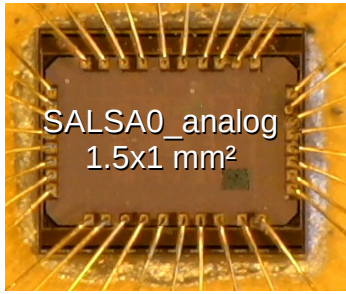
TIMELINE OF THE SALSA PROJECT

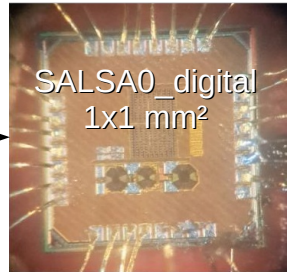
Steps of SALSA development

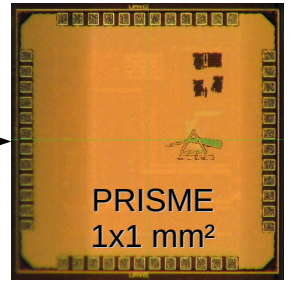
- 2020-22: Discussions and reflections on the project
- 2022-23: SALSA0 prototypes to study first designs
  - SALSA0_analog featuring 4 front-end channels
  - SALSA0_digital featuring an ADC block
- 2023: PRISME prototype to test PLL block + first version of general services
- 2023-24: SALSA1 prototype to test full front-end + ADC chains
- 2023-25: SALSA2 prototype to test fully featured ASIC including DSP, but with small number of channels (≤ 32)
- 2025-26: SALSA3 as pre-serial prototype with nominal number of channels

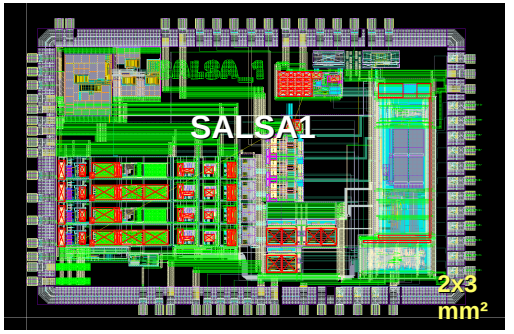
Current status

- SALSA0 prototypes tested in 2023-2024, performance evaluation and bug fixes of frontend and ADC blocks
- PRISME prototype tested from early 2024, bug fixes on PLL block, performance evaluation ongoing
- SALSA1 prototype submitted for production in April 2024
- SALSA2 architecture and DSP design ongoing, submission foreseen March 2025



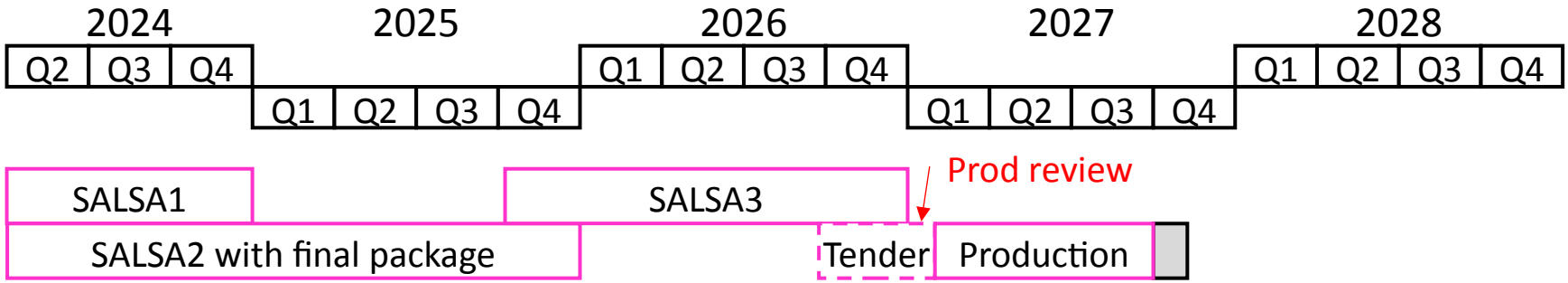






PLANNING AND RISKS

Planning of production



- > 4000 ASIC to produce to read all EPIC MPGDs, larger production if requests from other projects
- ~9-12 months production in 2027 including packaging and tests
- Tight schedule mainly driven by SALSA development phases
- With 6 to 9 months contingency

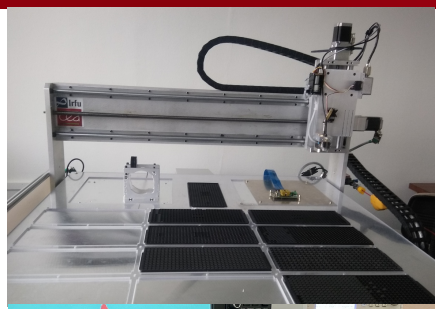
Main risks

- Unexpected SALSA behavior or performance issues
  - Thorough evaluations on prototypes and with simulations to avoid such an issue
  - Integration of back-up solutions in prototypes (ADC, frontend block)
  - Time to diagnose, correct and get new production may require 1 year, also costly
- Delay due to lack of manpower
  - Saclay: temporary contract proposed, with perspective to gain permanent contract
  - Sao Paulo: students hired to contribute on the project

QUALITY ASSURANCE

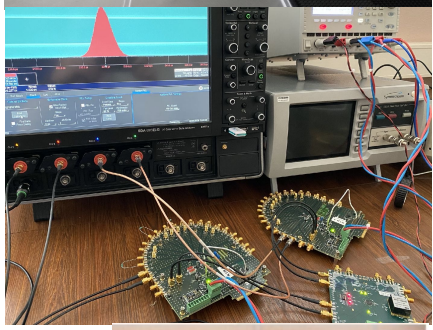
Expertise in large scale ASIC production

- In-house at Saclay: automated ASIC tester robot, test-benches
- In industry: development of turn-key test-benches
- Recent experience: 40k Rafael and 80k Catia ASICs produced and tested for CMS Ph2 upgrade



Test equipment

- At Saclay: high-end LeCroy and Textronic oscilloscopes
- High performance phase noise analyzer
- Low jitter precision clock sources
- Climate chamber
- Bonding machine



Test facilities

- Radiation facilities at Saclay, Sao Paulo, CERN and in Europe
- High magnetic field facilities at Saclay and CERN

Expertise

- System-level design, production and commissioning
- Readout electronics, acquisition software, analysis (CLAS12, T2K TPC, Asakusa tracker)
- Respect of ES&H regulations of host laboratories (BNL, CERN, JLab, J-PARC)

Charge 5

SUMMARY

SALSA development

- Considered solutions and architecture are realistic and would cover performance requirements
- Our groups have required experience to develop such an ASIC
- Manpower reinforcement ongoing to accelerate ASIC development
- Major steps ahead: test of SALSA1 prototype, development of SALSA2 DSP design

SALSA production

- 4000 SALSA ASICs to produce in 9 to 12 months
- Planned for 2027, compatible with the overall EPIC installation schedule
- May be delayed by 1 year in case of unexpected misbehavior of SALSA prototypes