# CALOROC for SiPM readout
# EIC calorimetry

**IPDR**
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Organization for Micro-Electronics desiGn and Applications

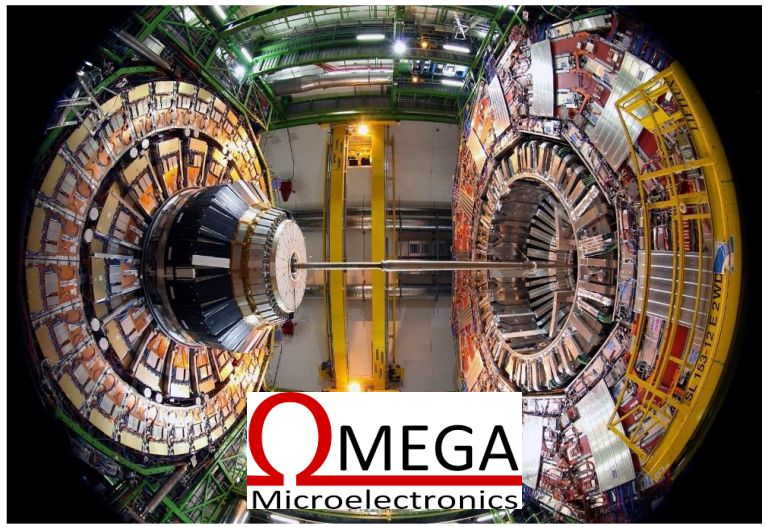
# From H2GCROC to CALOROC

H2GCROC for the endcap calorimeter – Phase II

6M of Silicon channels
(+ 240k of SiPM)

Radhard (200 Mrad)
Low Power (15 mW per chn)
Precise timing (25 ps)

Total of 150k ASICs needed
Pre-prod this year




CALOROC for EIC

Same ASIC structure (floorplan)
Same ADC and TDC
Same readout

Common interfaces

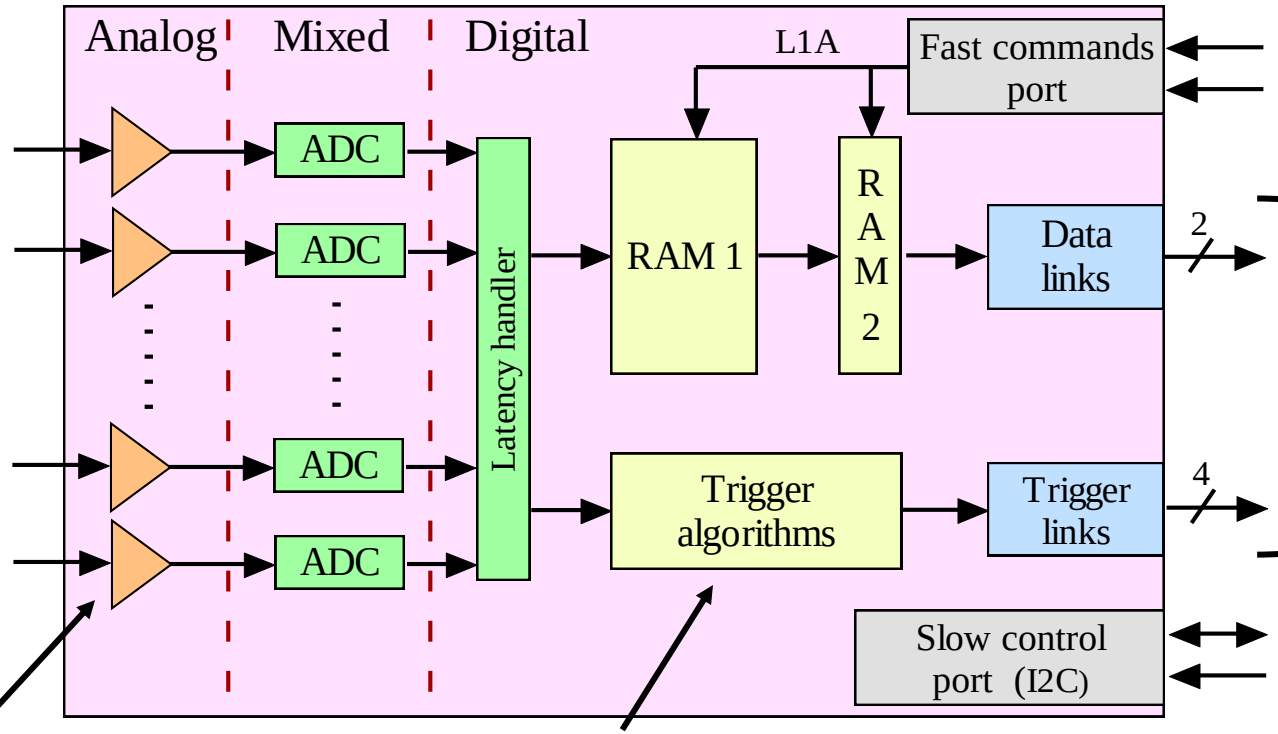
HEP trend => imaging calorimetry

- ❑ High number of channels
- ❑ Charge and precise timing (<100 ps)
- ❑ Low power + System-On-Chip

Based on H2GCROC, CALOROC will provide a versatile and low-power solution for SiPM readout

# ROC chips standard structure

- H2GCROC (for SiPM readout) is an HL-LHC colored ASICs (external L1 trigger)
  - Below is an calorimetry structure (but interfaces for CALOROC will similar)




Dedicated fast command interface : calibration pulses, external L1 trigger.

Data and trigger serial links with CLPS signaling (LpGBT @ 1,28 Gbps)

Analog front-end specific to sensor

LHC-like structure :
Ram1 for data storage
Ram2 for L1 accepted events

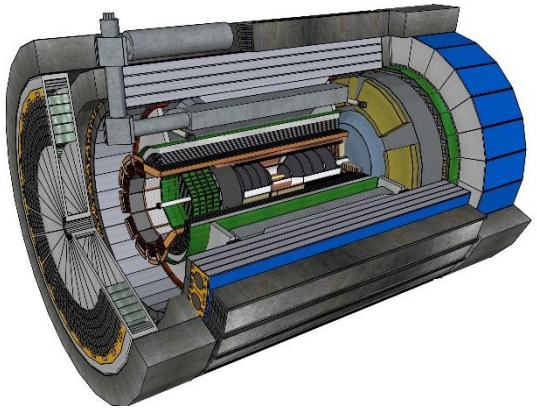
I2C interface to load the ASIC parameters (slow control interface)

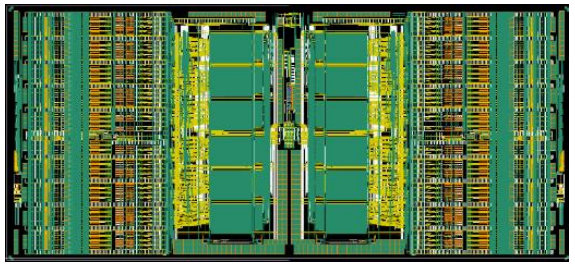
# What is CALOROC ?

- CALOROC will be available in 2 versions for SiPM readout:
  - SiPM range capacitance from 500 pF to 10 nF
  - ~ 10 mW / channel
  - Radiation hardening (HL-LHC levels)
    - 200 Mrad and $10^{16}$ $n_{eq}$ / $cm^2$ (1 MeV equivalent neutrons)
    - SEE hardening on control logic
  - Charge and time measurement
  - Max triggering rate of 50 kHz / chn

- Conservative CALOROC1A based on CMS H2GCROC:
  - H2GCROC (ADC, TOT) analog/mixed reuse
  - Back-end compatible with EIC + zero-suppress

- New CALOROC1B based on gain switching:
  - New analog part without TOT (dynamic gain switching)
  - Backend « à la HKROC »: auto-trigger, zero-suppress – EIC compatible







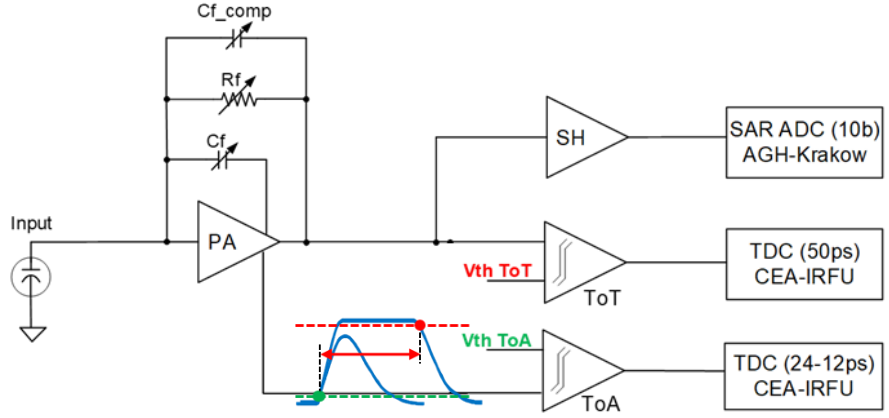
CALOROC 1A
CMS front end
EIC readout

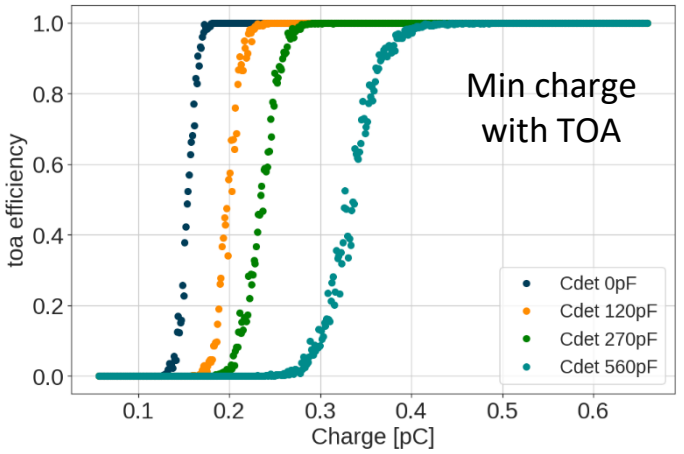
CALOROC 1B
New front end
EIC readout

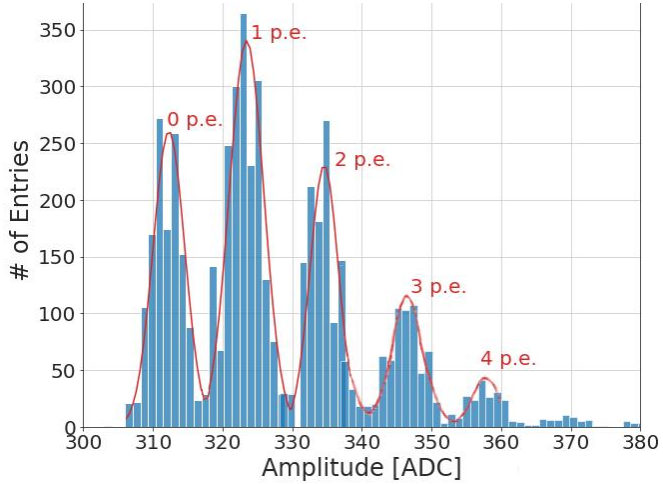
CALOROCs will share a common backend
+ pin-pin compatibility

# CALOROC1A (based on H2GCROC)

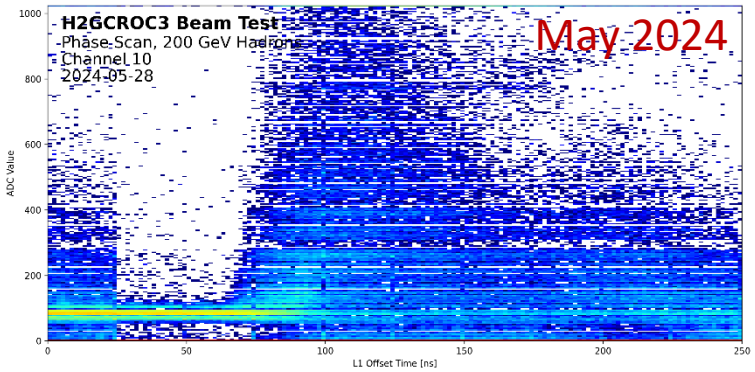
- Reuse of analog front-end based on ADC/TOT and TOA: fully characterized *
  - 15 mW per channel / Radiation performance / SiPM range 100-600 pF

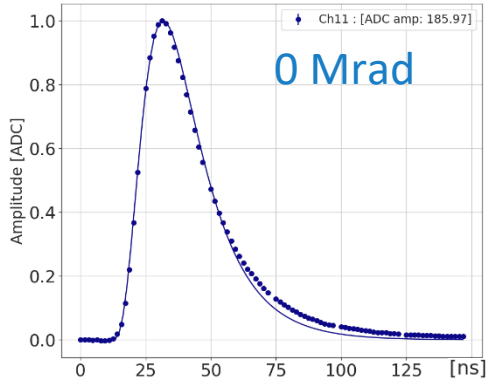


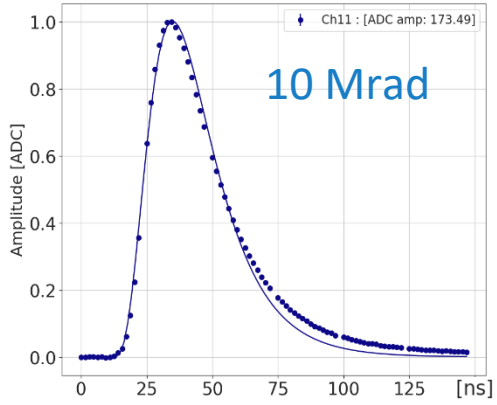




- H2GCROC already evaluated by ORNL for EIC calorimetry

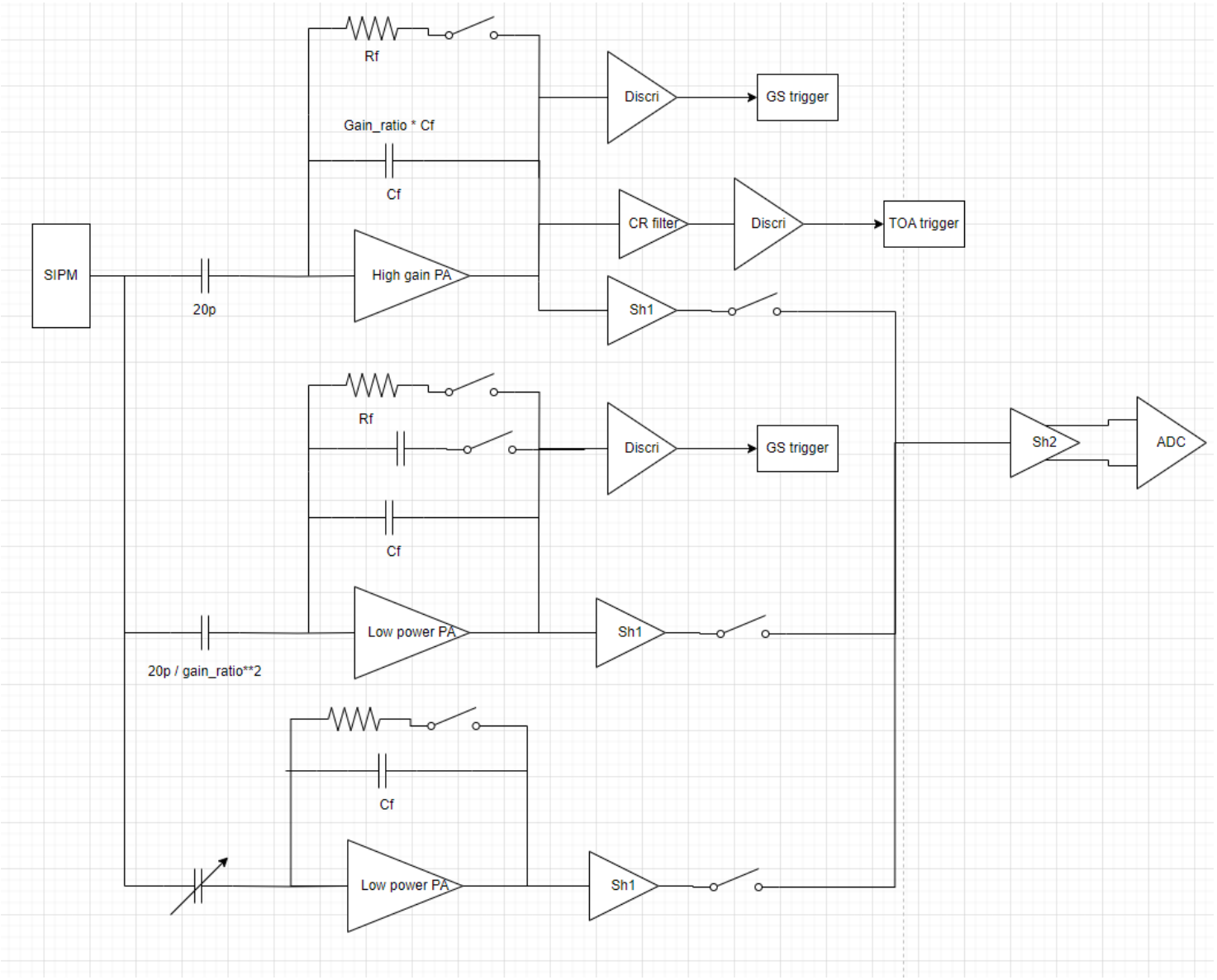

- CALOROC1A will only update its back-end to be EIC compatible

* TWEPP 2023 ➔ https://edms.cern.ch/document/2954073/1

Charge 2, 3

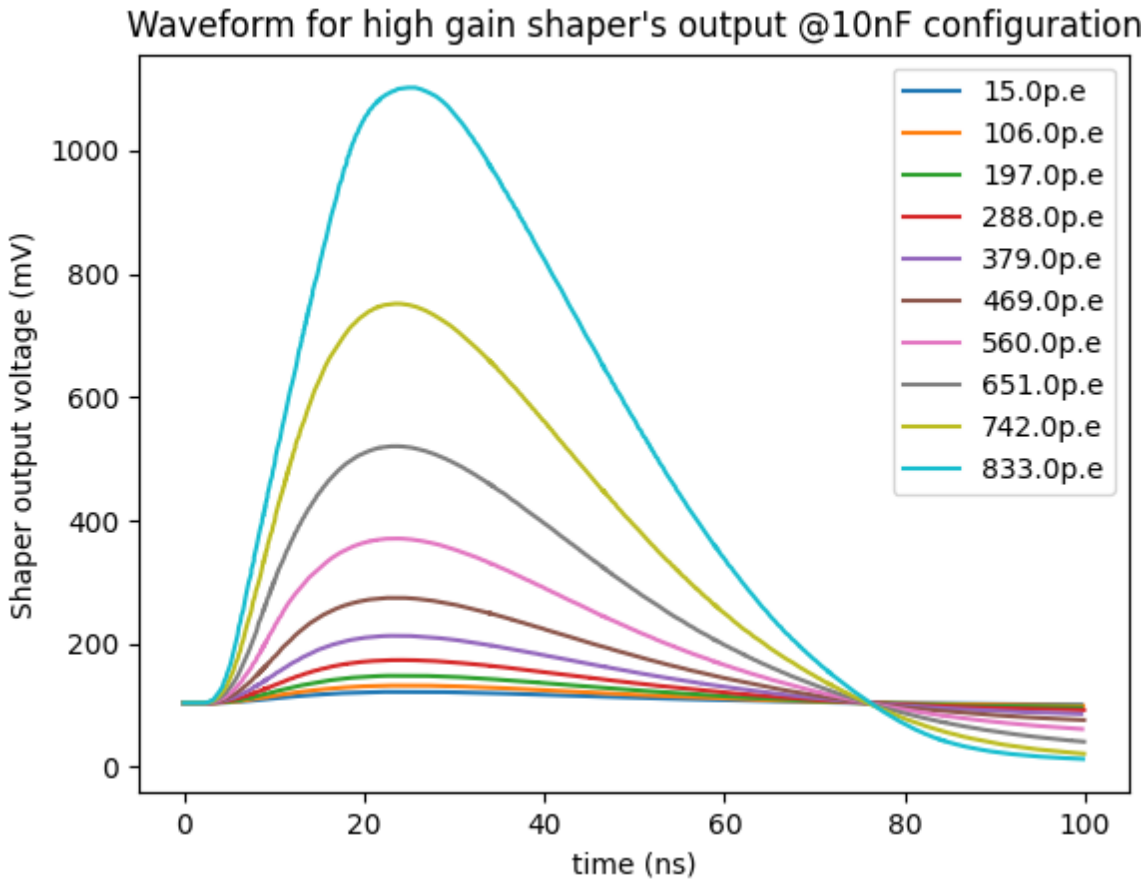
# CALOROC1B: Chosen architecture [P. Dumas]

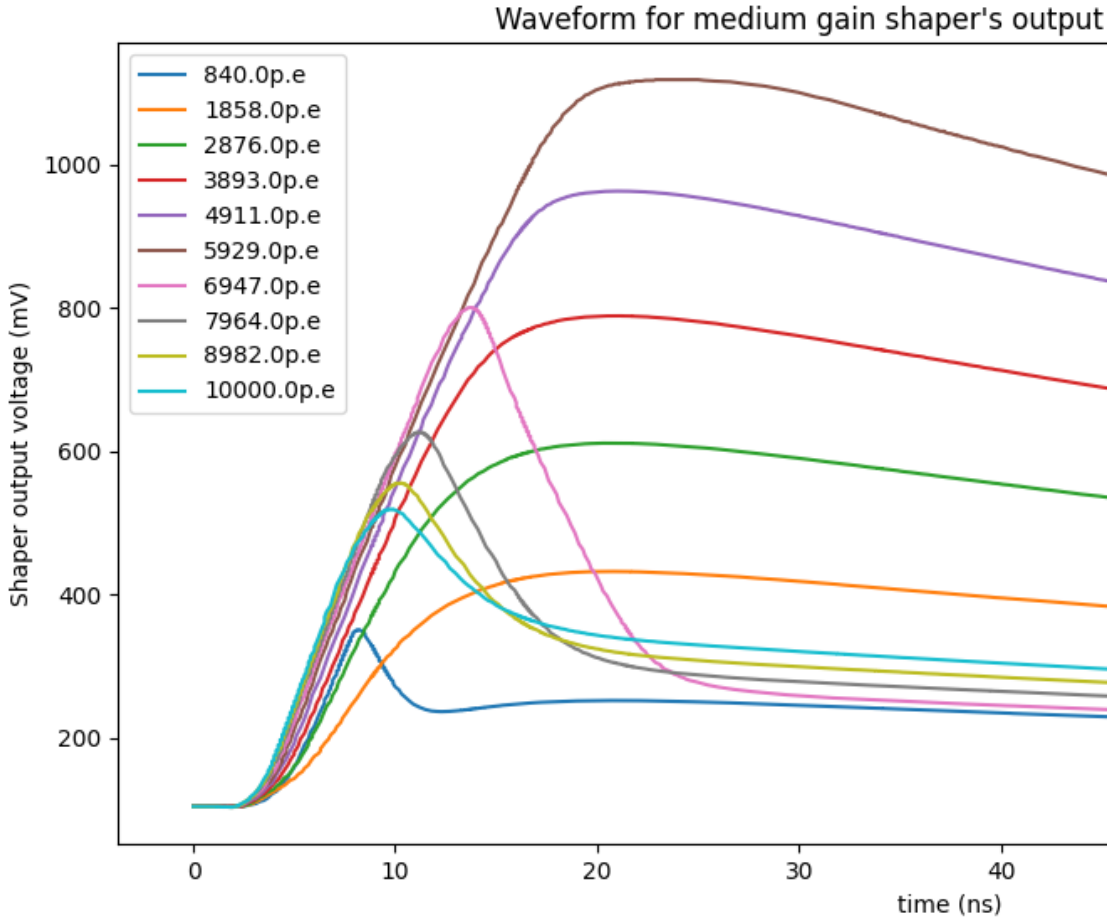
- New dynamic frontend with switched gain:
  - High gain
  - 2x medium gain
  - Low Gain
- Reuse CMS-H2GCROC ADCs and TDCs:
  - 10-bit 40 MHz ADC (Krakow)
  - 25 ps TDC (Saclay)
- Shared CALOROCs backend
- Common specifications:
  - SiPM from 500 pF to 2.5 - 10 nF
  - ~ 10 mW/channel
  - CMS HL-LHC Radiation level 200 Mrad



# CALOROC1B: Charge and time simulations

- Waveform for HG on the left + gain switching on the right:
  - Example with Cd of 10 nF

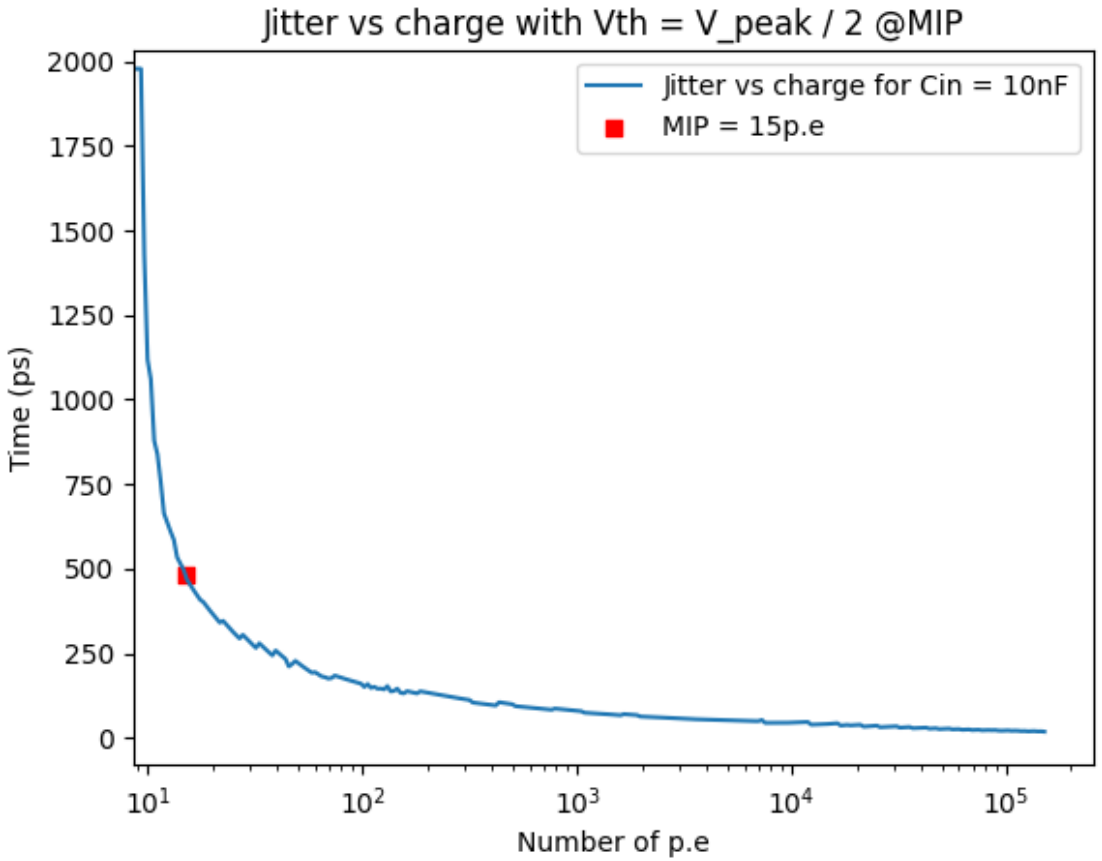


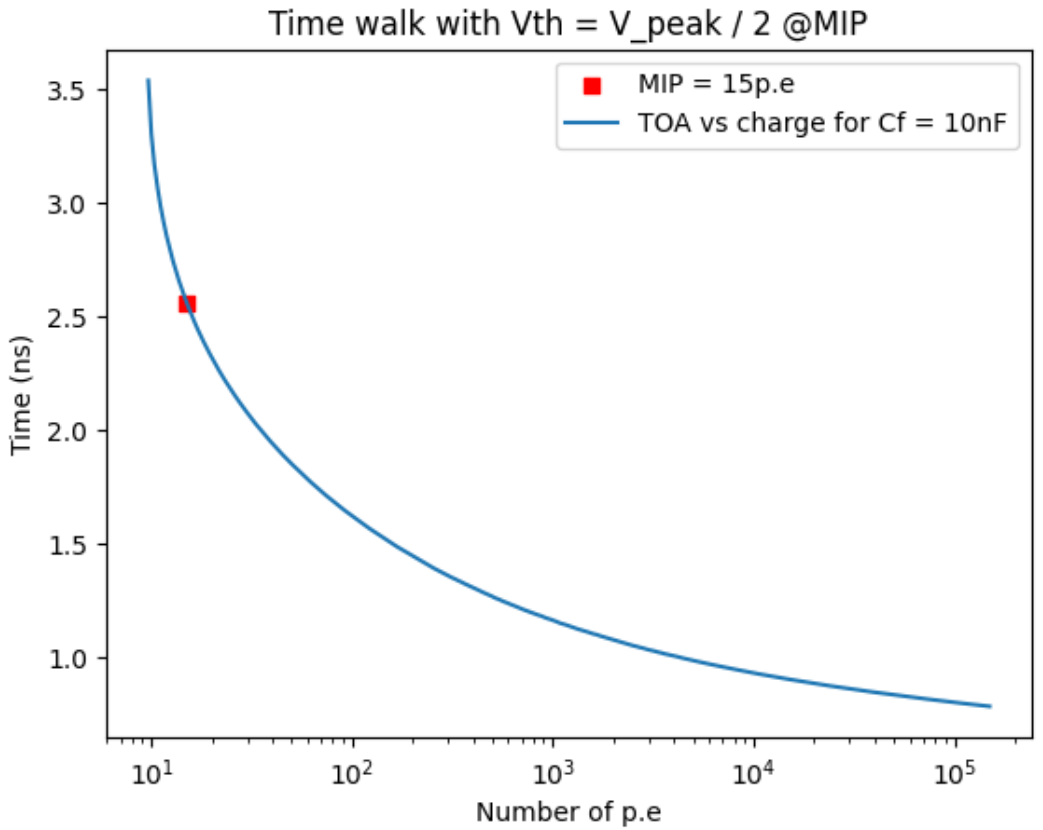



# CALOROC1B: Timing precision

- Simulated time jitter goes down to 20 ps with < 500 ps for the MIP

- Time walk is below ~2,5 ns (equivalent to the value of CMS H2GCROC)



# CALOROC1B: SiPM vs SNR

- The SiPM configuration has a direct impact on the SNR
  - SNR for 1p.e is proportional to Q/C (larger SiPM cap decrease SNR)
  - Gain of 1.8e5 electrons per p.e (table below)

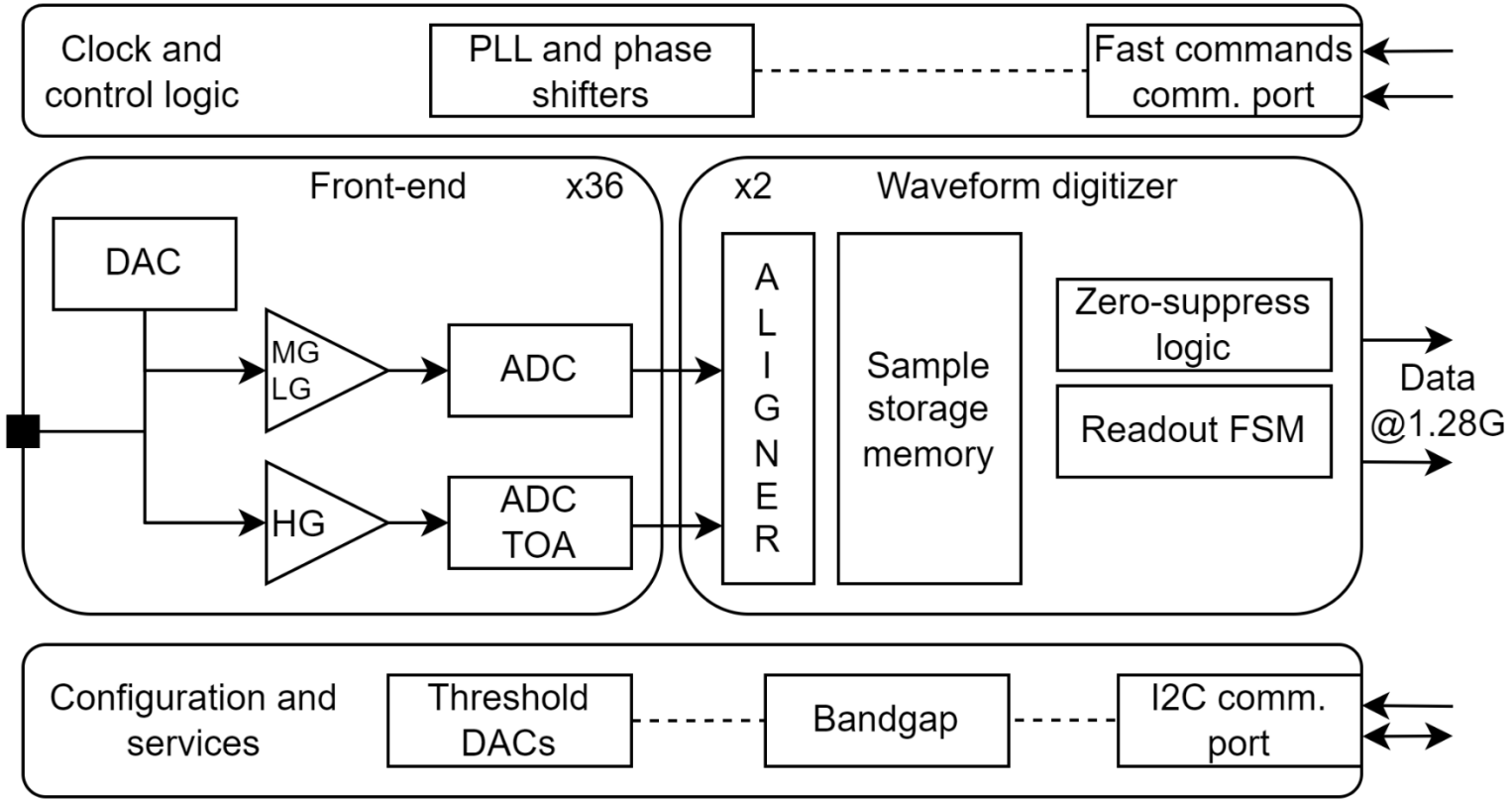
- CALOROC1b will be able to readout SiPM in the range ~ 500 pF to 10 nF
  - Timing measurements will focus on the MIP (~15pe)

| Operation modes | 1 SiPM of 530pF | 1 SiPM of 2.5nF | 4 SiPM of 2.5nF |
|---|---|---|---|
| Cin | 530pF | 2.5nF | 10nF |
| SiPM config gain ($\mu$V/p.e or Q/C) | 13.58$\mu$V | 11.52$\mu$V | 2.88$\mu$V |
| Dynamic range (in p.e) | 22.79k | 107.5k | 430k |
| Dynamic range (Charge) | 656pC | 3.1 nC | 12.3nC |
| Jitter @ 1p.e | 390ps | Not measurable | Not measurable |
| SNR @ 1p.e | 10 | 2.13 | 0.53 |

SiPM: S14160-3010PS 3x3mm (530pF) / S14160-6010PS 6x6mm (2.5nF)

# CALOROCs: block diagram and interfaces

- CALOROCs will have the same interfaces (comparable to CMS H2GCROC *):
  - Fast command to dynamically control the ASIC
  - I2C to set the parameters
  - High speed serial links (**C**ern**L**ow**P**ower**S**ignal compatible)




| Fast commands | Value |
|---|---|
| Idle | 00011 |
| External trigger | 01101 |
| ChipSync | 01110 |
| BCR | 10101 |
| EBR | 11001 |
| Link-sync-ROC or Link-reset-ROC | 10110 |
| Calibration int or ext | 11010 |

CALOROC

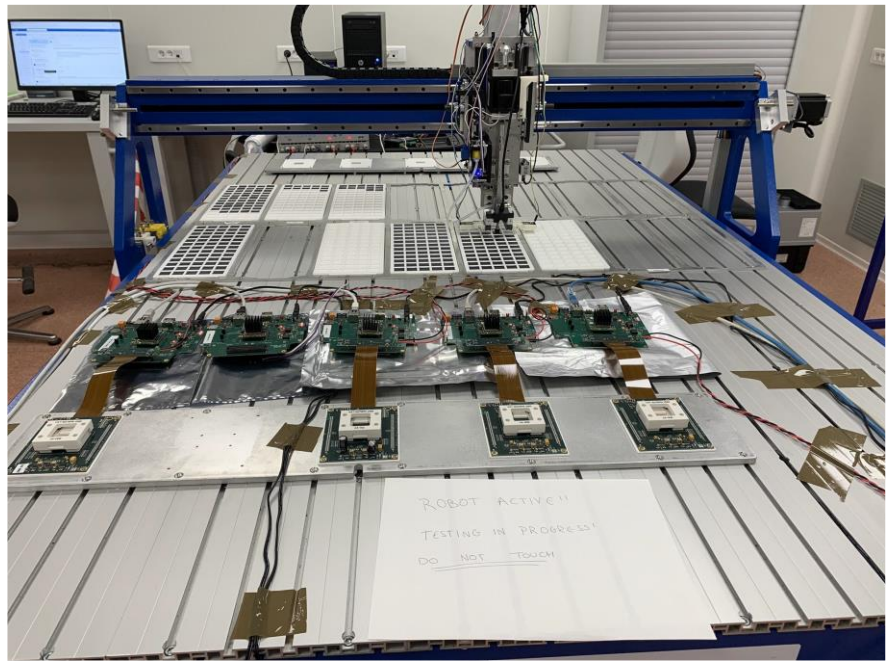
| | | | | |
|---|---|---|---|---|
| 4b-data Header | 2b Mode | Dh | 24b Timestamp | 1 |
| 4b-data Header | 8b 0 | Dh -d | Dh -h | 18 channels Hit map |
| 2b Gain | 10b $ADC_{-1}$ - HG or 0s | 10b ADC 3-gain or 4-gain | | 10b TOA |
| 2b Gain | 10b $ADC_{-1}$ - HG or 0s | 10b ADC 3-gain or 4-gain | | 10b TOA |
| ⋮ | | | | |
| 2b Gain | 10b $ADC_{-1}$ - HG or 0s | 10b ADC 3-gain or 4-gain | | 10b TOA |
| CRC | | | | |
| Idle/Sync Header | 28b default IDLE Pattern | | | |

* CERN EDMS ➔ https://edms.cern.ch/document/2954073/1

Charge 2, 3

# Quality assurance and time line

- Expertise in radiation-hardened front-end ASICs for HEP
  - HL-LHC ASICs: ATLAS HGTD and CMS HGCAL ($10^5$ ASICs)
- Expertise in irradiation testing (dose and displacement)
  - HL-LHC levels 200 Mrad and $10^{16}$ $n_{eq}$ / $cm^2$ (1 MeV equivalent neutrons)
- Standard interfaces ensures a full compatibility with our robot
  - 2x 50 ASICs tested per hour (H2GCROC) with QR code scan
- CALOROC timeline – 2024 to 2027
  - End 2024, CALOROC1s submission (Eng. Run)
  - 2025, packaging, performance tests and DAQ validation
  - 2025-2026, irradiation tests and CALOROC2s preproduction (final ASIC/package)
  - (If chosen, possible CALOROC3B extra submission end 2026)
  - Q1 (Roc1A) or Q3 (Roc1B) 2027 production and robot tests

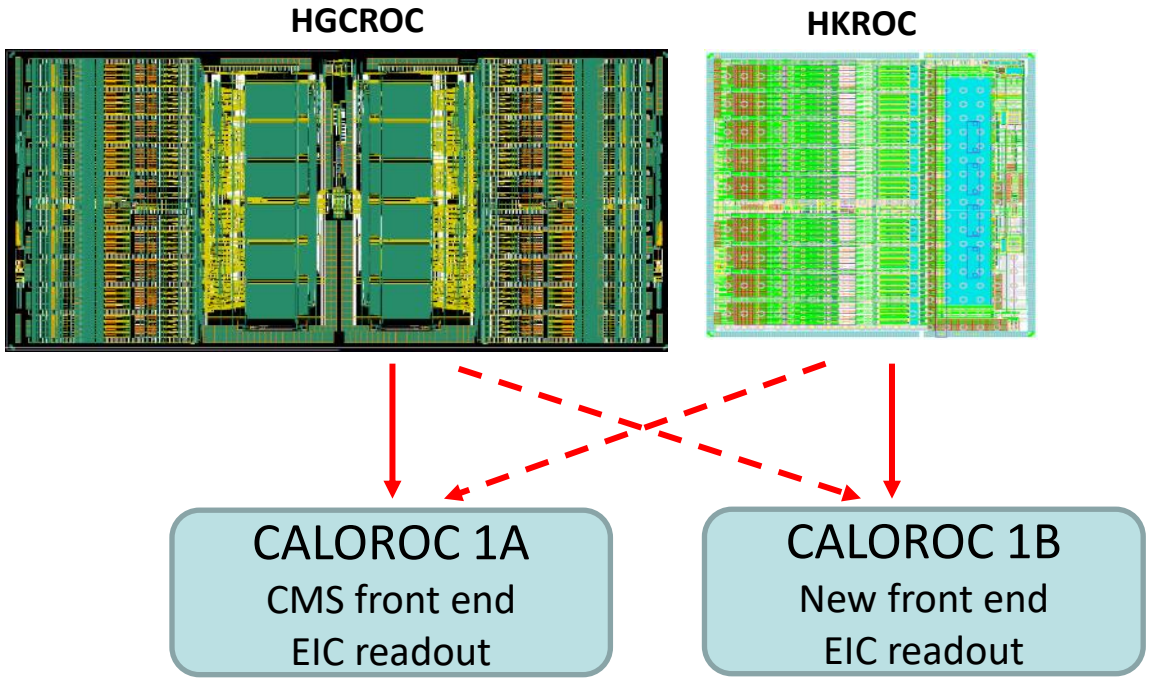




Charge 4, 5

# Conclusion

- Both CALOROC will be submitted by the end of 2024 (common fabrication run)
- 2 new designers joined OMEGA for CALOROC
  - 1 PhD in 2023 + backend designer in March 2024
- Conservative **CALOROC1A**: analog and mixed part finished
  - Shared CALOROCs backend under simulation
- New **CALOROC1B**: Analog and mixed architecture frozen
  - Analog and mixed part finished
  - Shared CALOROCs backend under simulation
- CALOROCs will be compatible with CMS test robots




CALOROCs are targeted to include all features + radiation hardness on the first submission

# backup

# Common: Fast commands for EIC

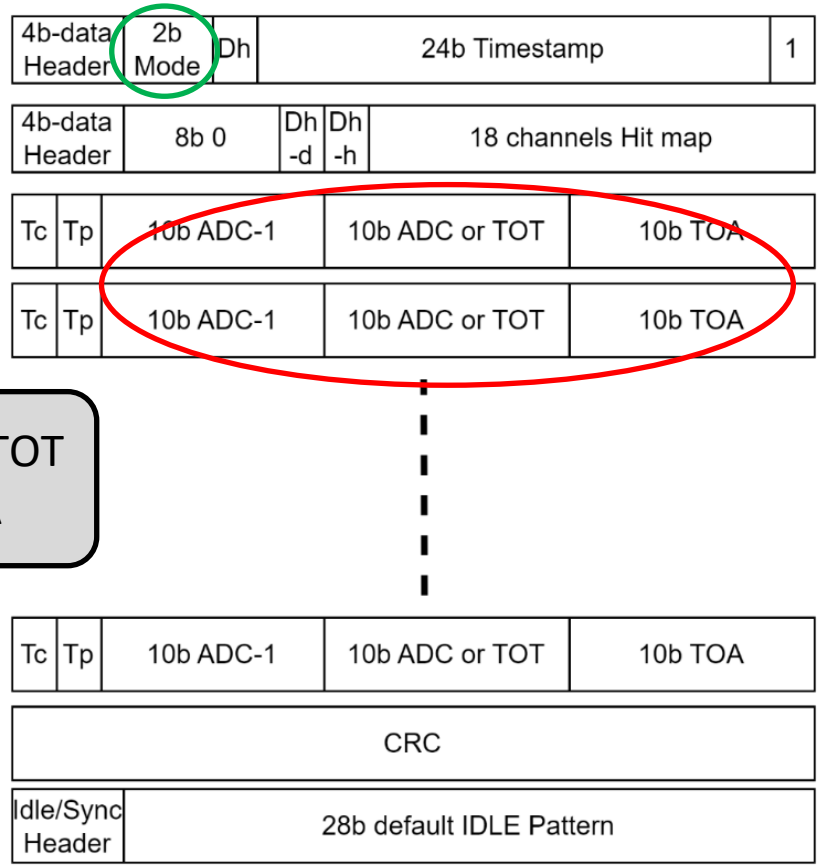
- Internal clock generator + external fast commands (x2 EIC clock bitstream, x2/5 internal clock)
  - 5 unique fast commands
  - 2 dual uses (link + calibration): 1 or 2 consecutive FC
  - Not included: 3 dedicated FC for parameters (I2C emulation) + 1 spare

| Fast commands | Value | Description | Comment | Possible back to back | HD to IDLE |
|---|---|---|---|---|---|
| Idle | 00011 | Default, 40M phase inside | ~99% of the time | Y | 0 |
| External trigger | 01101 | Pedestal measurement | For calibration | Y | 3 |
| ChipSync | 01110 | Fast digital only reset | Only when problems | N | 3 |
| BCR | 10101 | Load default value (parameter) | Real time operation | N | 3 |
| EBR | 11001 | Empty readout buffers | Free all internal memories | N | 3 |
| Link-sync-ROC or Link-reset-ROC | 10110 | Send sync pattern (x400) or Internal serial link reset | Link sync procedure or Link bit shift recovery (PLL SEE) | Y (1 or 2) | 3 |
| Calibration int or ext | 11010 | 800 ns or 100 ns calib pulse | | Y (1 or 2) | 3 |
| SC0 | 00101 | Send SC bit 0 | To built R or W frame | Y | 2 |
| SC1 | 01001 | Send SC bit 1 | To built R or W frame | Y | 2 |
| SC_Valid | 01010 | Validate action | Validate if frame + ID are valid | Y | 2 |
| Spare1 | 10010 | | | Y | 2 |

# CALOROC readout frame - WIP

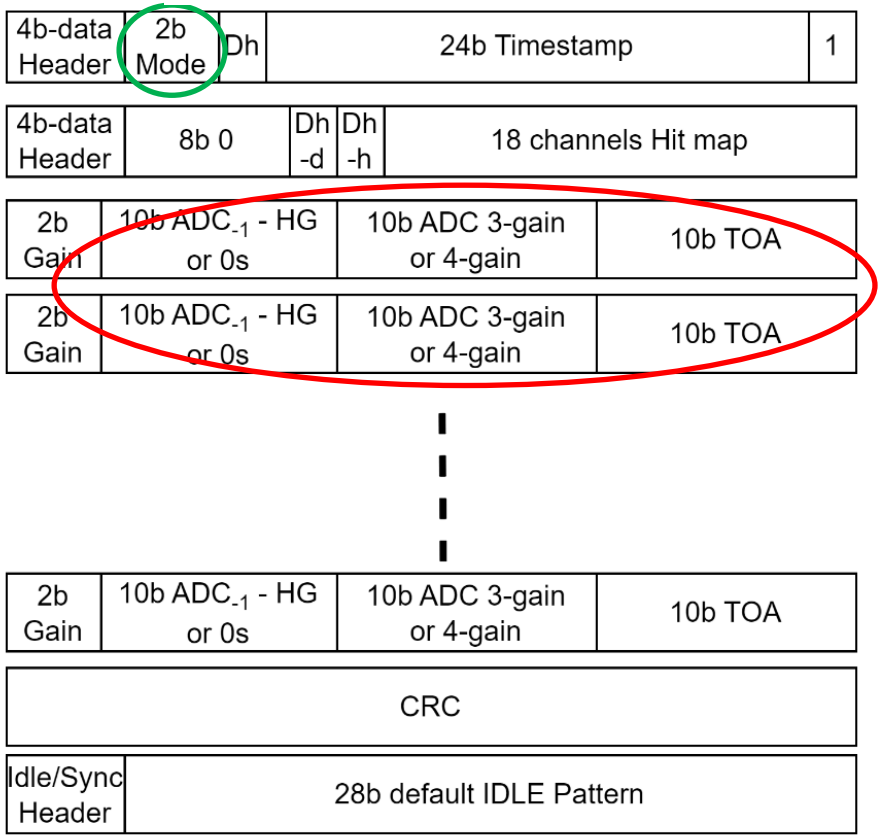
- Common to both CALOROC

## CALOROC1A – similar H2GCROC



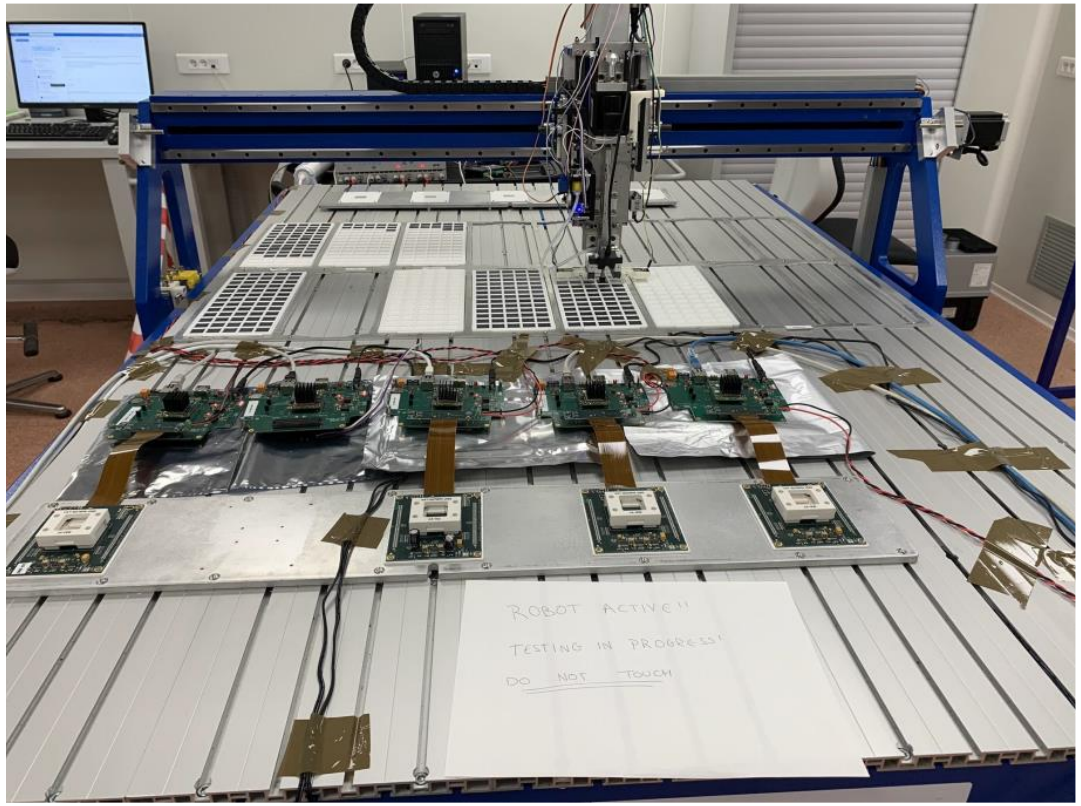

ADC – TOT TOA

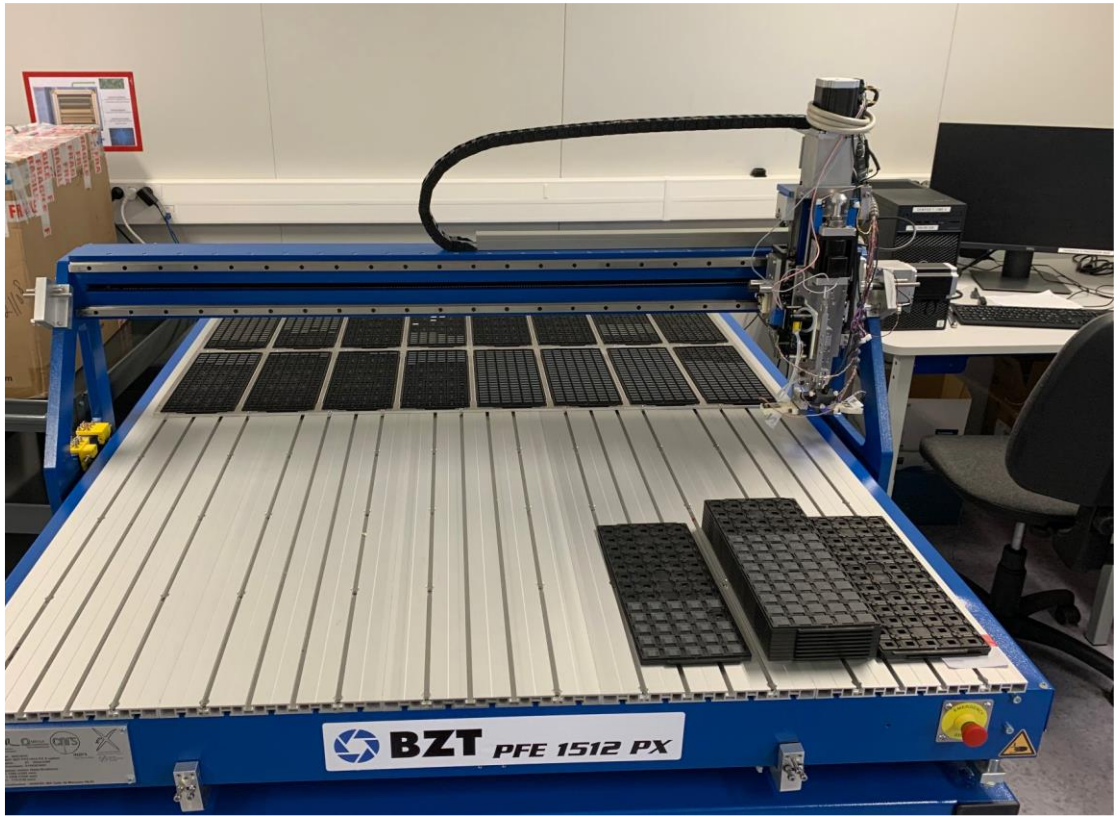
## CALOROC1B – no TOT




4-gain ADC TOA

# Robots


ROBOT ACTIVE!!
TESTING IN PROGRESS!
DO NOT TOUCH


BZT PFE 1512 PX

# EIC: CLPS signaling (LpGBT documentation)

- Used for fast commands, clock and output data links in ROC chips

- Link types:
  - Point-to-point;
  - Multi-drop transmitter.
- Maximum data rate:
  - 1.28 Gbps (NRZ signalling).
- Maximum clock frequency:
  - 1.28 GHz.
- Programmable signalling level:
  - 100 mV to 400 mV (single-ended amplitude);
  - 200 mV to 800 mV (differential amplitude).
- Common mode voltage:
  - 600 mV (nominal, for 1.2 V supply voltage).
- Load impedance:
  - 100 Ohm differential.