Istituto Nazionale di Fisica Nucleare

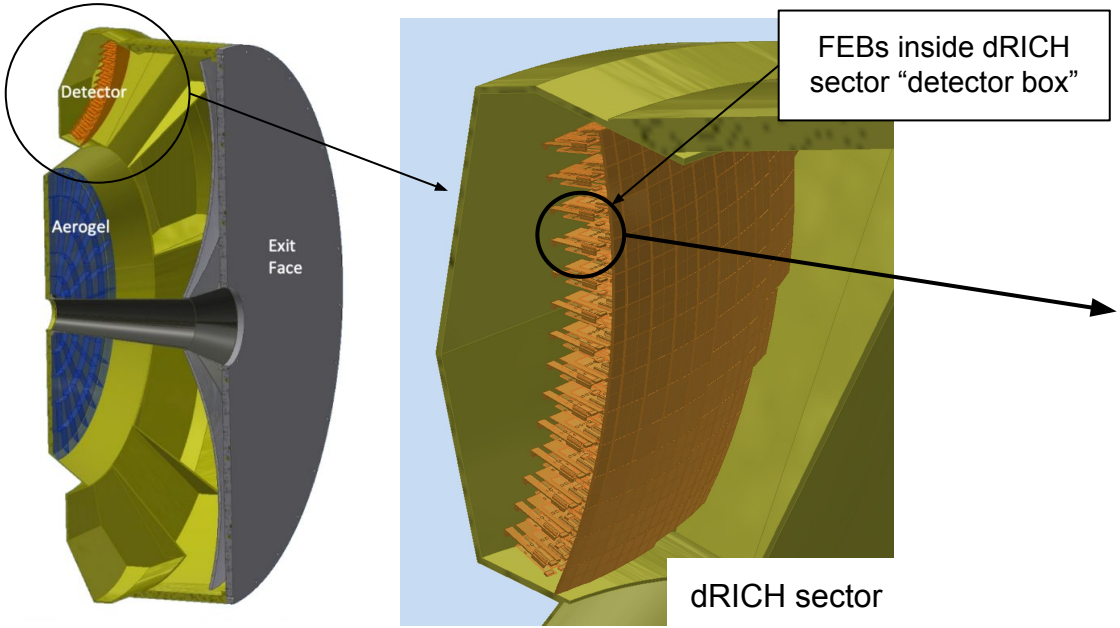
with DoE/eRD109 support

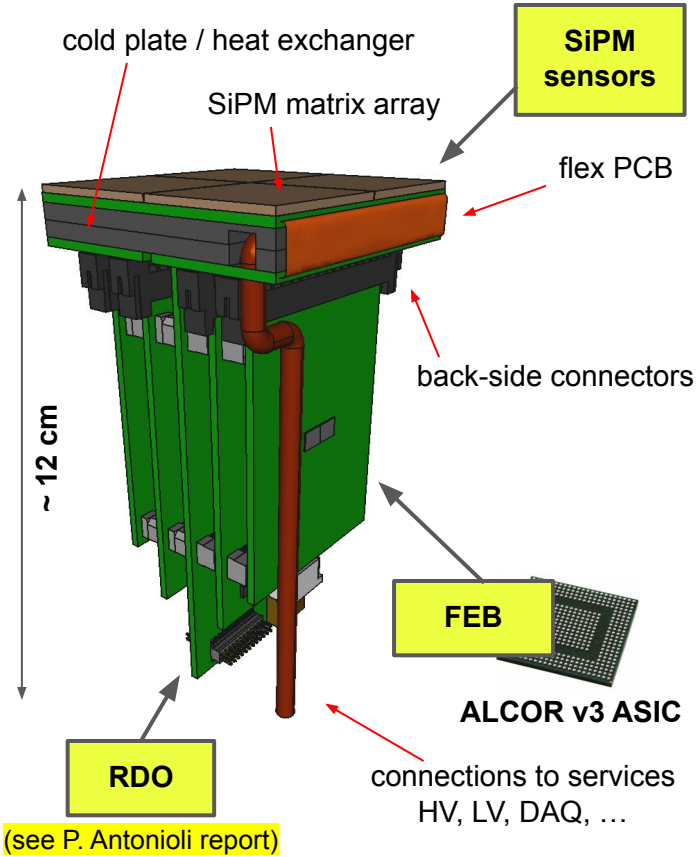
The ALCOR ASIC for the dRICH Detector

Fabio Cossio (INFN Torino)
on behalf of the dRICH Collaboration

Incremental Preliminary Design and Safety Review of the
EIC Detector DAQ and Electronics - 10th June 2024

Requirements: space and number of channels





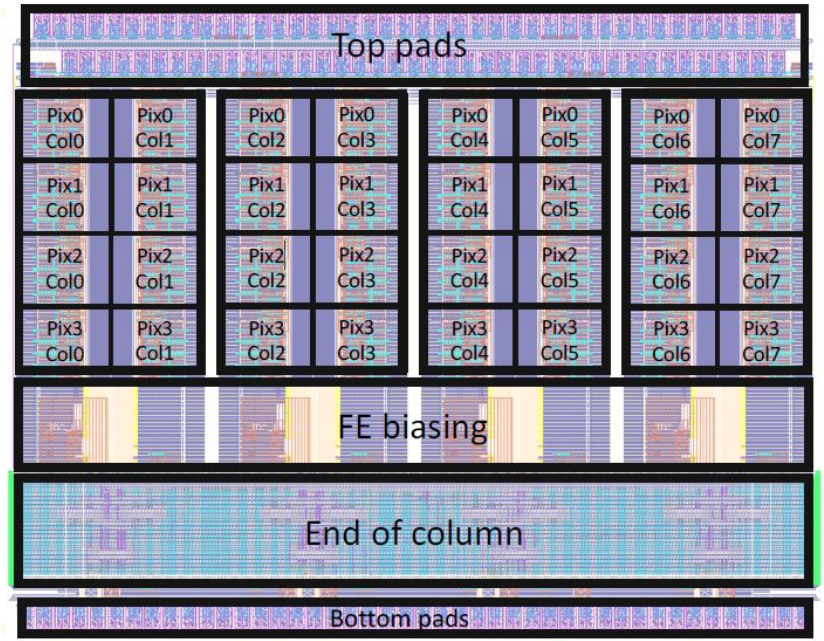
- **1 PDU**: 4x64 SiPM array device (256 channels), **4 FEBs, 1 RDO**
- **1 ALCOR** (64 channels) per **FEB:** 8x8 SiPM matrix readout
- 1248 PDUs for full dRICH readout
- **4992 FEBs → 4992 ALCOR v3**
- **319488 readout channels**

Requirements: SiPM readout with single-photon sensitivity

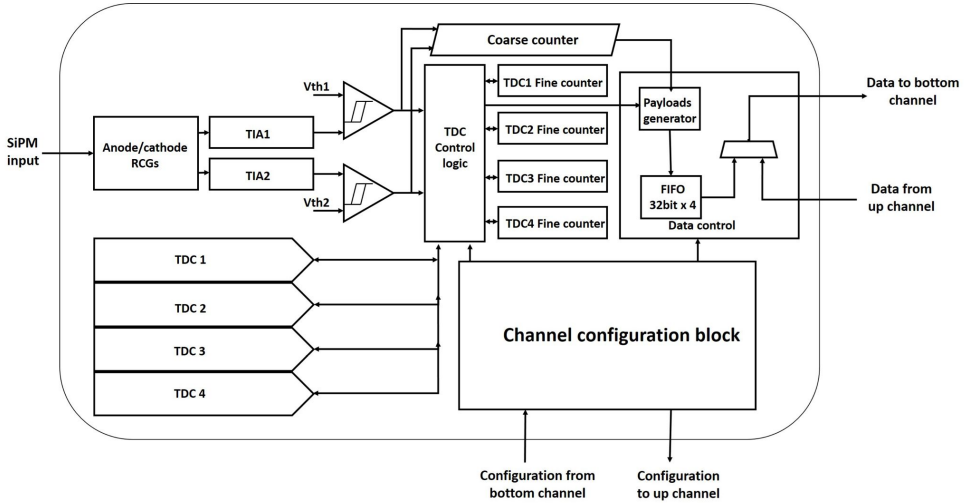
- ALCOR must provide **single-photon time tagging** of signals coming from SiPM sensors
- ALCOR must cope with **SiPM DCR: 300 kHz/channel** (at max SiPM radiation damage)

ALCOR: A Low Power Chip for Optical Sensor Readout

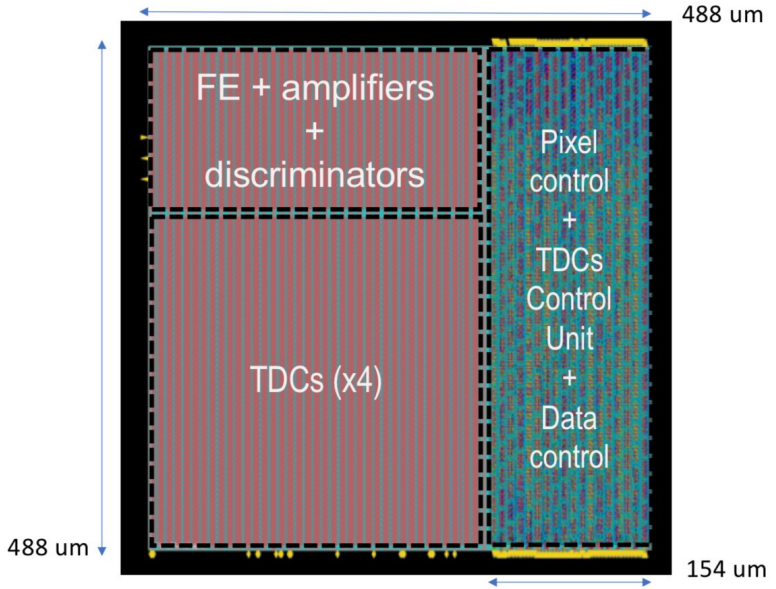
- **32-pixel** matrix (8x4) mixed-signal ASIC (4.95 mm × 3.78 mm), new version will be **64-pixel** matrix (8x8)
- Single-photon time tagging + **Time-over-Threshold** or **Slew-Rate** measurements for time walk correction
- On-chip **signal amplification**, **conditioning** and **digitization**, 32-bit event word
- Fully digital output: 4 LVDS 320 MHz DDR Tx links
- Power consumption **~10-12 mW/channel**
- 0.11 μm CMOS technology



Implementation: pixel architecture



pixel size: 440 x 440 μm^2



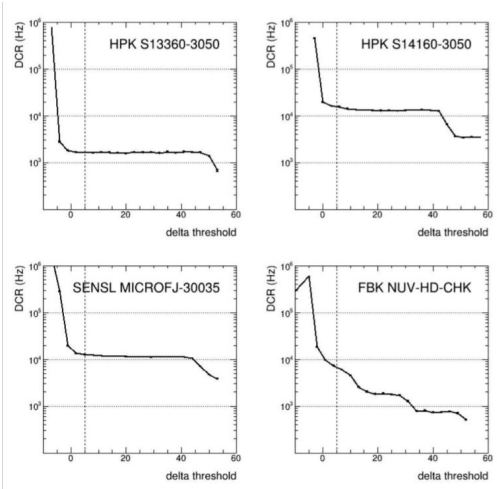
- **RCG input stage** current conveyor (Z_{in}= 10-20 Ω)
- **2** independent **TIA branches** with 4 gain settings
- **2 leading edge discriminators** with independent (and per pixel) threshold settings (6-bit DAC)
- **4 TDCs** based on **analogue interpolation** with 25-50 ps time-bin (at 320 MHz clock frequency)
- Pixel control logic handles TDC operation, pixel configuration and data transmission

Reminder: ALCOR v1

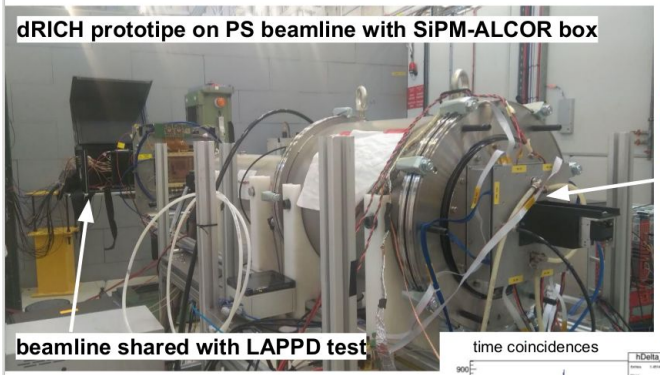
Developed by INFN for the readout of SiPMs at 77K, in the framework of Darkside (Dec 2019)

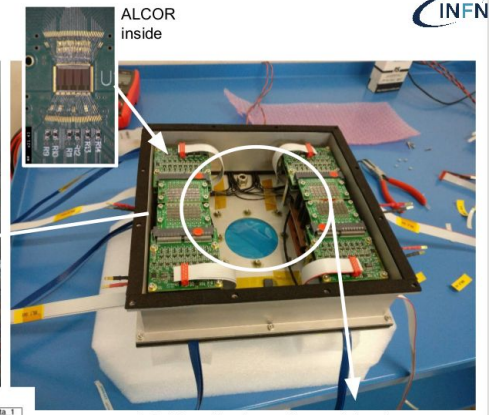
- Pixel matrix layout to explore solutions towards the development of an active silicon interposer for the integration of large area SiPMs for future massive frontier LAr Dark Matter Experiments

Extensively used within the EIC dRICH Collaboration during 2021-2022

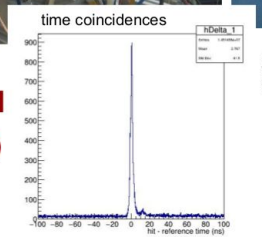


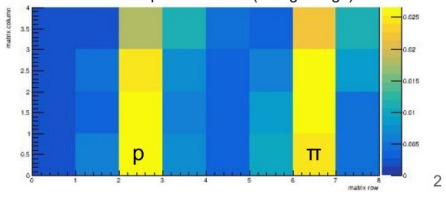
2022 test beam at CERN-PS





successful operation of SiPM irradiated (with protons up to 10^{10}) and annealed (in oven at 150 C)





Reminder: ALCOR v2

ALCOR v2

- MPW, submitted in Dec 2022
- 60 chips, received in June 2023
- Includes new features targeted for EIC dRICH and bug fixes:
  - ✓ TDC logic critical error at high rates solved also for DCR rate at room temperature
  - ✓ New FE gain settings more suited for single photon applications
  - ✓ On-chip test-pulse also for EIC SiPM polarity
- Successfully validated in 2023 beam test

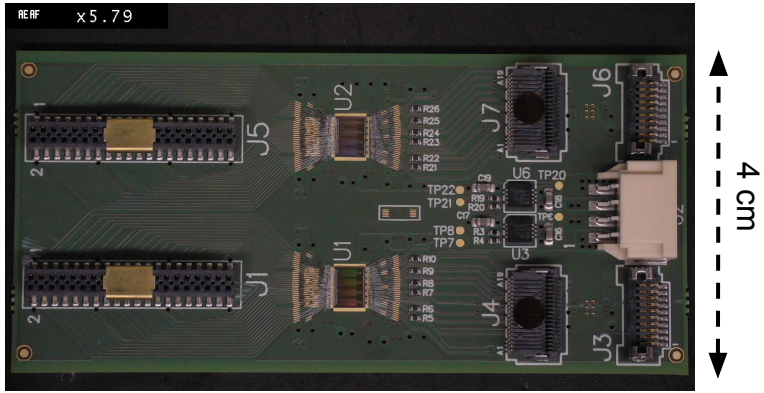
ALCOR v2.1

- INFN internal engineering run, chips received in Jan 2024
- Includes small bug fixes w.r.t. ALCOR v2
- Very high number of chips available to increase instrumented area for dRICH prototype and assemble other test setups
- Version currently used: beam test (May-June 2024) to validate ALCOR-based dRICH readout and evaluate its performance

Implementation: dRICH prototype readout system

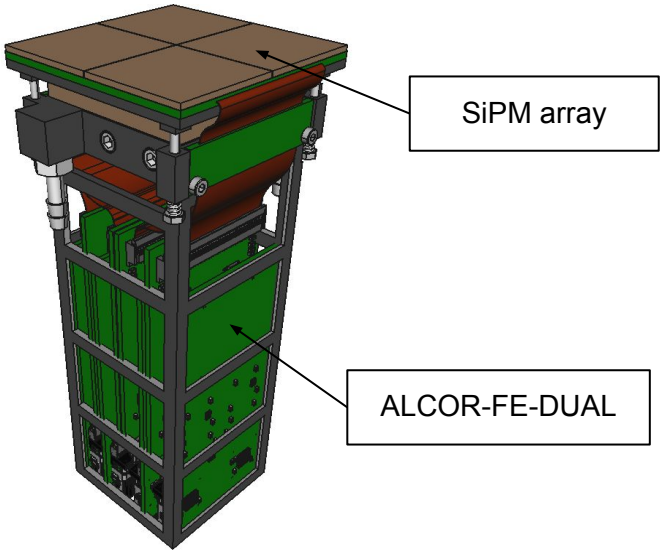
ALCOR-FE-DUAL

- Two **32-channel** ALCOR ASICs **wire-bonded** on the PCB
- **4 ALCOR-FE-DUAL** boards for each PDU (**256 channels**)
- System used for **2023-2024** ePIC dRICH beam tests



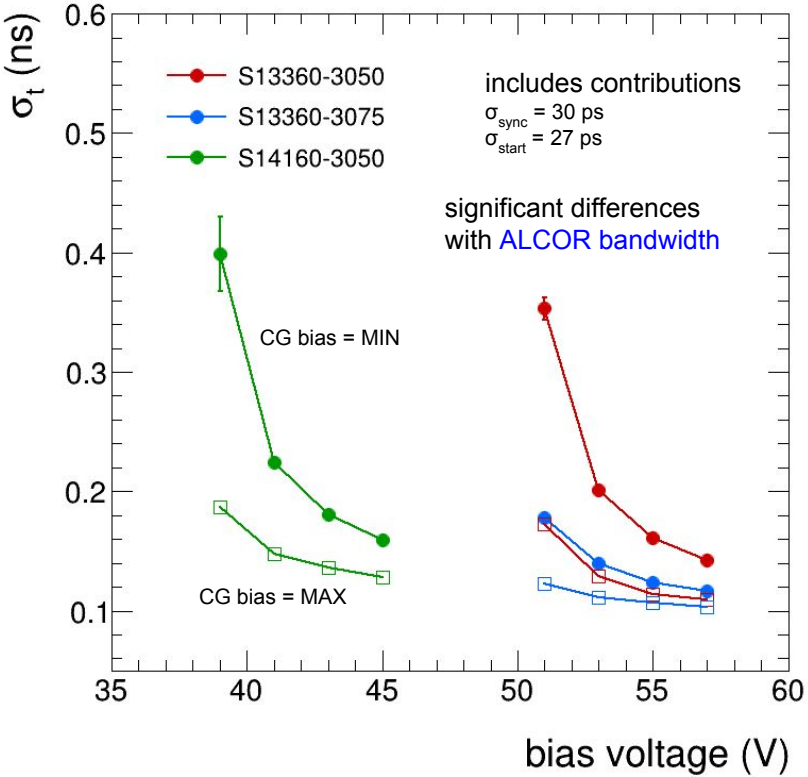
Designed using specifications close to final FEB: very similar space constraints and same number of channels (64)

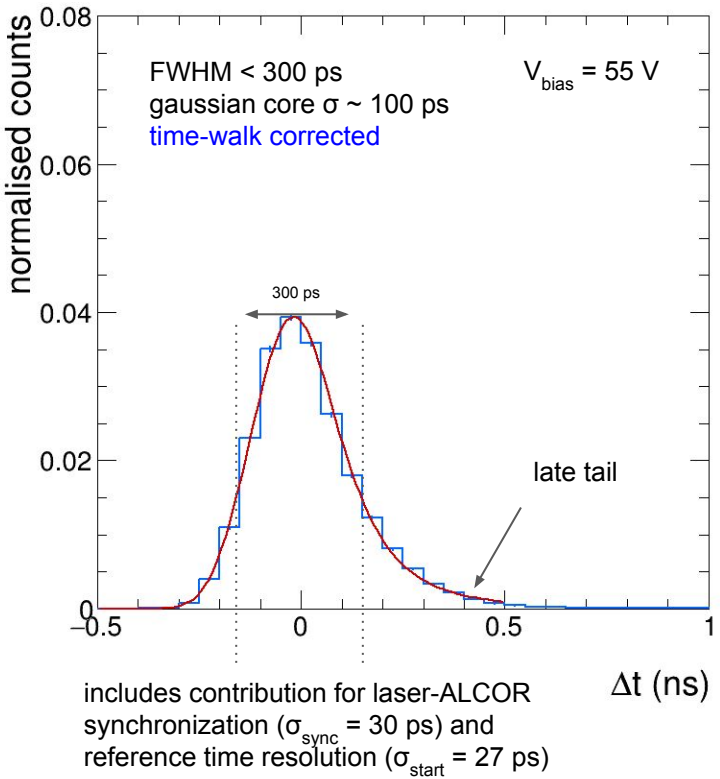
ePIC dRICH Prototype photodetector unit (PDU)



Prototype to test and validate PDU geometry and functionality (no RDO)

Performance: laser timing measurements



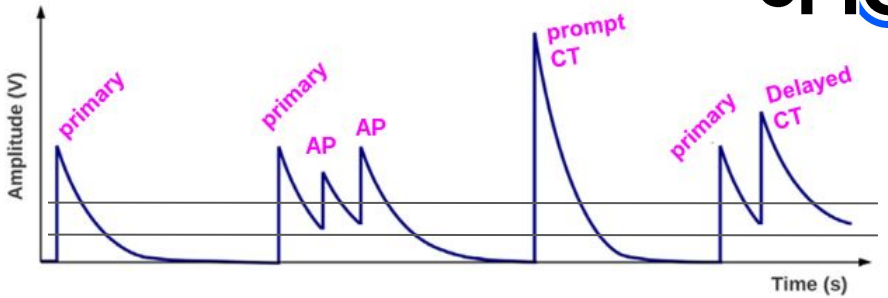


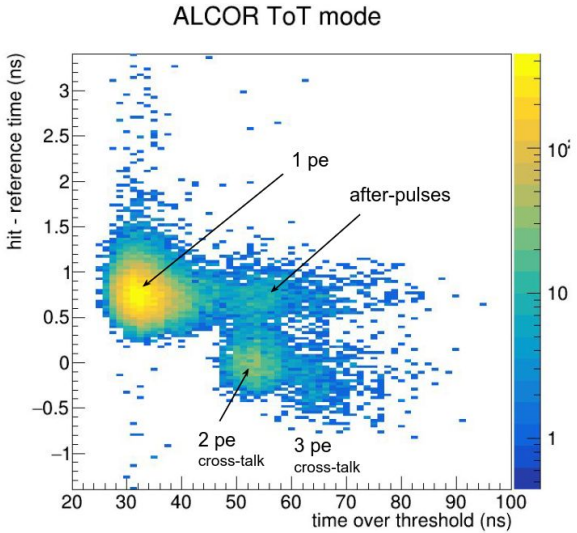
includes contribution for laser-ALCOR synchronization (σ_{sync} = 30 ps) and reference time resolution (σ_{start} = 27 ps)

- ➔ Better time resolution with **75 µm SPADs**
- ➔ Comfortably below **σ_t = 150 ps** also at low Vbias

Time walk correction

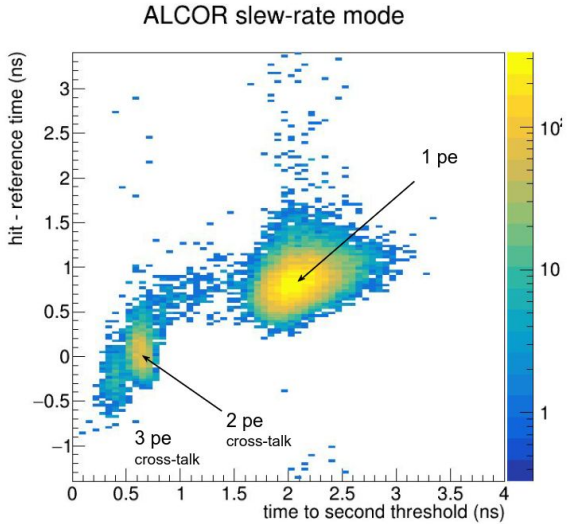
Time walk correction needed to improve overall time resolution → studies with laser setup using ***ToT*** and ***SlewRate*** measurements





✗ ***ToT mode*** cannot distinguish between afterpulses (slow-rise time, large ToT) and cross-talk (fast rise-time, large ToT)

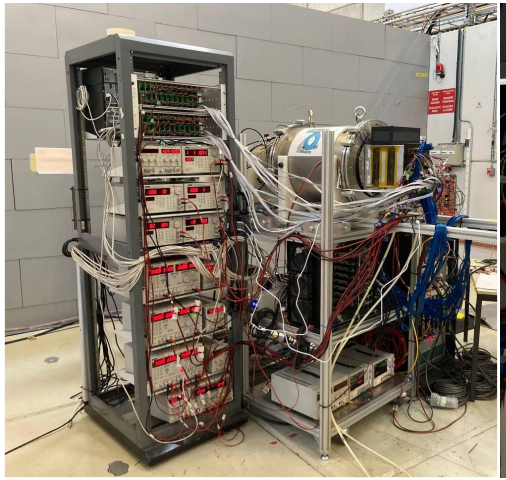
✓ ***SR mode*** provides better separation

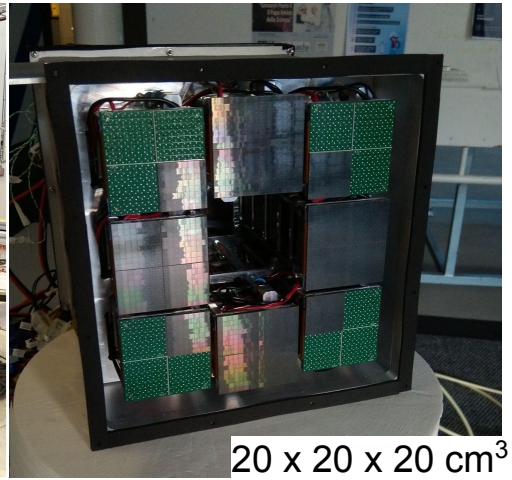


Performance: 2023 test beam at CERN-PS

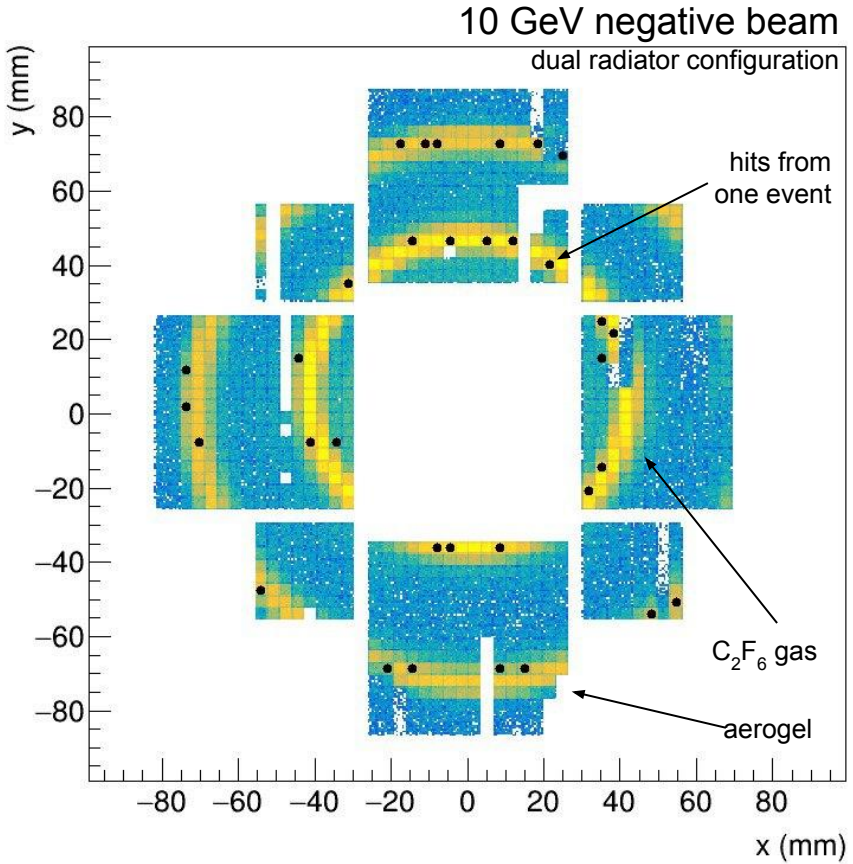
Successful beam test with prototype dRICH and PDUs (CERN-PS, October 2023)

- HPK S13360-3050 (3x3 mm^2, **T = -30/-40°C**)
- 20 FE-DUAL (40 ALCOR v2.0, **1280 channels**)
- DAQ: Xilinx Kintex 7 KC705





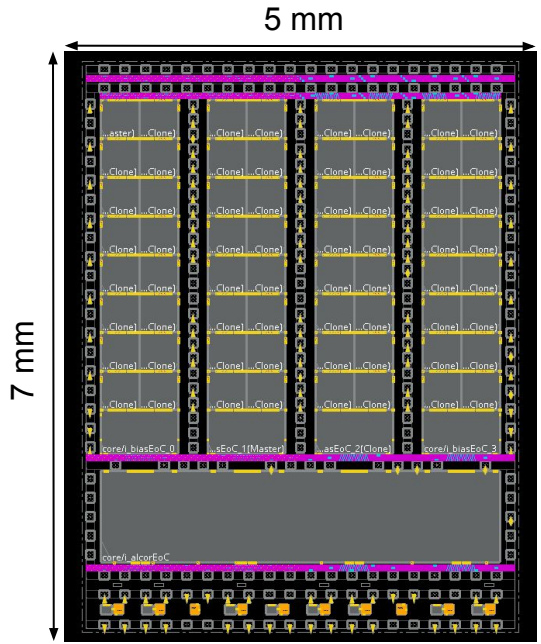
20 x 20 x 20 cm^3

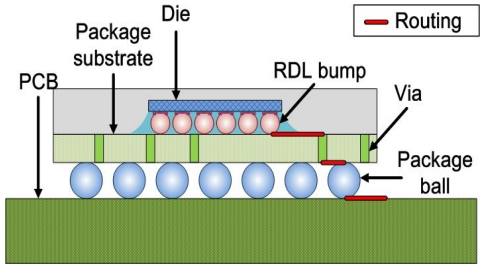


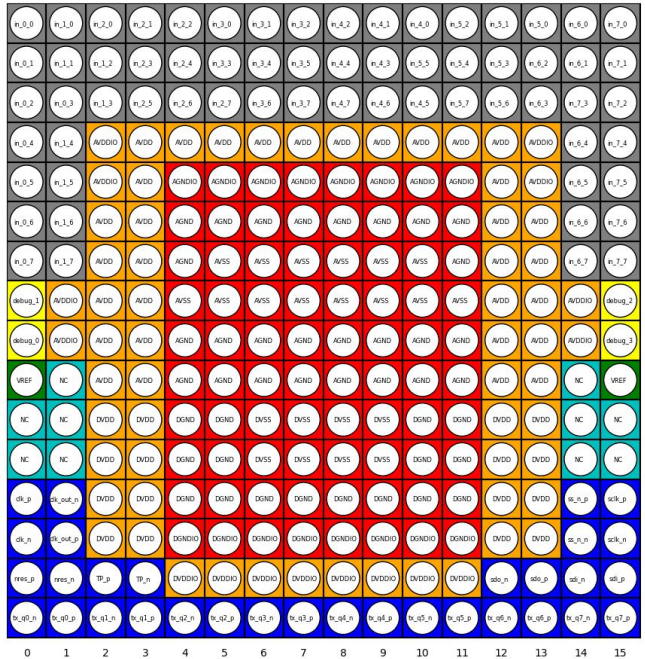
Implementation: ALCOR v3

ALCOR v2: 32-channel wire bonded ASIC

ALCOR v3: 64-channel ASIC, flip-chip BGA package







8x8 pixel matrix ASIC (64 channels)

- SiPM inputs bump pads between the pixel sectors
- Digital EoC in the bottom part

256 balls, 1mm pitch BGA package

- Power and ground on inner/mid contacts
- I/O on outer contacts

ALCOR v3 requirements for EIC

ePIC streaming data acquisition system (no traditional hardware trigger)

- **Digital shutter**: “inhibit” pixel digital logic to suppress out-of-gate DCR hits and **reduce data throughput**
- ~10.2 ns bunch crossing, ~300 ps bunch length, select **2-3 ns time window** → **3x-5x data reduction** before ALCOR digitization
- Asynchronous digital shutter implemented in ALCOR v3 pixel logic using external test-pulse signal
- **Programmable delay chain**: 4 configuration bits at channel-level (LSB ≃ 350 ps) and at the chip periphery (LSB ≃ 100 ps) to adjust offsets between different pixels and columns
- Shutter needed only when DCR becomes higher due to SiPMs taking radiation damage over time → use first period of ePIC data taking to optimize **shutter calibration**

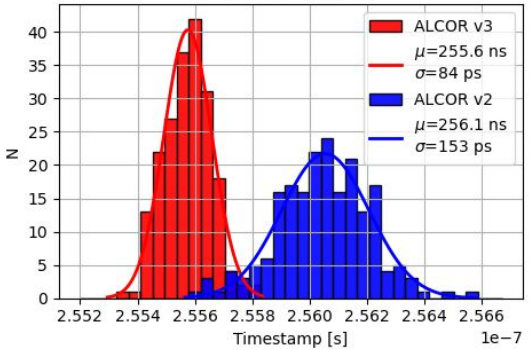
Operation of ALCOR at multiple of **EIC clock frequency** (98.52 MHz)

- Nominal ALCOR v3 clock frequency: 98.52 MHz x 4 = **394.08 MHz**
- Digital logic, TDCs and serializers/drivers re-implemented and verified at 394.08 MHz

ALCOR v3 front-end

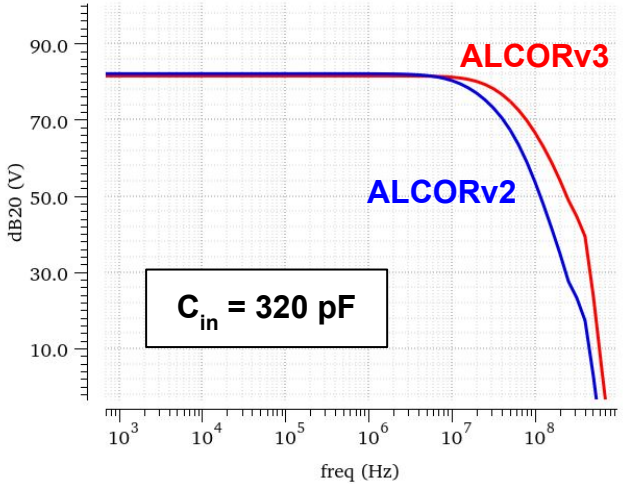
Small revisions on ALCOR FE design

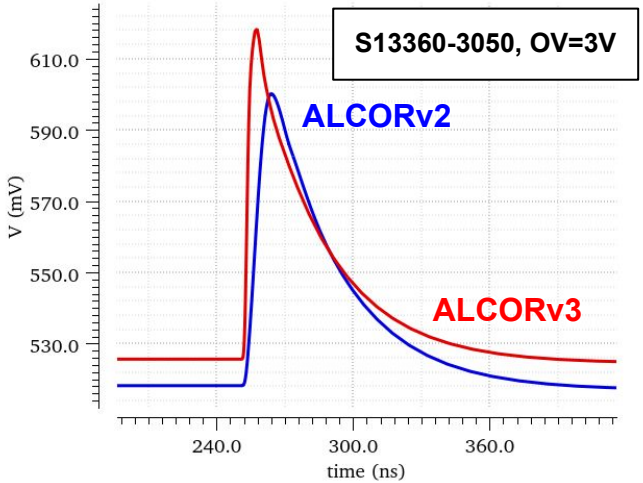
- **Increased amplifier bandwidth** to improve time resolution
  - transient noise simulation
  - Vth = 0.5 p.e.
  - **jitter: 153 ps → 84 ps**



- **Hysteresis discriminator** to avoid re-triggering on slow tail with very low thresholds

➢ **Tape-out scheduled for Fall 2024**





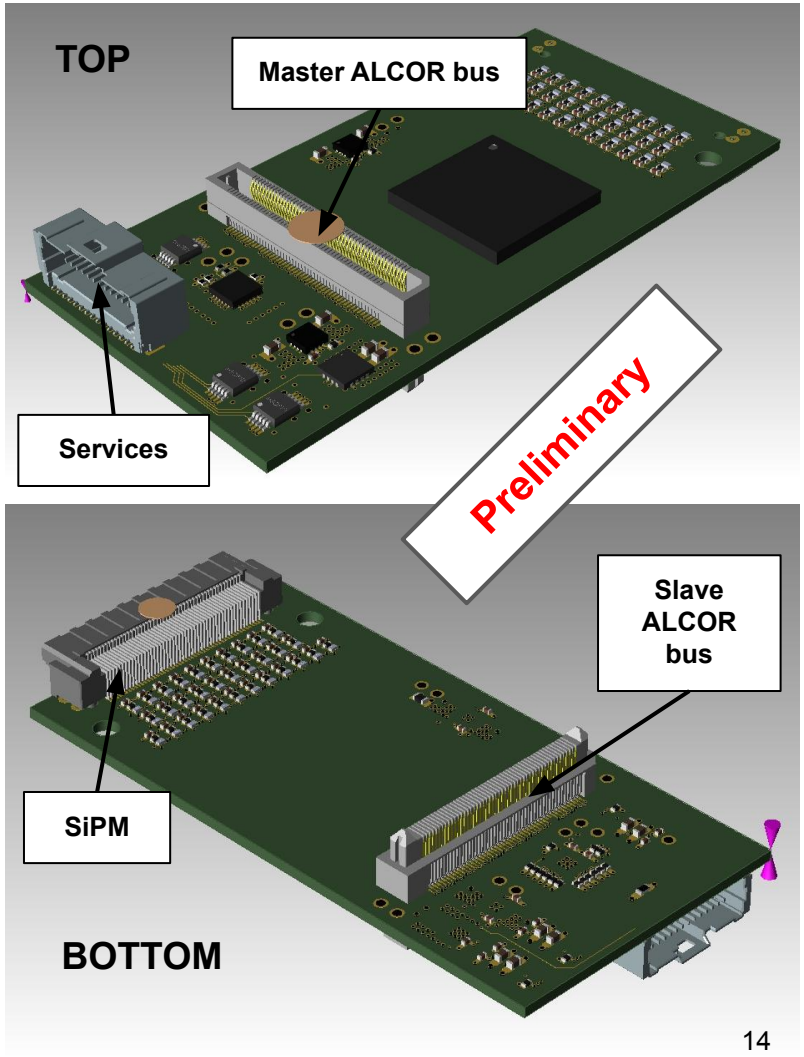
ALCOR FEB

Close cooperation with Bologna colleagues for RDO design, SiPMs requirements and space constraints

Preliminary selection of connectors and components:

- **Master ALCOR bus** (between RDO and FEB, LVDS signals, see P. Antonioli presentation): *Samtec ERM5-050-04.0-L-DV-TR*
- **Slave ALCOR bus** (between first and second FEB, LVDS signals): *Samtec ERF5-050-05.0-L-DV-K-TR*
- **Services connector** (SiPM V_{bias} and $V_{annealing}$, ALCOR LV): *Molex 2035663007*
- **SiPM connector** (SiPM signals, V_{bias} and $V_{annealing}$): *Samtec LSHM-150-01-L-RH-A-N-K-TR*

➢ Dedicated PCB section for SiPMs HV routing
  - 2 V_{bias} and 2 $V_{annealing}$ channels, up to 1 A each
  - **SiPM self-annealing**: forward-bias, **T=150°C** on SiPM matrix board (see ageing modeling and annealing procedures for SiPM DCR in PreBrief)
  - FEB to support **T up to 80-100°C**

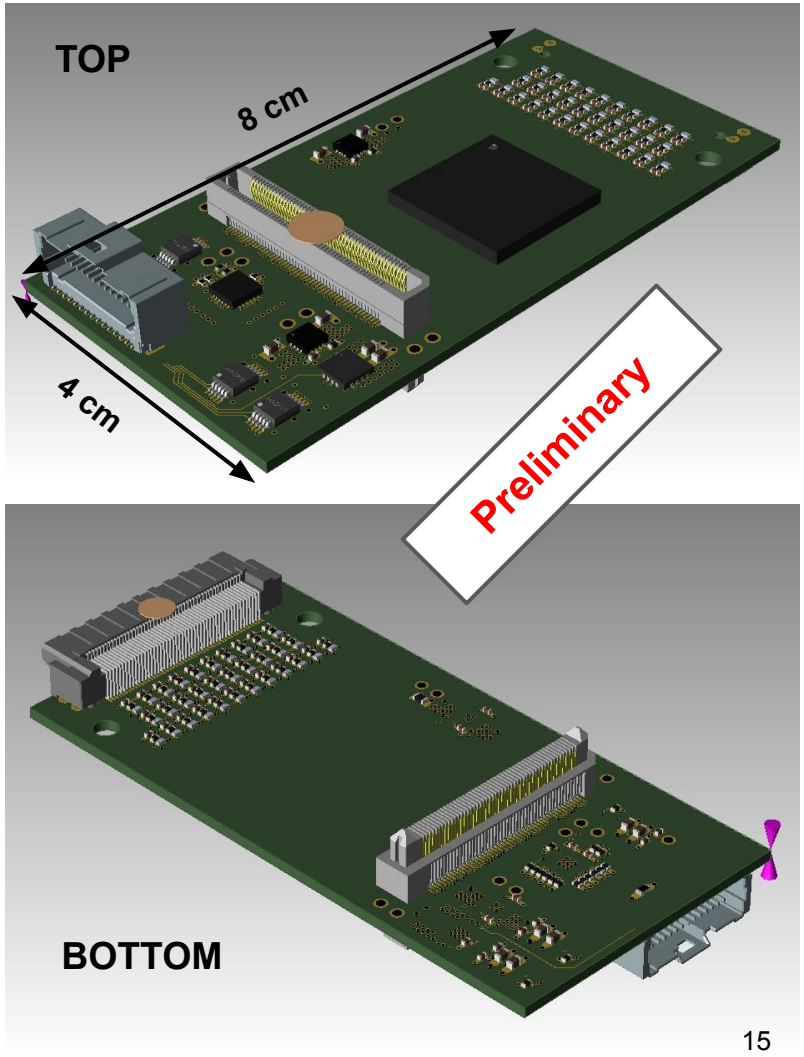


ALCOR FEB

Close cooperation with Bologna colleagues for RDO design, SiPMs requirements and space constraints

Preliminary selection of connectors and components:

- **Linear Regulators** (2.5 V DVDD_IO, 1.2 V DVDD, 1.2 V AVDD): *Analog Devices ADP1752ACPZ-2.5-R7, ADP1761ACPZ-R7*
- **Current monitors** (before regulators): *Microchip Technology MIC2040-1YMM-TR*
- **I2C to Parallel-Port Expander** (read/control regulators and current monitors → **single FEB power on/off granularity**): *Texas Instruments PCF8575RGER*
- **RC High Pass Filter** (AC-coupling between SiPMs and ALCOR)
- **Annealing circuit**: to be included



Other requirements: radiation tolerance

The dRICH-PDUs are in a moderately hostile radiation environment

- Φ (p+n > 20 MeV) = 200 Hz/cm^2
- TID ≅ 650 rad (for 1000 fb^{-1}) < 1 krad

} note these values include a safety factor 5

SEU-SEL

- **Pixel** configuration registers and FSMs **already protected against SEU** in ALCOR v2
- TMR SEU **protection added also for periphery** configuration registers, Hamming code SEU protection for FSMs: Single Error Correction, Double Error Detection codes (SECDED)
- On board prevention of SEL: **current monitor** on FEB regulators

TID

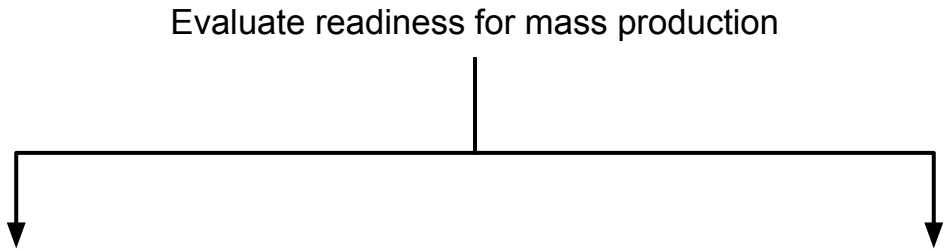
- Same technology already verified for TID up to a **few hundreds of krad**
- Also other FEB components will be tested and validated

➢ Irradiation tests campaign: SEU/SEL and TID tests at Centro of Proton-Therapy in Trento with ALCOR current version foreseen in July 2024

Schedule

Our aim is to have the **first FEBs validated by Spring 2027** in order to begin the PDUs assembly

- Fall 2024: **ALCOR v3 MPW** tape-out and BGA package
- Spring 2025: ALCOR v3 BGA devices received → electrical characterization and integration tests



- Fall/Winter 2025: **ALCOR Engineering Run**
- Summer 2026: start ALCOR mass production tests, FEBs assembly and validation

- Fall 2025: **ALCOR v3.1 MPW** tape-out
- Spring 2026: ALCOR v3 BGA devices received → electrical characterization
- Summer 2026: **ALCOR Engineering Run**
- Winter 2026: start tests of ALCOR mass production, FEBs assembly and validation

ESH & QA plans

FEB produced following EU rules on restriction of hazardous substances (RoHS)
ALCOR/FEB tests and validation managed by INFN Torino
Safety rules enforced at INFN Torino Lab available here

The company charged to produce FEB:

- PCB electrical test
- RX analysis for BGA connections

Test procedure:

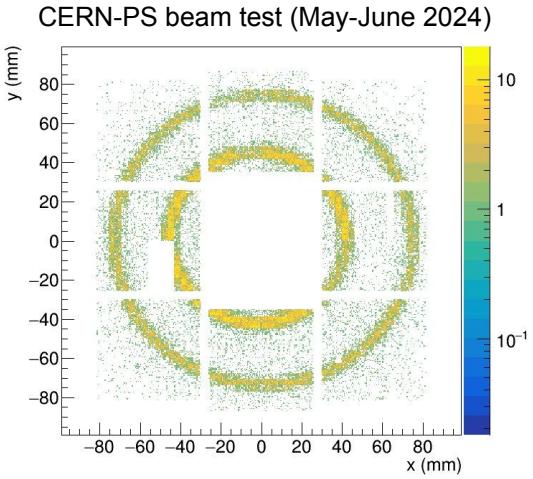
- Power-on, configuration, alignment, TDC scan, VTH scan, (SiPM DCR scan)
- Special test board card will be developed to test ALCOR/FEBs also without RDO
- Different options are currently being evaluated: in-house testing or external company
- FEB moved to PDU assembly line: test repeated with FEBs connected to PDU & RDO

FEB (ALCOR) is part of INFN IKC: compliance with US norms + delivery/acceptance procedures at BNL being specified in PPD

Reference documentation, test protocols and special cards for testbenches will be developed in 2026

Summary

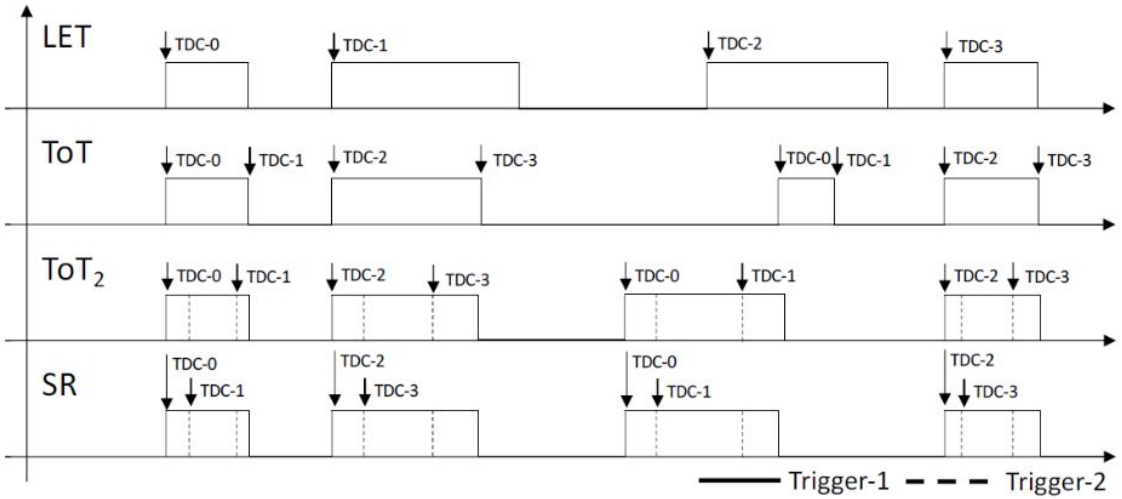
- ALCOR fulfills dRICH requirements for SiPM readout
  - Several laboratory and beam tests demonstrated ALCOR-based readout **single photon sensitivity**, approaching 100 ps time resolution
  - New test beam at CERN-PS (May-June 2024) to validate the full system and evaluate its performance (2048 readout channels)



- Identified technical solutions to meet EIC-driven specifications
  - **Digital shutter** to reduce data throughput
  - New ALCOR **clock frequency**: 98.52 MHz x 4 = **394.08 MHz**
- Other design revisions for ALCOR new version defined
  - Analogue **FE optimization**, **hysteresis discriminator**
  - New chip layout for **BGA package**
  - **ALCOR v3 MPW tape-out in Fall 2024**
- FEB design ongoing to meet dRICH readout system requirements
  - **RDO** design: interface for data, configuration, control, services (more details in P. Antonioli talk)
  - **SiPMs** requirements: provide bias and annealing
  - **Space** constraints: 4 cm x 8 cm

Backup Slides

ALCOR pixel operating modes



4 operating modes:

- **LET**: leading edge measurement
- **ToT**: Time-over-Threshold measurement using the first discriminator for both edges
- **ToT2**: Time-over-Threshold measurement using both discriminators
- **SR**: slew-rate measurement

Each mode can be set to:

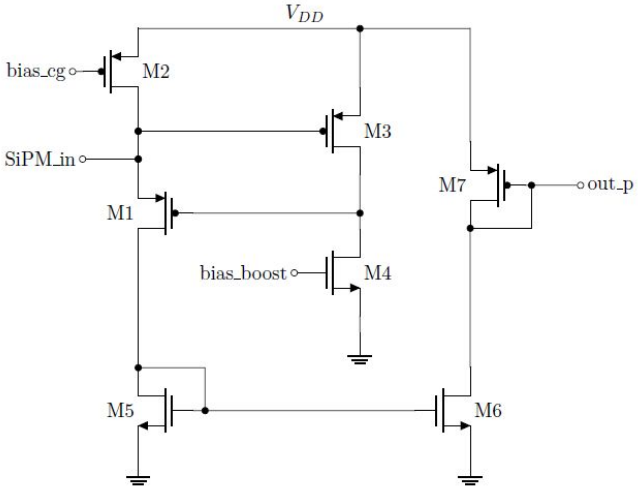
- **FE**: normal operation mode
- **FE_TP**: send test-pulse to analogue front-end
- **TDC_TP**: send test-pulse to pixel control logic to test and calibrate TDCs (bypass front-end)

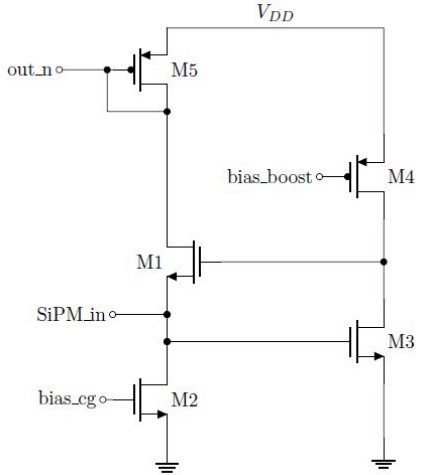
Each pixel can also be disabled

ALCOR Front-End

Input stage

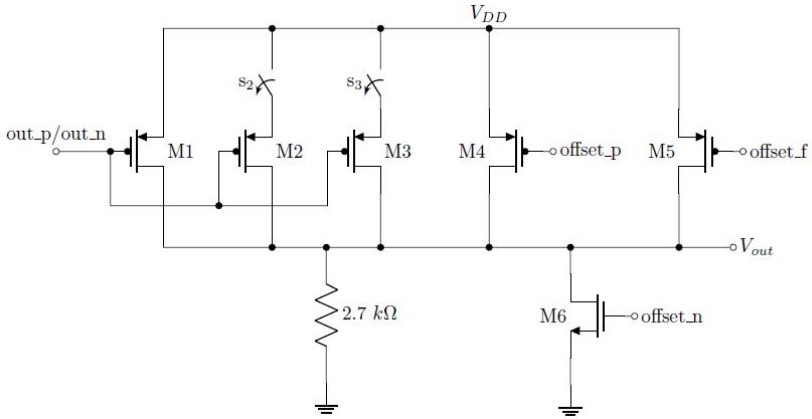
- Dual-polarity RCG current conveyor
- Programmable bias currents: CG (30-100 µA) and BOOST (1-4 mA)
- Z_{in} ~ 10-20 Ω





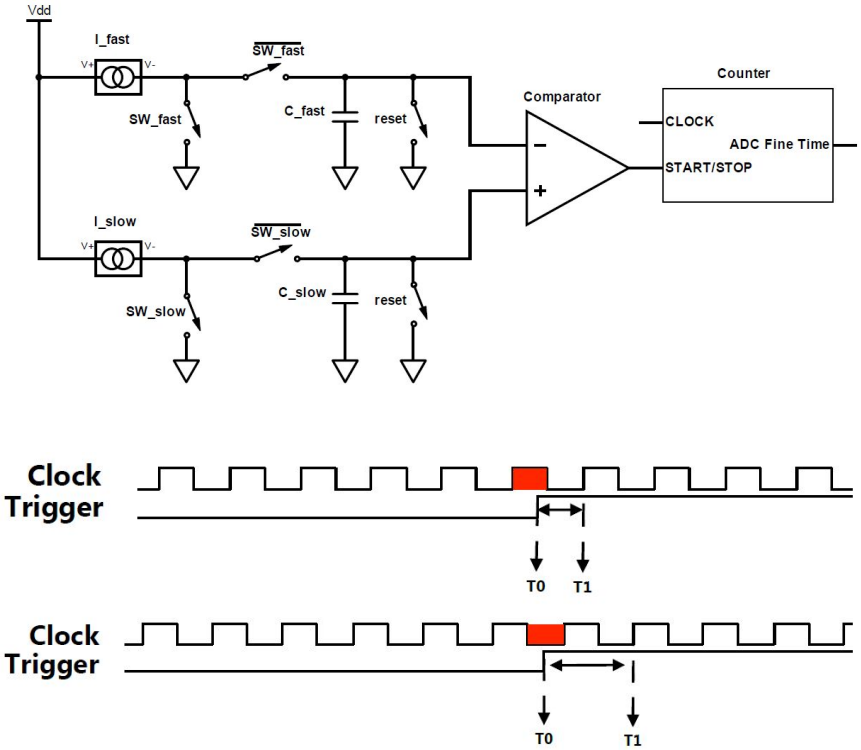
Output stage

- TIA gain: 2.7 kΩ
- 4 gain settings: 1/3, 4/3, 7/3 and 10/3
- DC coupled: baseline compensation based on gain and CG bias current settings + fine offset adjustment (3-bit)

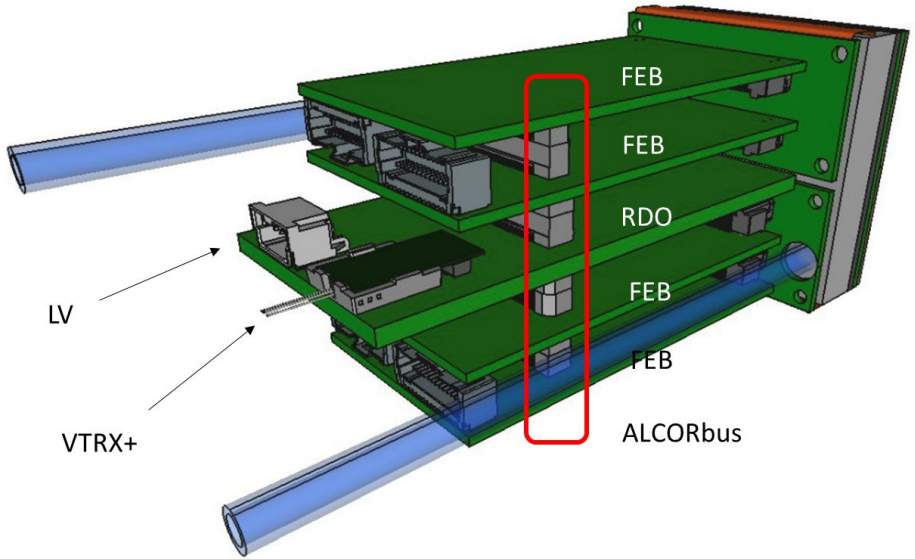


Time to Digital Conversion

- Coarse time: 15-bit clock counter
- Time conversion performed by **TDC** based on **analogue interpolation** (9-bit fine time):
  - ***fast ramp***: constant current to charge C_{fast} → measure phase between event trigger and clock
  - ***slow ramp***: smaller constant current to charge C_{slow} → counts clock cycles until C_{slow} and C_{fast} are equal
- I.F. 64 or 128 → LSB = 25-50 ps @320 MHz
- Measured time interval: 0.5 - 1.5 clk period
- TDC conversion time: [200, 600] ns
- 4 TDCs per pixel for **event derandomization**



ePIC dRICH photodetector unit (PDU)



ALCOR QA → Mass production tests

Different options are currently being evaluated

- N. FEBs: 4992 → N. ALCOR: 4992 (to be increased to include QA, yield and lifetime)
- 7500 ALCOR → 85% yield → 6375 ALCOR
- Test time: 5-10 min./ALCOR (to be defined, test procedure used for ALCOR v2.1 as reference)

- 7500 ASIC · 10 min./ASIC = 75000 min. = 1250 h.

<u>Manual handling</u> (in-house testing)

6 h./day · 5 days/week = 30 h./week

1250 h. / 30 h./week = 42 weeks ⇒ **10-11 months**

- ➢ Parallel setups to reduce time for mass testing (contribution from other INFN sections under discussion)
- ➢ After first batch, rest of production can be tested in parallel with PDUs assembly → no schedule delays

<u>Automated handler</u> (external company)

24 h./day · 7 days/week = 168 h./week

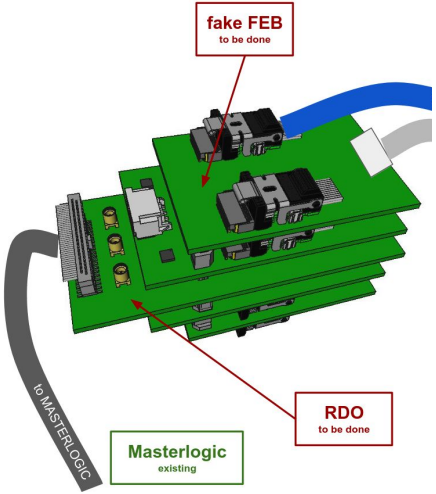
1250 h. / 168 h./week = 7-8 weeks ⇒ **2 months**

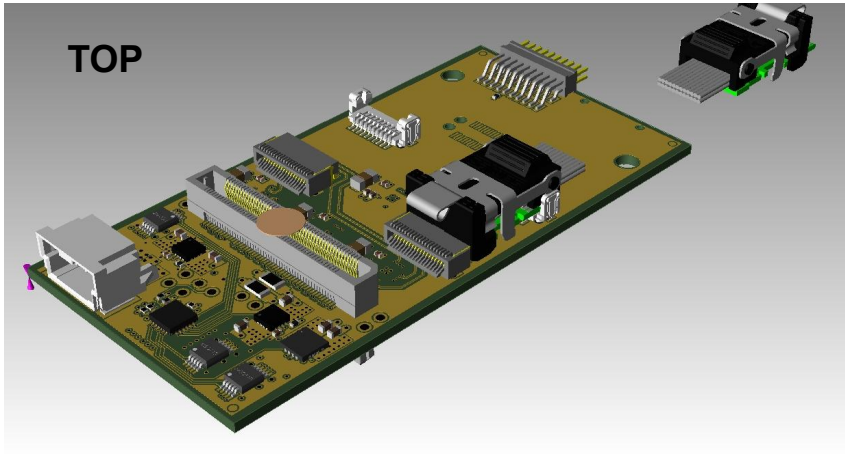
- ➢ Will require external company to perform the tests (→ **additional costs**)
- ➢ No manpower required for mass tests, but still requires manpower to develop and debug the test system

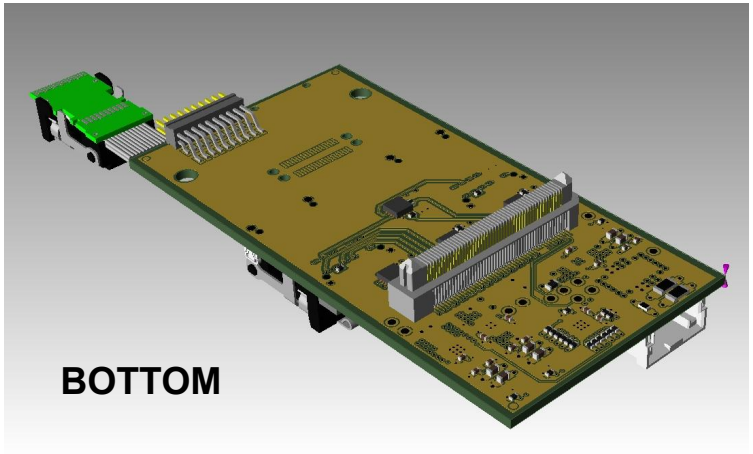
“Fake” FEB

Support 2024-2025 dRICH activities when final FEB and ALCOR v3 are not available yet

- Allows integration tests of RDO with current ALCOR-FE-DUAL boards (already available and validated)
- 4 fake-FEBs + 1 RDO (still off-detector)





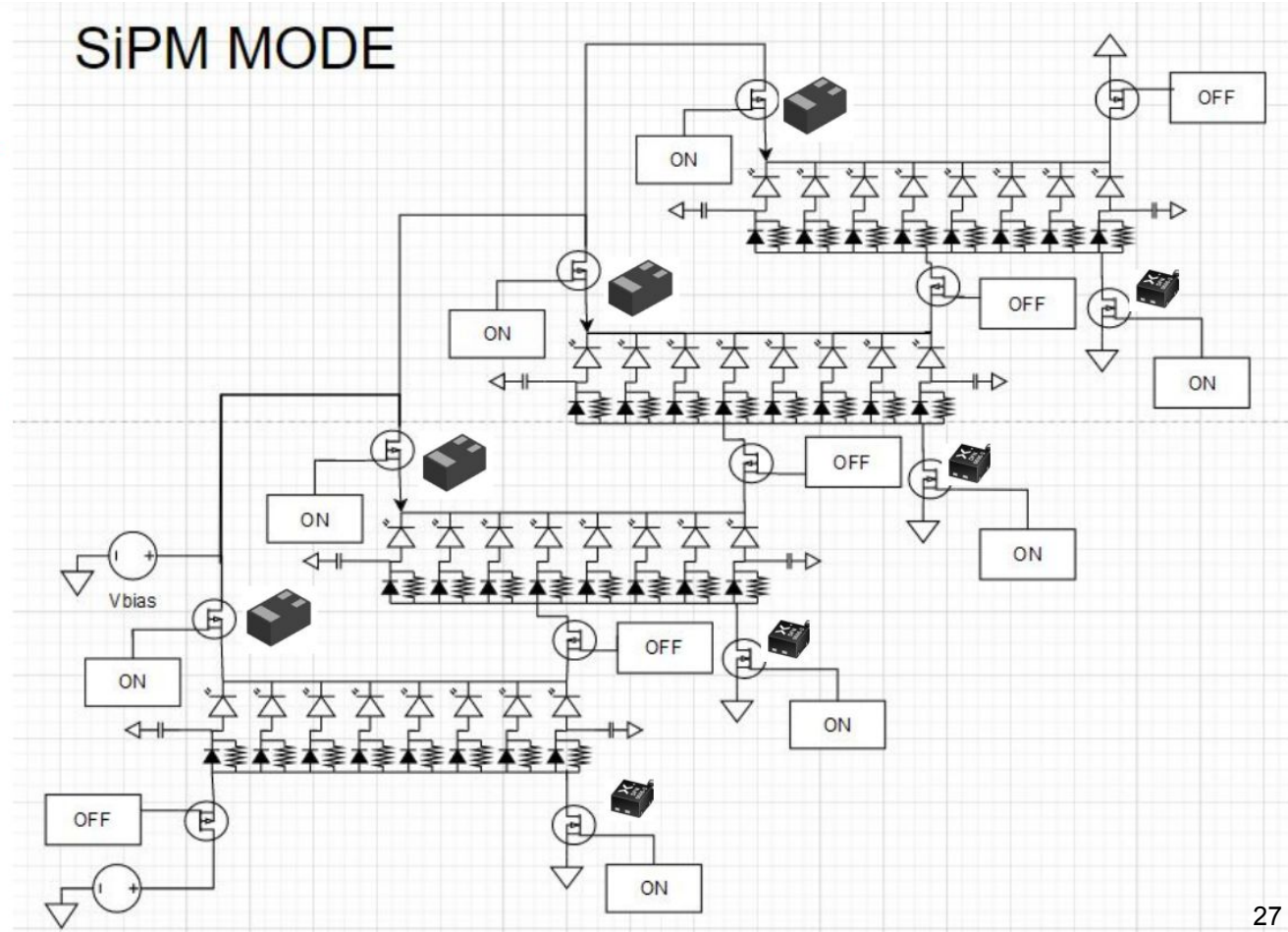


Vbias distribution

the circuit foreseen to allow both normal operation of SiPM (reverse bias) and self-annealing (forward bias) allows to inhibit the Vbias to a granularity of 8 SiPM.

might come at handy in case of troubles with Vbias distribution in a specific SiPM → inhibit Vbias in a string of 8 SiPM sensors while the rest of the PDU can still be operated

digital switches (MOSFET) controlled by RDO



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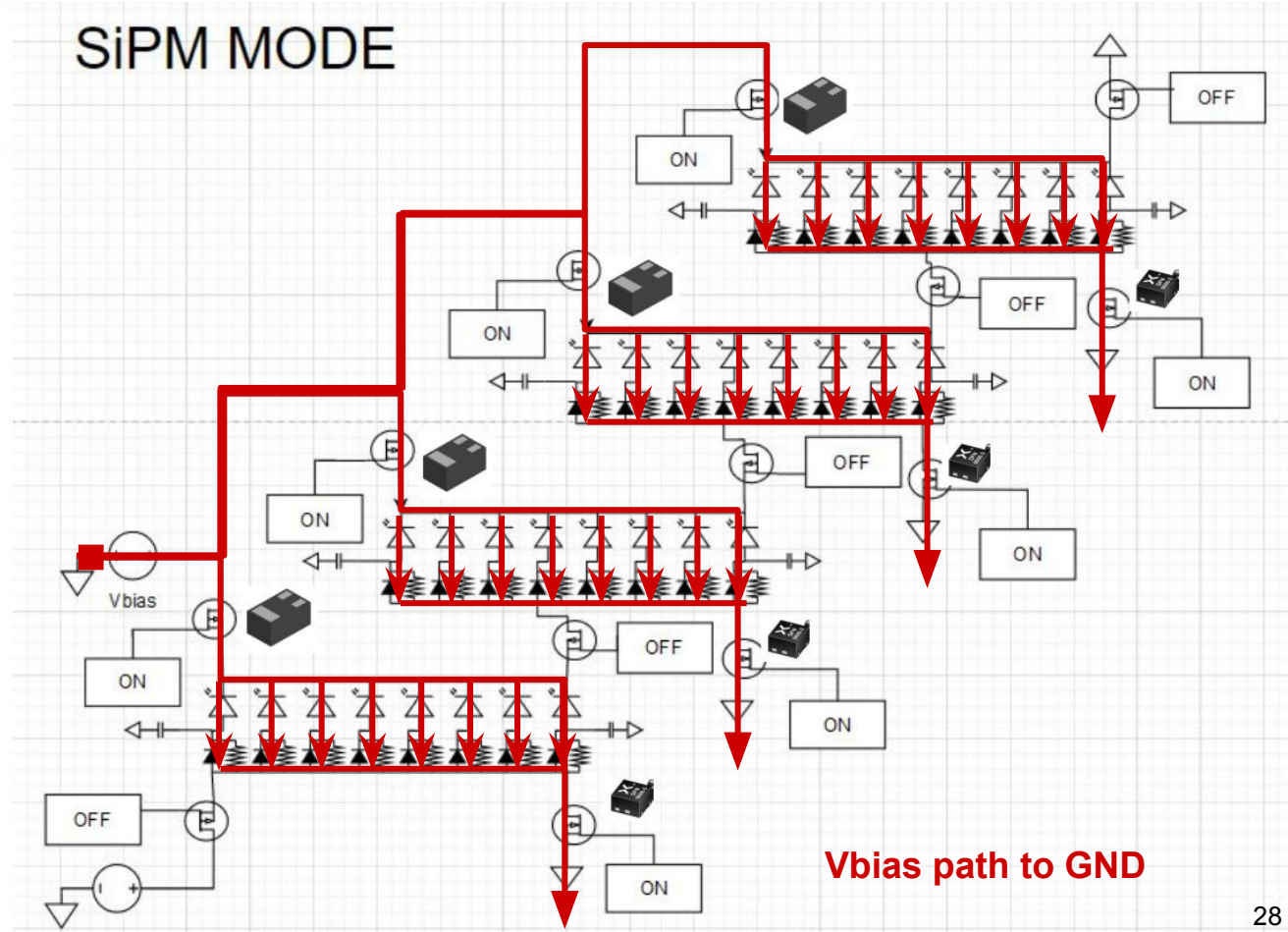

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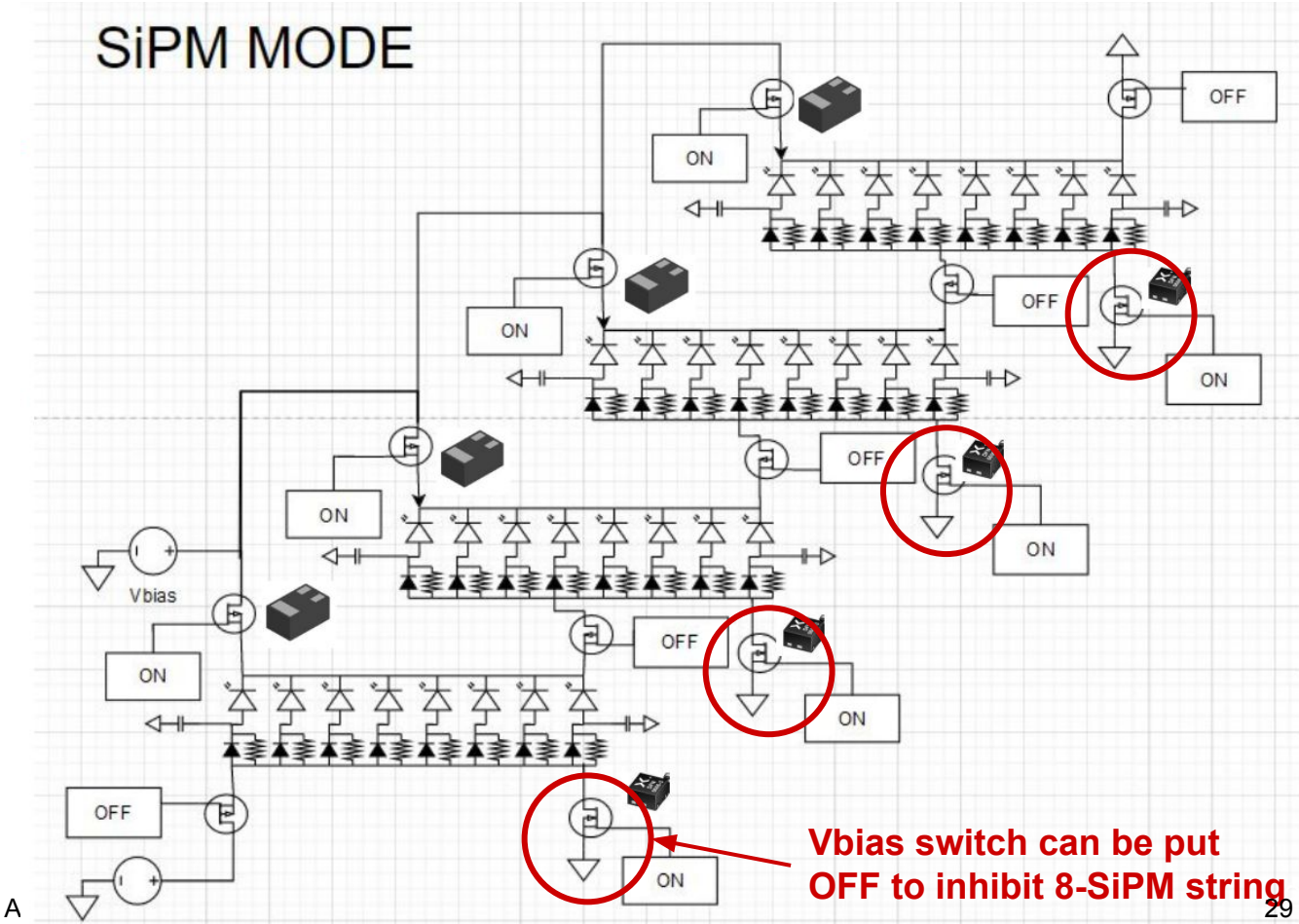
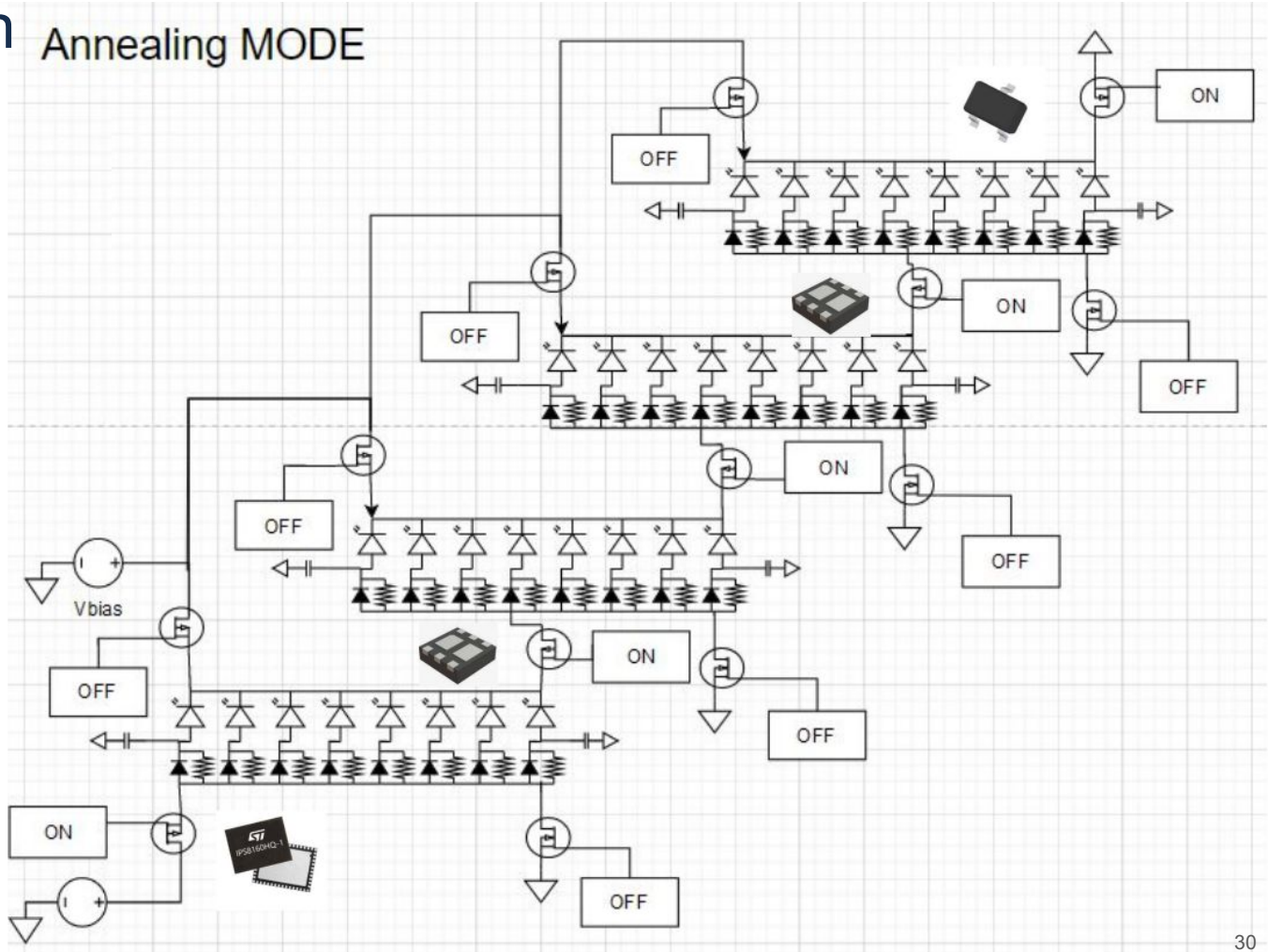


Vann distribution

forward-bias annealing current for each sensor can reach up to 100 mA
to keep annealing current low we foresee to forward-bias the SiPM in series of 4 SiPM strings



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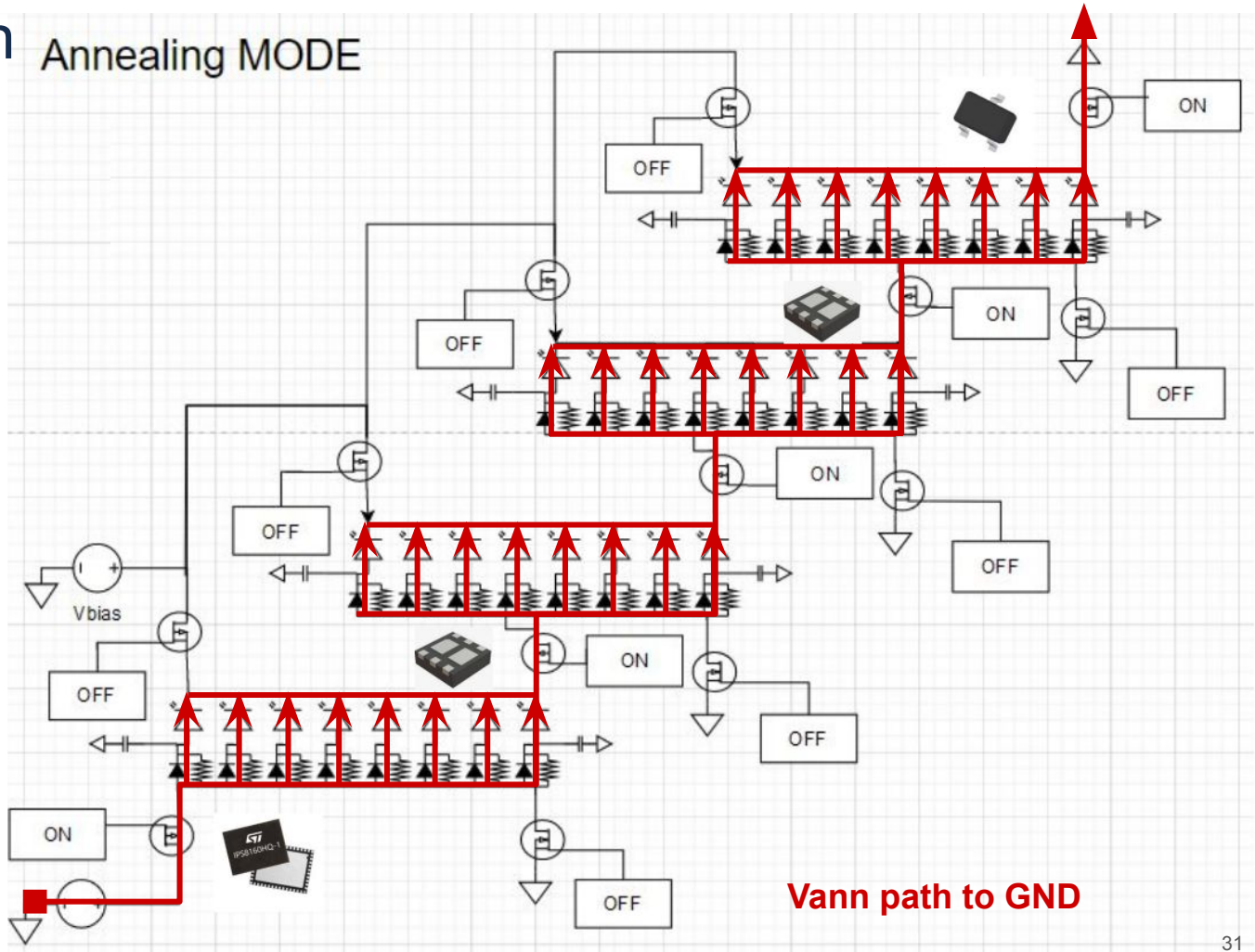


PDU voltage services

the **SiPM grouping** is composed of 4 strings of 8 SiPM each

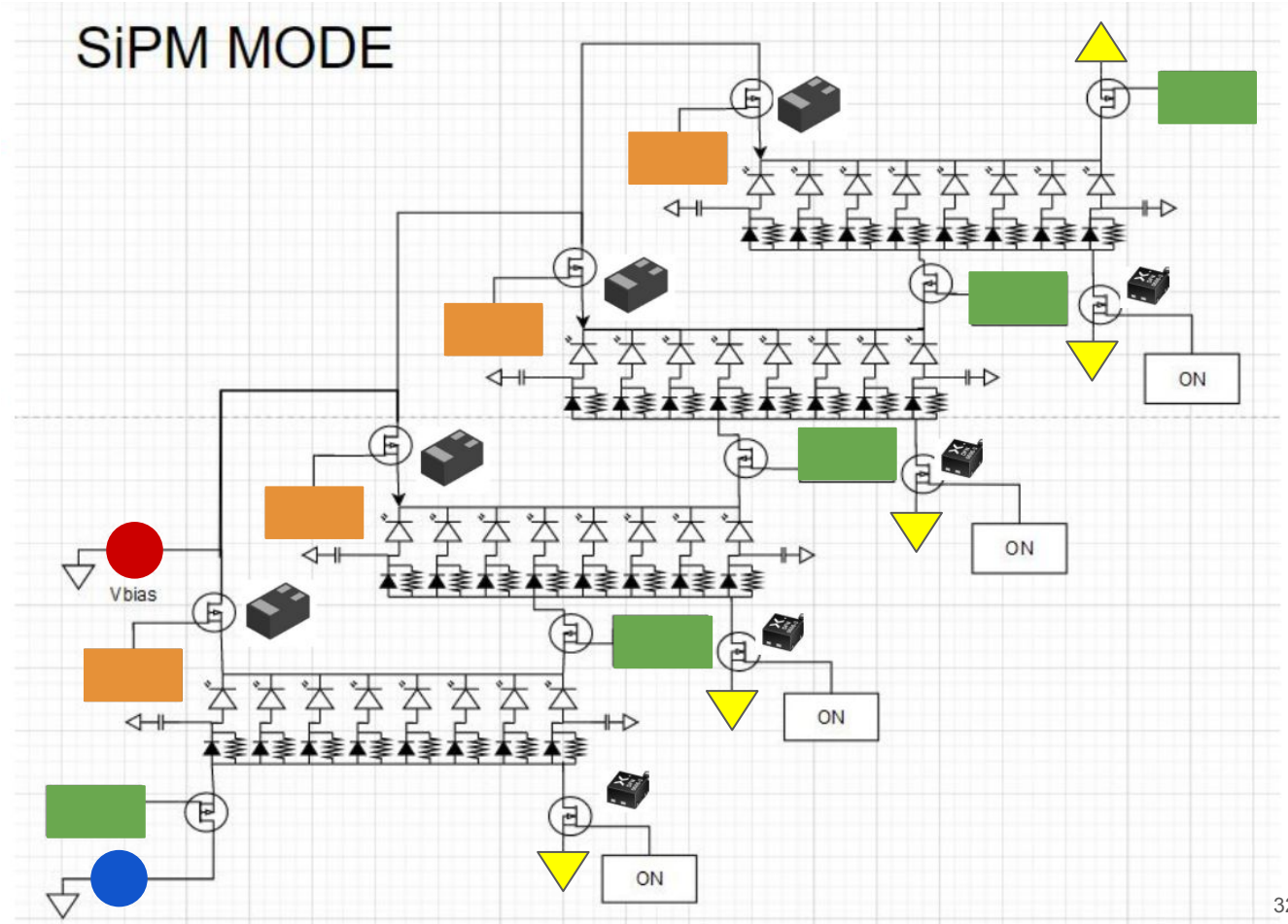
one **SiPM matrix** is composed of two SiPM groupings

the **dRICH PDU** is composed of four SiPM matrices

for each SiPM grouping we foresee the following external services (via FEB)

- **1 V-bias**
- **1 CTRL-bias**
- **1 V-ann**
- **1 CTRL-ann**
- **1 GND**

This is a total of 5 wires for each SiPM grouping, namely a total of **40 wires for one PDU**. The 40 wires enter from the readout box patch-panel.



ALCOR for SiPM characterization measurements