Brookhaven National Laboratory

Jefferson Lab

U.S. DEPARTMENT OF ENERGY

Timing Implementation for the Readout Chain

William Gu

Incremental Preliminary Design and Safety
Review of the EIC Detector DAQ and Electronics
June 10 -11, 2024

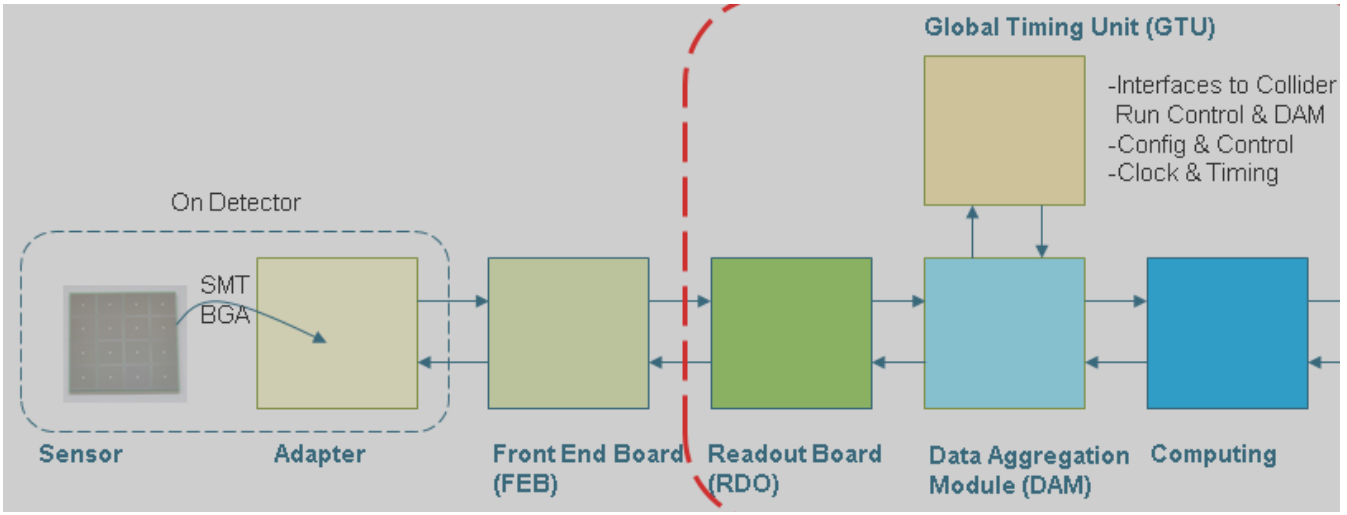
Electron-Ion Collider

About Me – William Gu

- 2009 – Now, Jlab
- 1998 – 2009, Ohio State, solely working on CMS/LHC
- 1990 – 1998, IHEP, Beijing, China

Outline

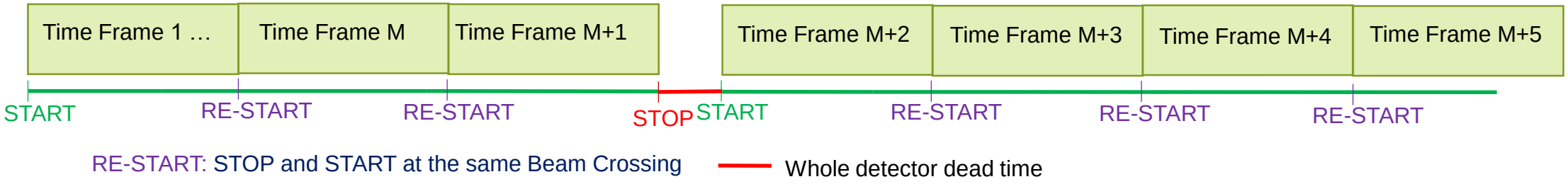
1. The requirements
2. The designs
3. Test results
4. Summary



1. The requirements

1.1 Synchronized control

Streaming Data



1.2 Jitter of the FEB/ASIC received clock: less than 5ps;

1.3 For TOF detectors, the phase of the clock relative to the beam crossing center point is stable (less than 5ps);

1.4 For dRICH detector, the phase of the clock relative to the beam crossing center point is stable (< ~100ps) for shutter implementation (zero suppression)

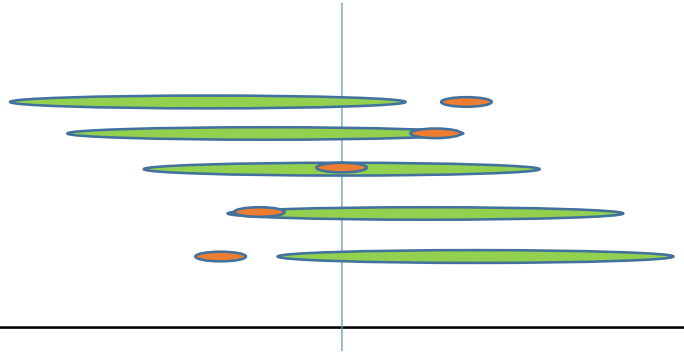
2. The designs

2.1 The EIC beam crossing

	Electron Storage Ring (ESR)	Hadron Storage Ring (HSR) (N_b=290)	HSR (N_b=1160)
Circumference C [m]	3833.940	match T_{rev}	match T_{rev}
Revolution period T_{rev}=C/c [μs]		12.7886	
RF harmonic number h [-]	match HSR	2520	7560
RF bucket spacing T_b=T_{rev}/h [ns] NOT bunch spacing!!!	match HSR	5.075	1.692
Number of bunches N_b	match HSR	290	1160
Bunch spacing T_{bun} [ns]	match HSR	40.599	10.150
Gap length [ns]	match HSR	1015	1015
RMS bunch length σ_z [mm/ps]	7-9/23-30	75-60/250-200	

Electron Beam Energy: 5 – 18 GeV
Proton Beam Energy: 41, 100 – 275 GeV
Luminosity: 10^{34} $cm^{-2}s^{-1}$

Beam crossing: 98.5MHz or 10.150ns
Orbit period: 12.7886 μs or 1260 BeamCrossing



2. The designs

2.2 The ePIC Timing/Control distribution

GTU: Global Timing Unit

control encoding, status decoding.
The interface for machine clock source,
Data acquisition control and monitor etc.

DAM: Data Aggregation Module:

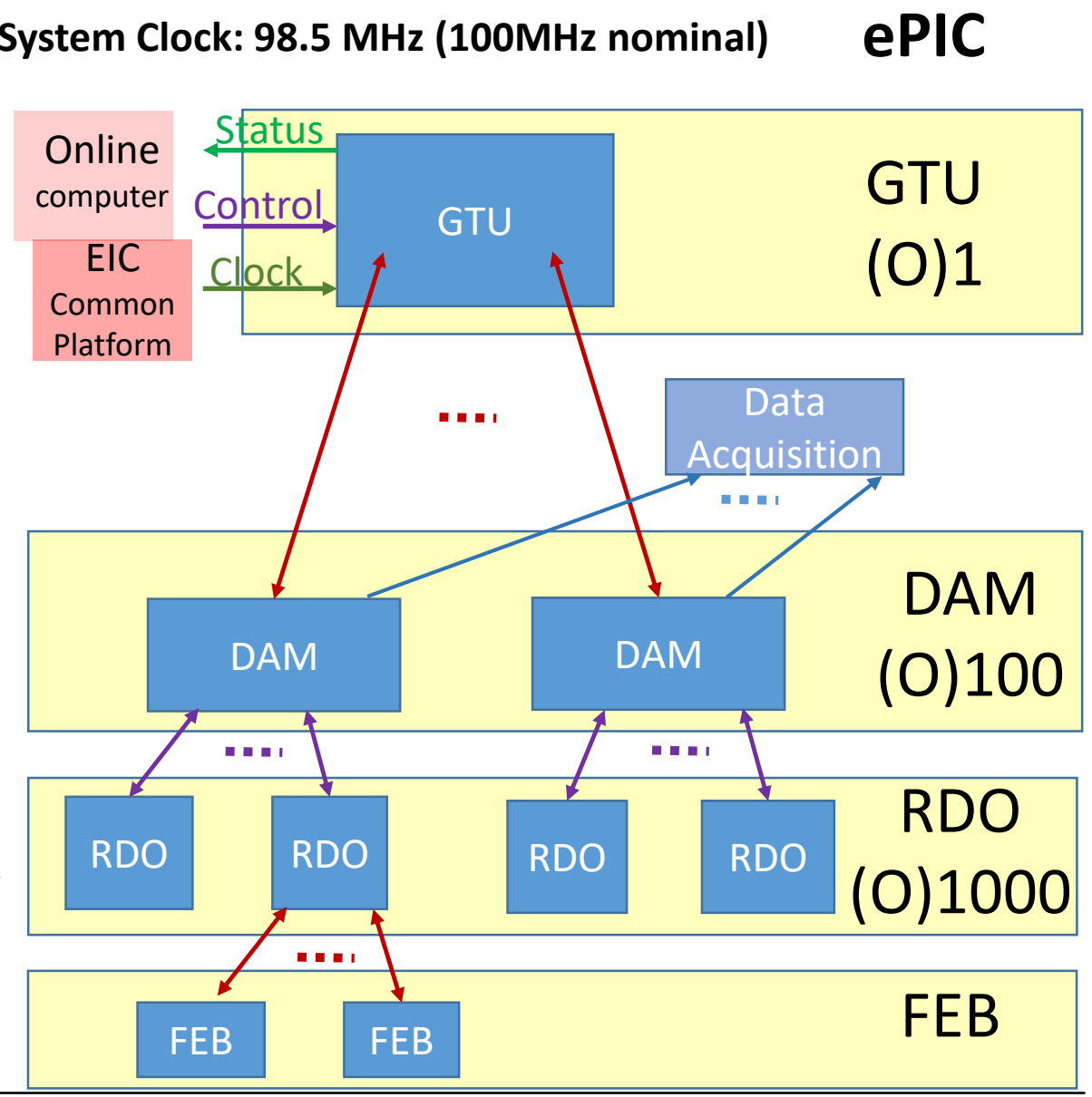
The clock/control fanout, and status/busy accumulation.
local control over the RDO boards connected, though the main function of the DAM is for Data Acquisition.

RDO: optical interface of detector ReaDOut

control decoding, status encoding.
The clock/control interface to the front end electronics.
Data collection from Frontend boards, and data transmission to the DAM

FEB:

Detector dependent Front End / ASIC carrier boards.



2. The designs

2.3 The hardware design

2.3.1 GTU

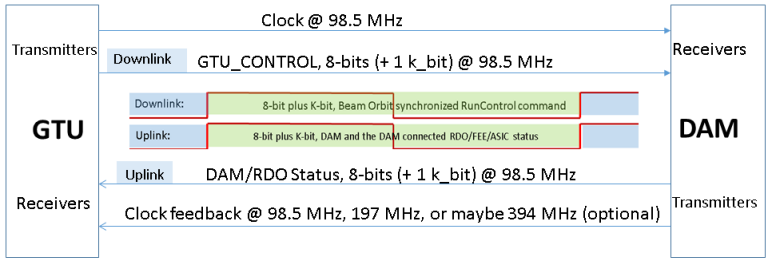
GTU clock fanouts (1:~200):
Additive Jitter <1ps; Phase: fixed

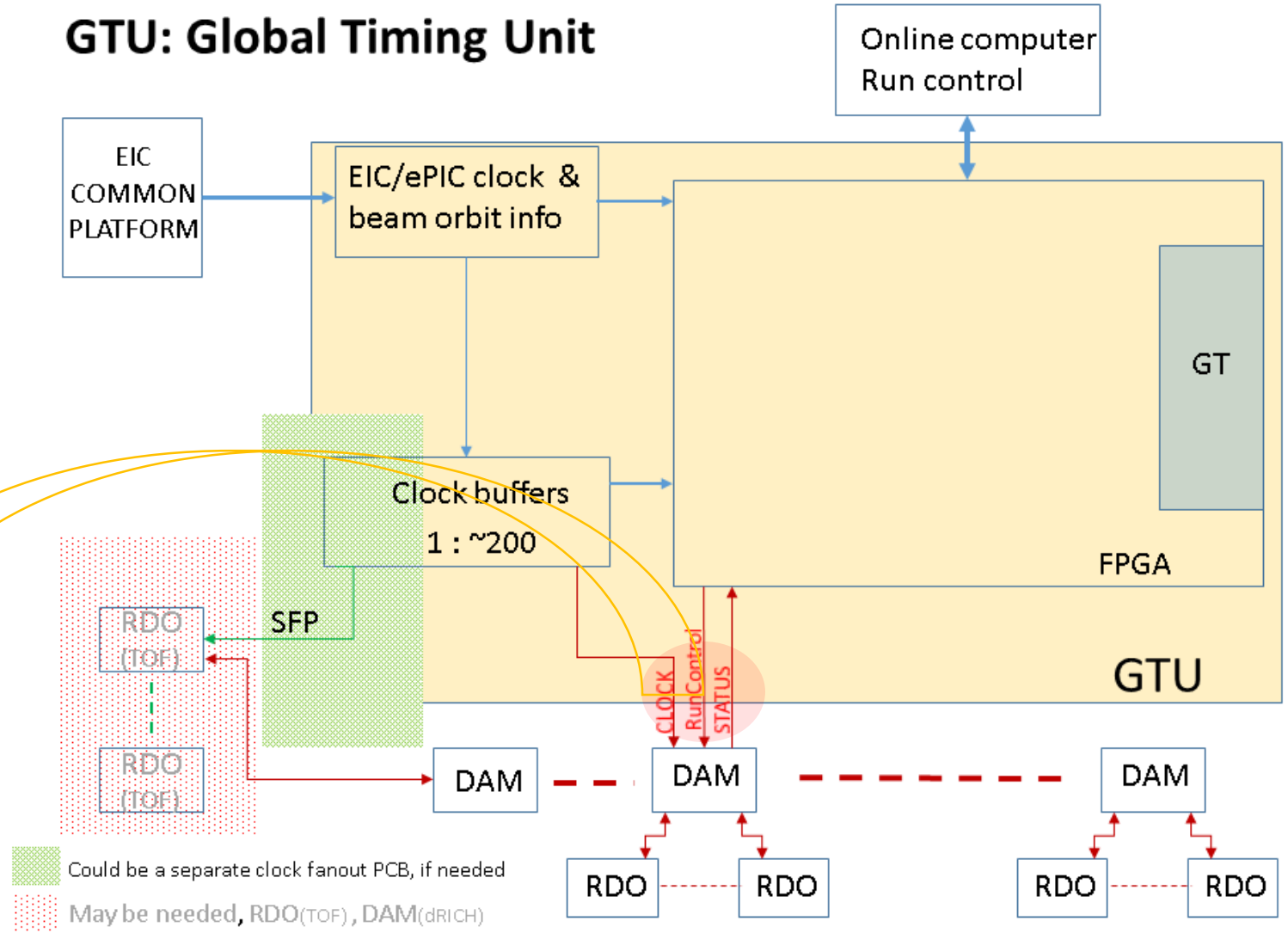
Global control: 8-bit code (> 256 codes) on every clock

Dedicated (clock only, 197 Mbps) fiber
Additive Jitter <1ps; Phase: fixed

The GTU will have ~150 ports (four fiber per port). Each port can connect to one DAM.

GTU ←→ DAM port





2. The designs

2.3 The hardware design

2.3.2 DAM

DAM clock fanouts (1:12):
Additive Jitter <1ps;
Phase: fixed

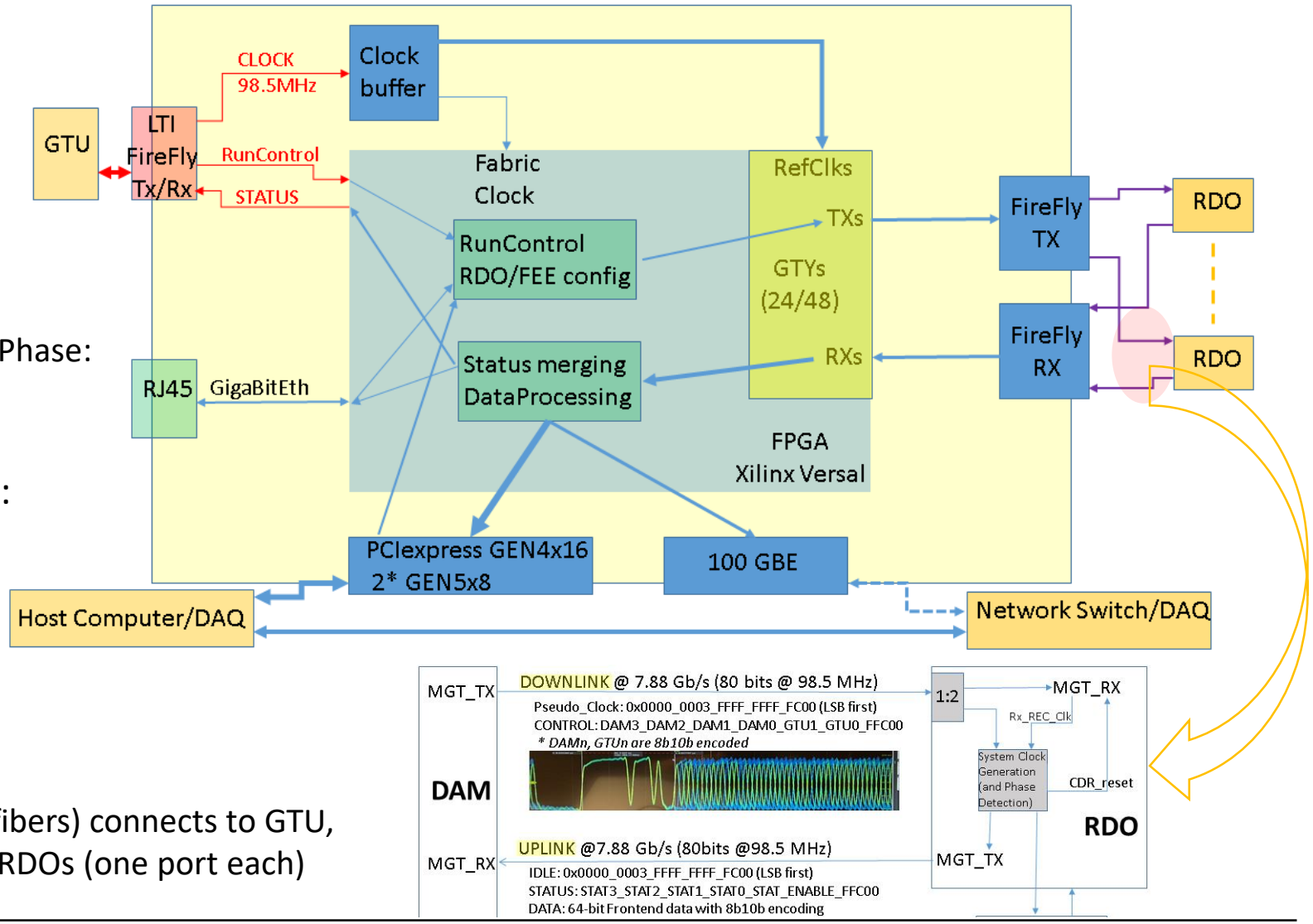
MGT Clock/Control encoding (Quad):
Additive Jitter <~ps;
(TX serialized data relative to the clock) Phase: stable, can be fixed

1:1 (Clock/Control, 7.88 Gbps) fiber:
Additive Jitter <1ps; Phase: fixed

The Controls include the Control from GTU, and the RDO/FEB configurations from DAM

The DAM will have one fiber port (four fibers) connects to GTU, and 48 ports (two fibers) connect to 48 RDOs (one port each)

DAM: Data Aggregation Module



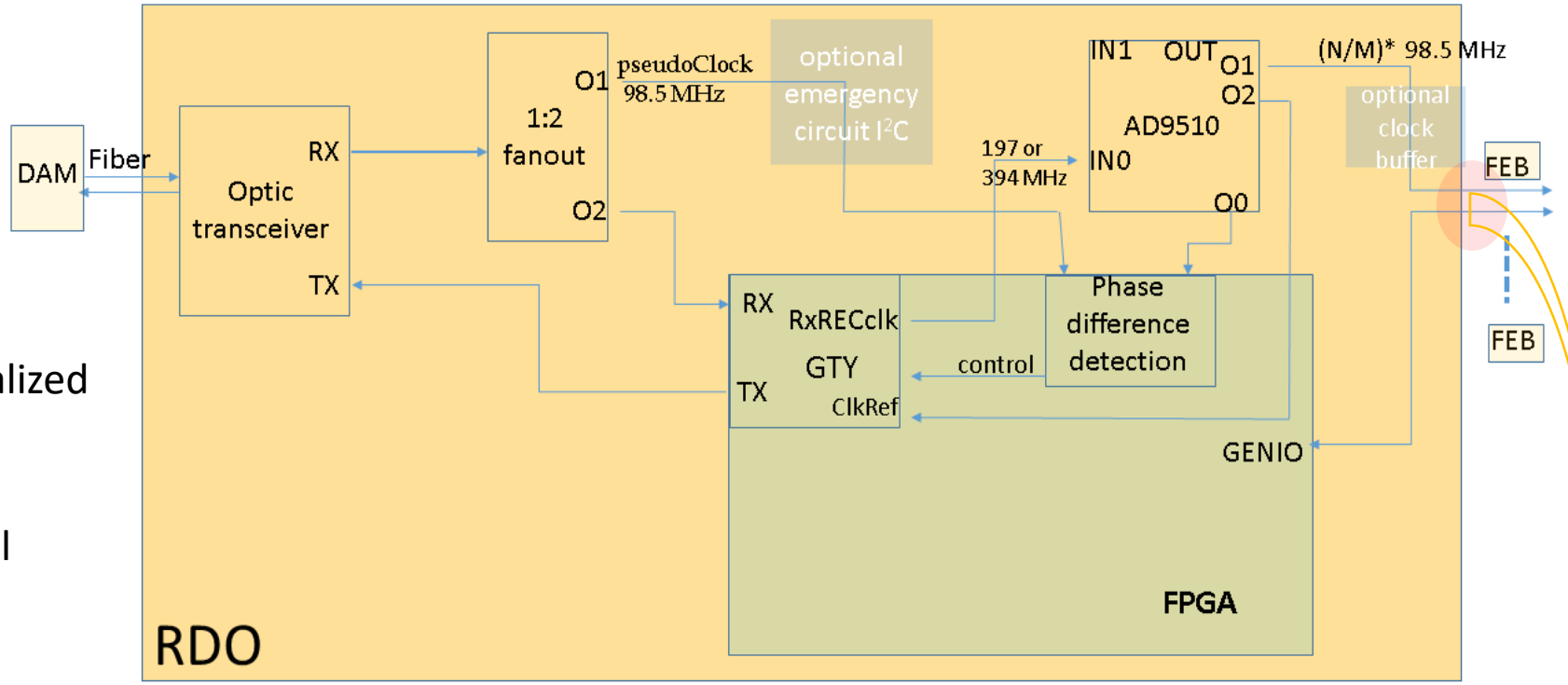
2. The designs

2.3 The hardware design

2.3.3 RDO

RDO MGT RECovered Clock:
Additive Jitter <3ps;
Phase: stable,
fixed with PseudoClock (serialized clock/control from DAM)

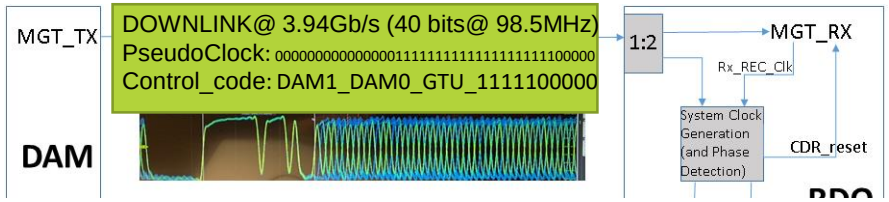
The RDO de-codes the control synchronously, and the RDO/FEB/ASIC configuration;
Assemble time-frame data, also RDO/FEB/ASIC status



VTRX+ on the RDO for radiation

This (3.94 Gb/s stream) can also be received by 7.88 Gb/s receivers

The RDO will have one fiber port (two fibers) connect to the DAM, and several ports connect to FEB/ASIC



RDO flavors (FEBs) dependent copper connection

2. The designs

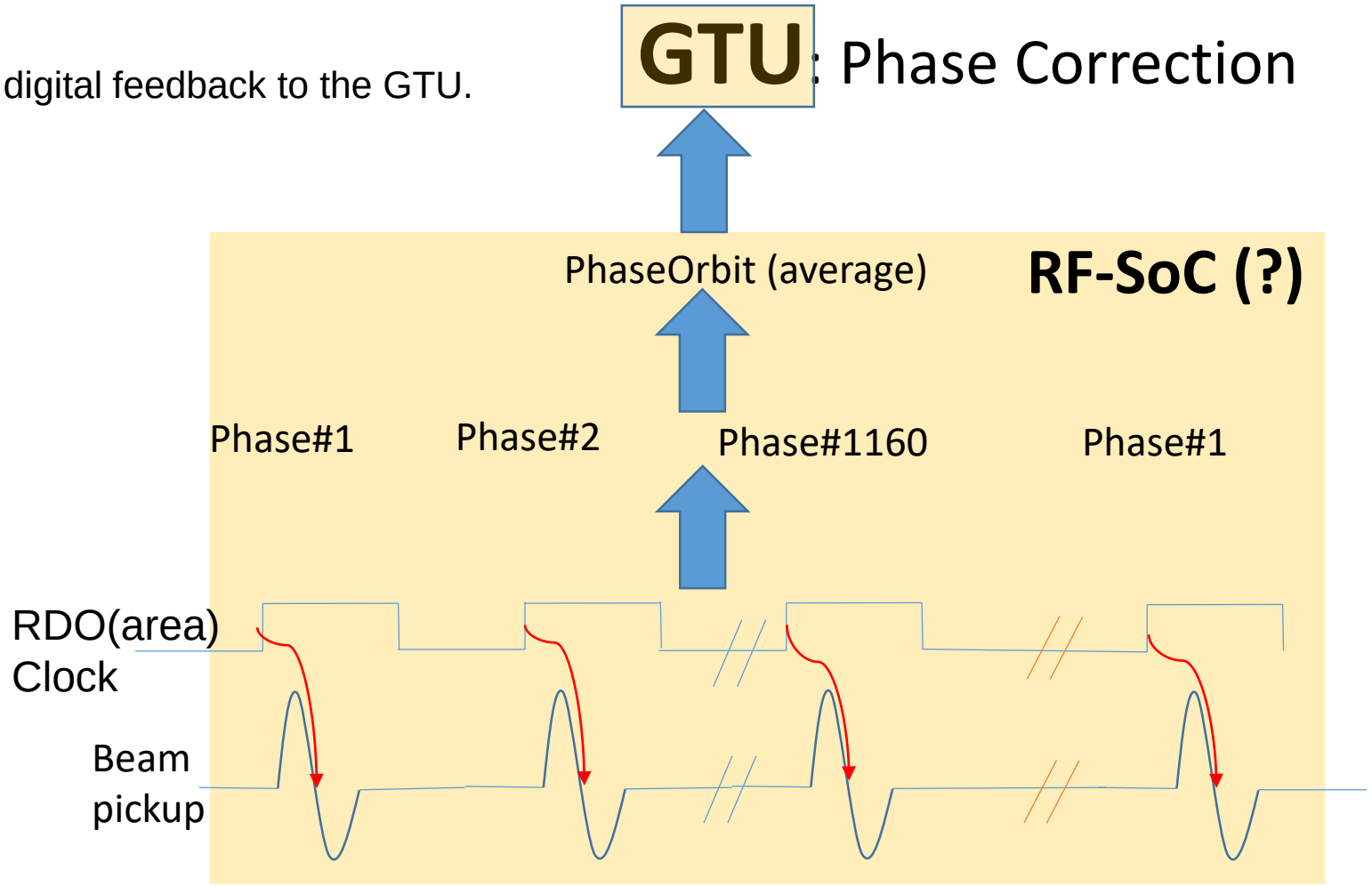
2.4 The risk mitigations (planB for *requirement 1.3*, Clock Phase < 5ps)

2.4.1 Direct system clock distribution from GTU to TOF_RDOs.

Clock jitter < 3ps, phase fixed

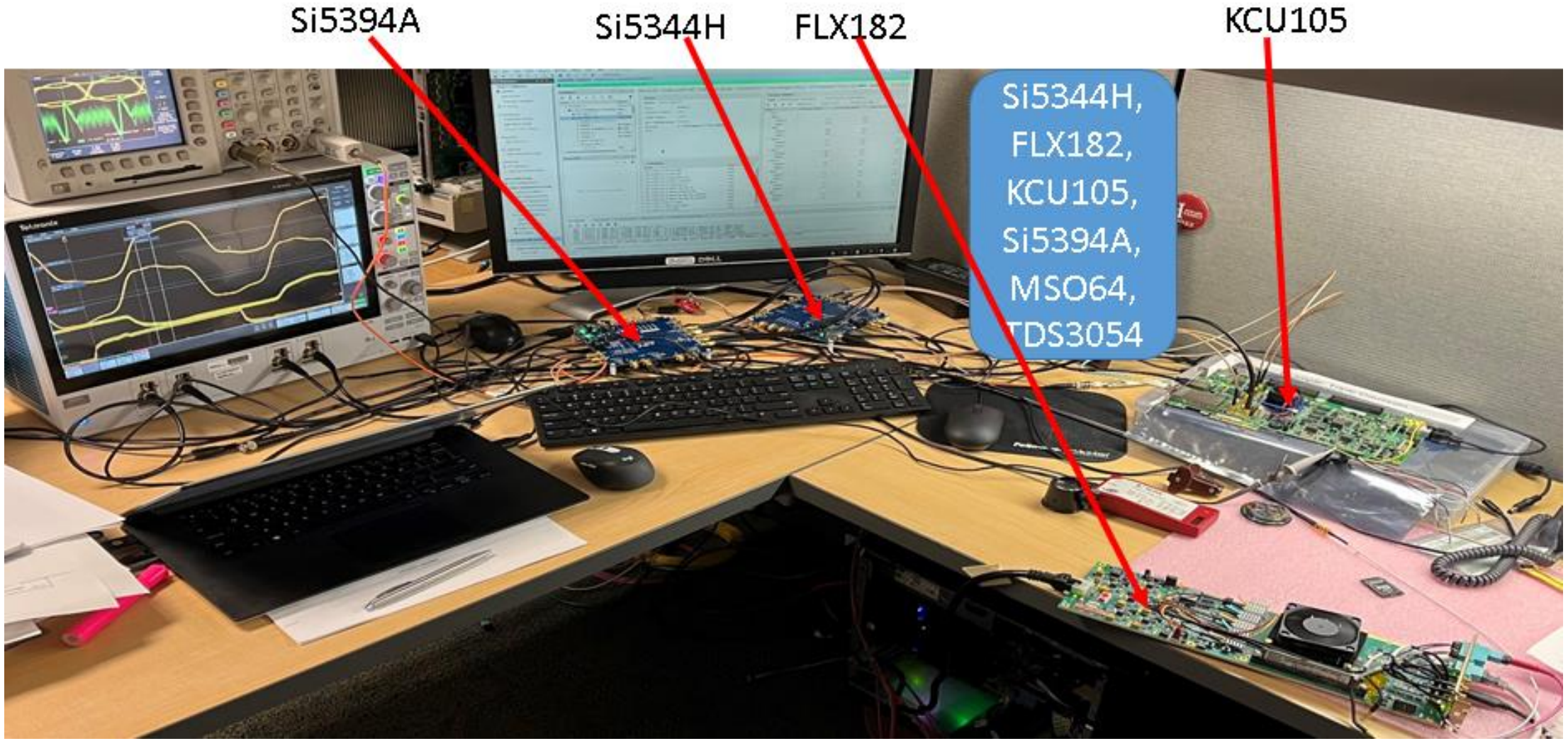
2.4.2 Beam Crossing monitoring and digital feedback to the GTU.

To collaborate with EIC.



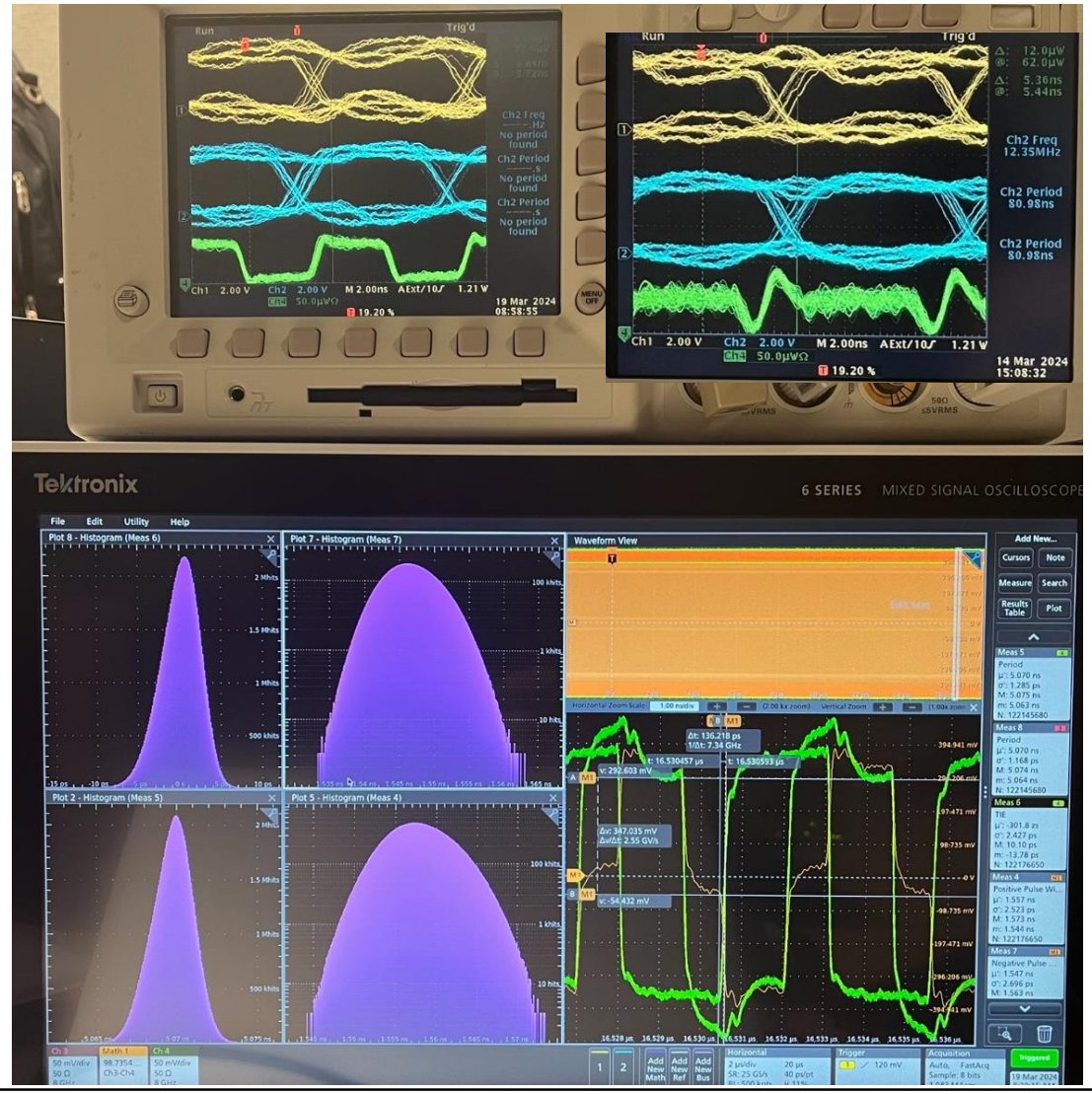
3. Test results

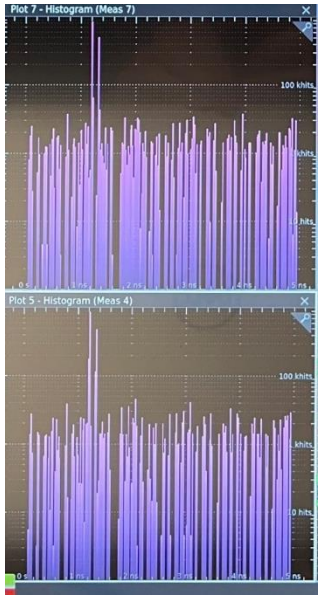
3.1 RDO MGT_RxRECovered clock



3. Test results

3.1 RDO MGT_RxRECovered clock





Si5344H → FLX182 → KCU105/XEM8320

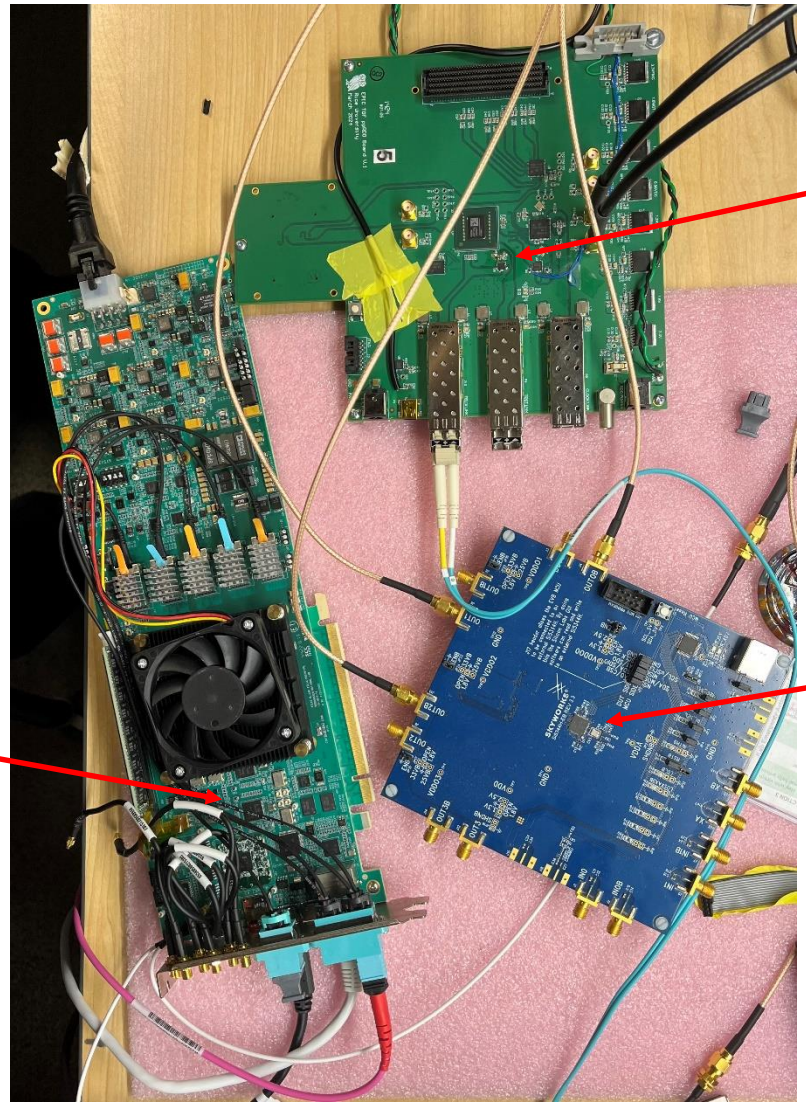
RxRECclk jitter < 3 ps (no jitter cleaner is necessary on the RDO)

RxRECclk phase can be fixed at ~(0)ps precision

(by measuring the phase difference between the RxRECclk and the pseudoClock, and resetting the RxRECclk CDR.)

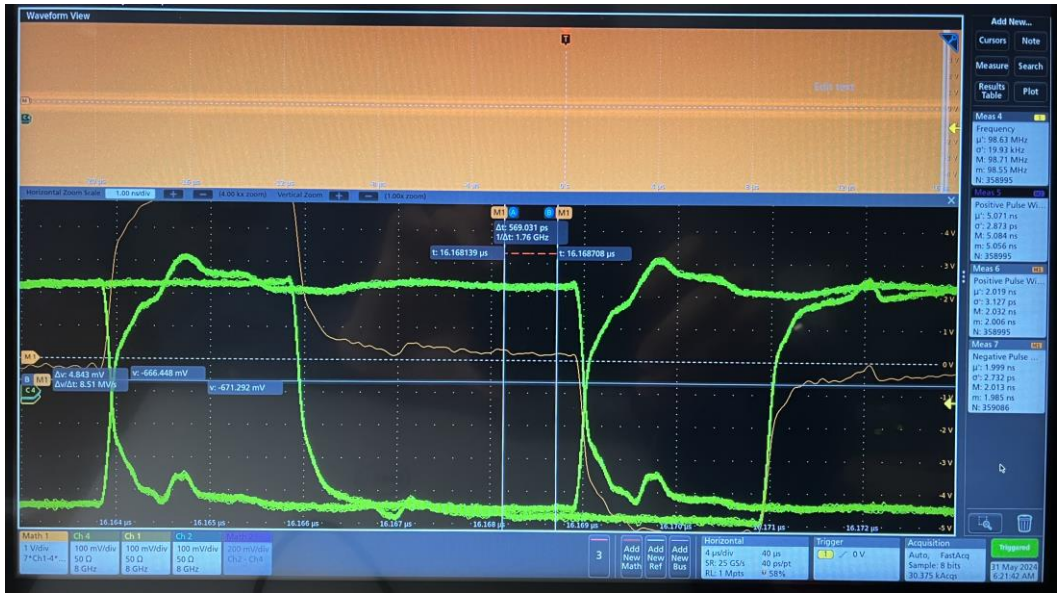
3. Test results

3.2 DAM TX serialized clock/control



Si5344 → FLX182 → ppRDO

(Reference_Clock → Txserilizer → PseudoClock)



Pseudo_Clock (TxSerializer and RDO_fanout):
Jitter: 3ps; Phase: stable

With AMD UltraScale Kintex FPGA test setup, the phase can be fixed to ~(O)ps using the RESET/Phase_measurement, but need be tested on the AMD Versal FPGA, which is used on the DAM.

3. Test results

3.3 Dedicated Clock from GTU to DAM

Jlab's 12GeV upgrade

Trigger SuperVisor

PCB and backplane
Copper traces

Signal Distributor

PCB and backplane
Copper traces

Trigger Distributor

Optic Transceivers
Multi-Mode fibers

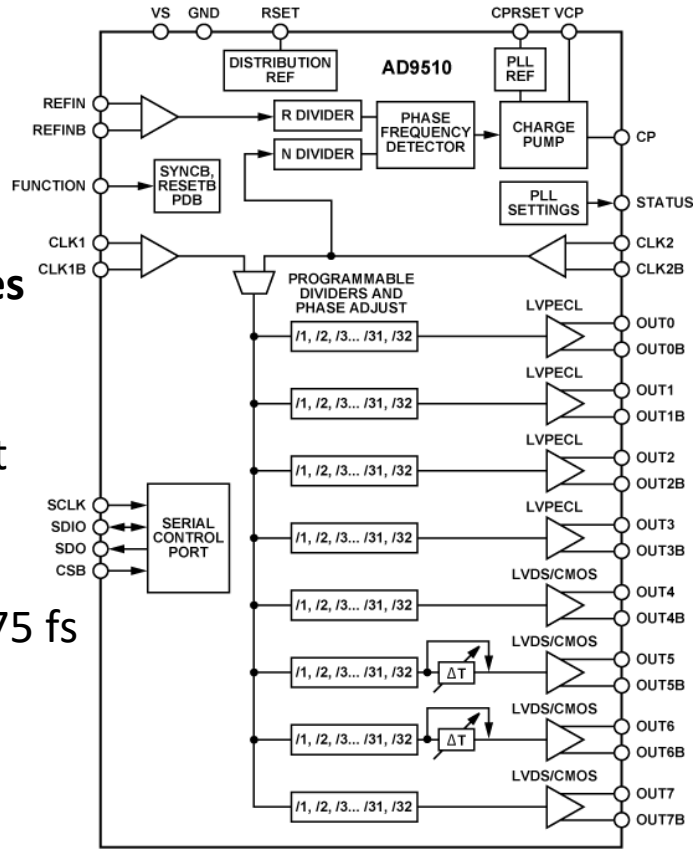
Trigger Interface

Clock Jitter (from Trigger Interface) σ < 3ps

3.4 Other clocks (lower f) from RDO to FEB/ASIC

Analog Devices AD9510

Additive output jitter (rms)
LVPECL: 225 fs
LVDS/CMOS: 275 fs

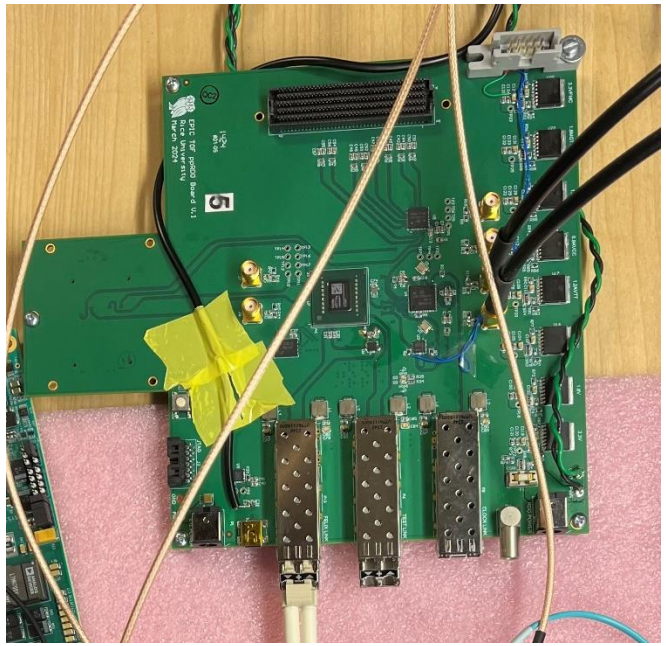


Used on the Trigger Interface modules to generate **SYNCHRONIZED** /2, /4, /6 and /8 lower frequency clocks

4. Summary

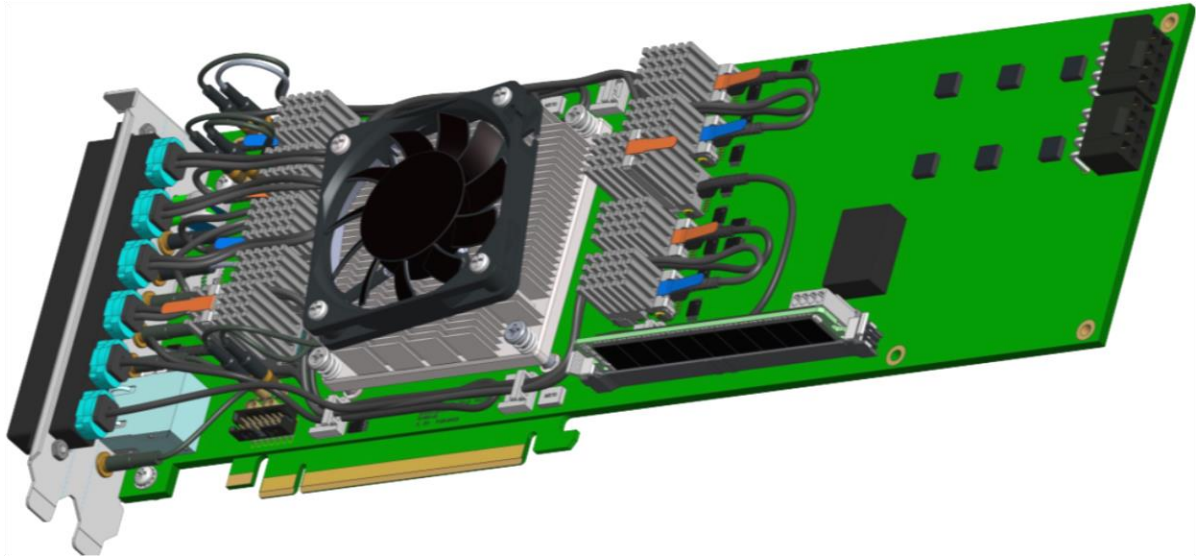
4.1 Status

4.1.1 RDO: preprotype RDO, **six in hands, being tested**



4.1.2 DAM: Prototype FLX155 (ePIC DAM) is expected this year

FLX155: Designed for **ATLAS** FELIX upgrade,
it is consistent with EIC/ePIC schedule.

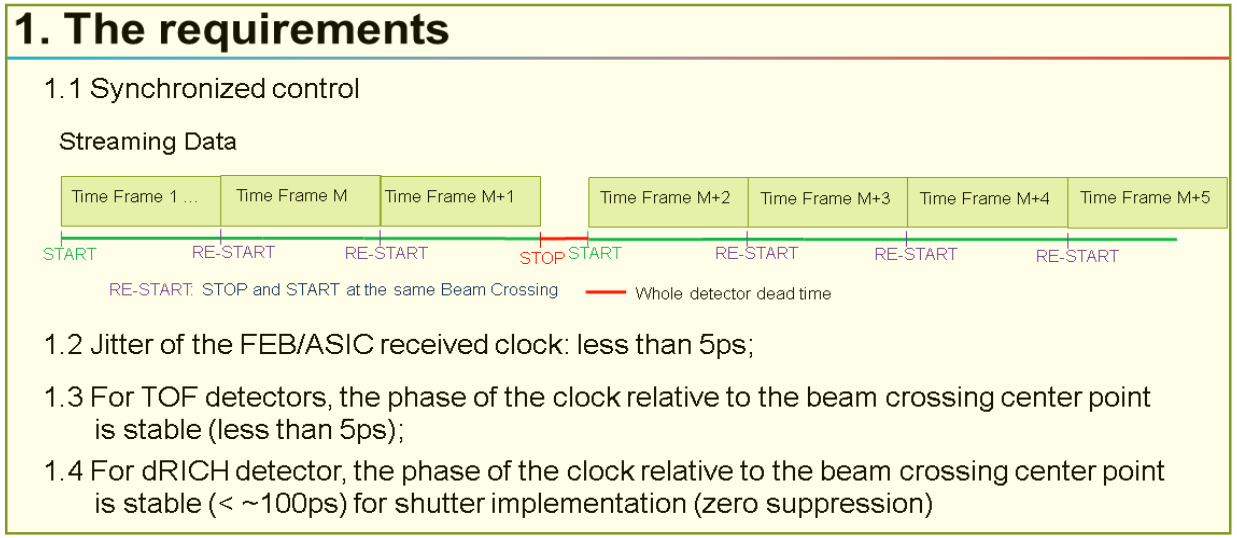


4.1.3 GTU: prototype is being considered
we plan on finalizing the development in 2025.

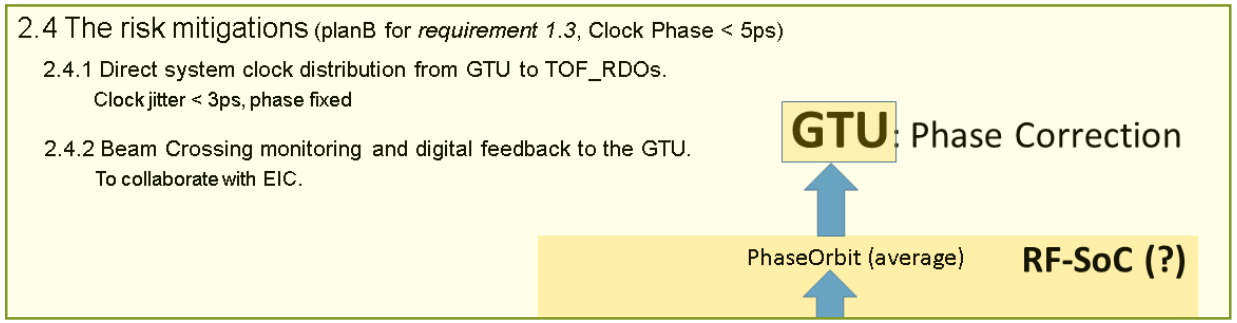
4. Summary

4.2 Conclusion

4.2.1 The design can satisfy all these four requirements, the tests and other experimental implementation proved that the requirements can be met.



4.2.2 More tests are needed to see if the risk mitigations (designed for *requirement 1.3*) are needed. The tests are expected to finish in 2025 with the new hardware.




BACK UP

Beam orbit cycle and ASIC clock requirement:

One orbit cycle = 1260 Beam Crossing (or ePIC system clock cycles)

1260 = 2x2 x 3x3 x 5 x 7 ; 1160 + 100 = 2x2 x 5 (58 + 5)

98.5 x 2 / 5 = 39.4 (MHz)

98.5 / 2 = 49.25 (MHz)

98.5 *4 = 394 (MHz)

……

Jitter and Phase measurement using an oscilloscope

EIC/Common Platform/GTU clock: Si5344H as reference;

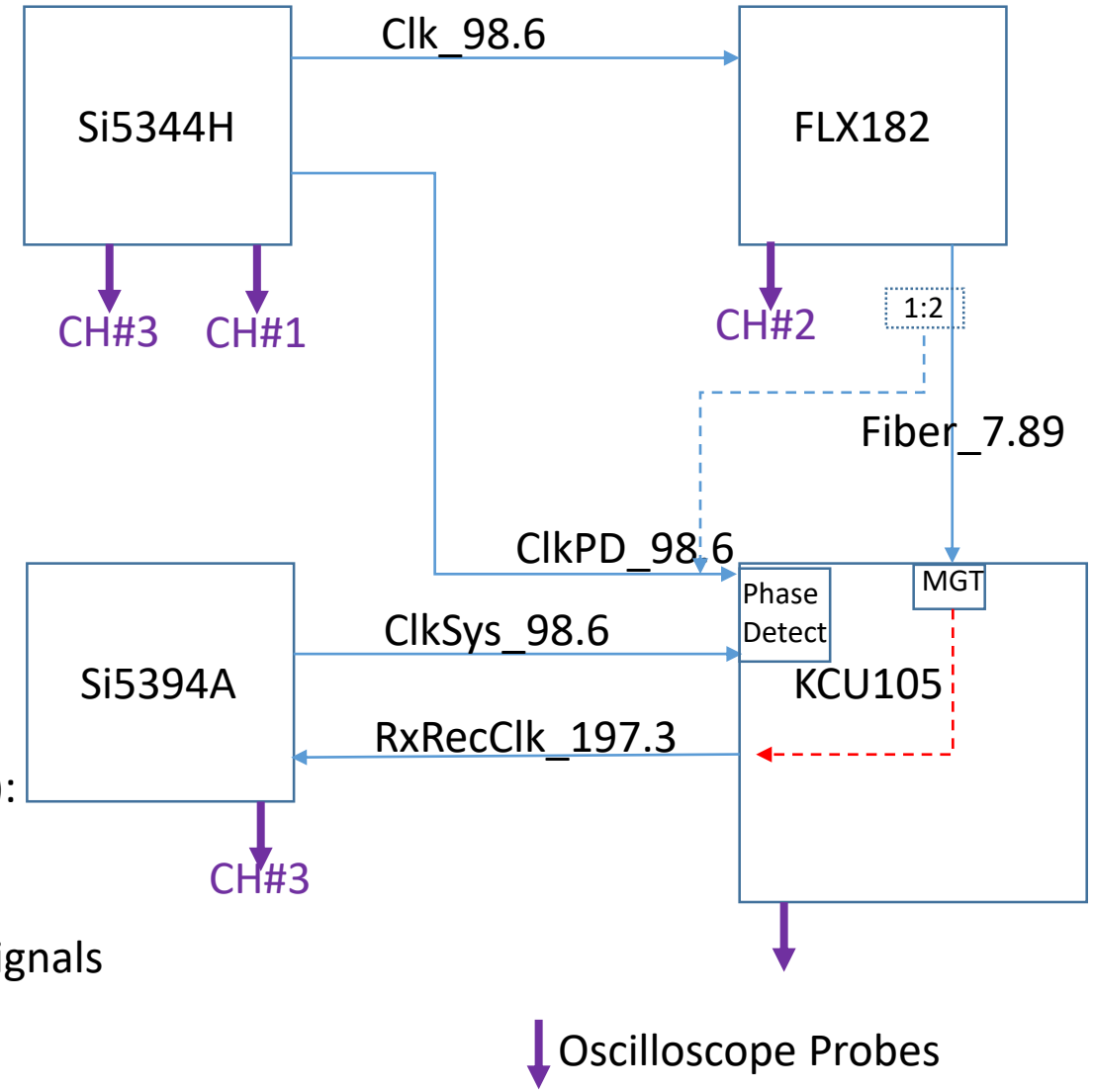
Beam Crossing/Reference Clock

DAM MGT_TX output: FLX182/KCU105 pseudoClock

Encoded Clock

RDO/FEB Recovered Clock: XEM8320/KCU105 plus Si5394A

Recovered Clock



Phase/Jitter measuring method using a scope (Tektronix MSO64):

Phase difference == WIDTH of the difference of the two signals
Jitter == uncertainty of the WIDTH of the difference of the two signals
assuming the reference clock is perfect.

Overall hardware design

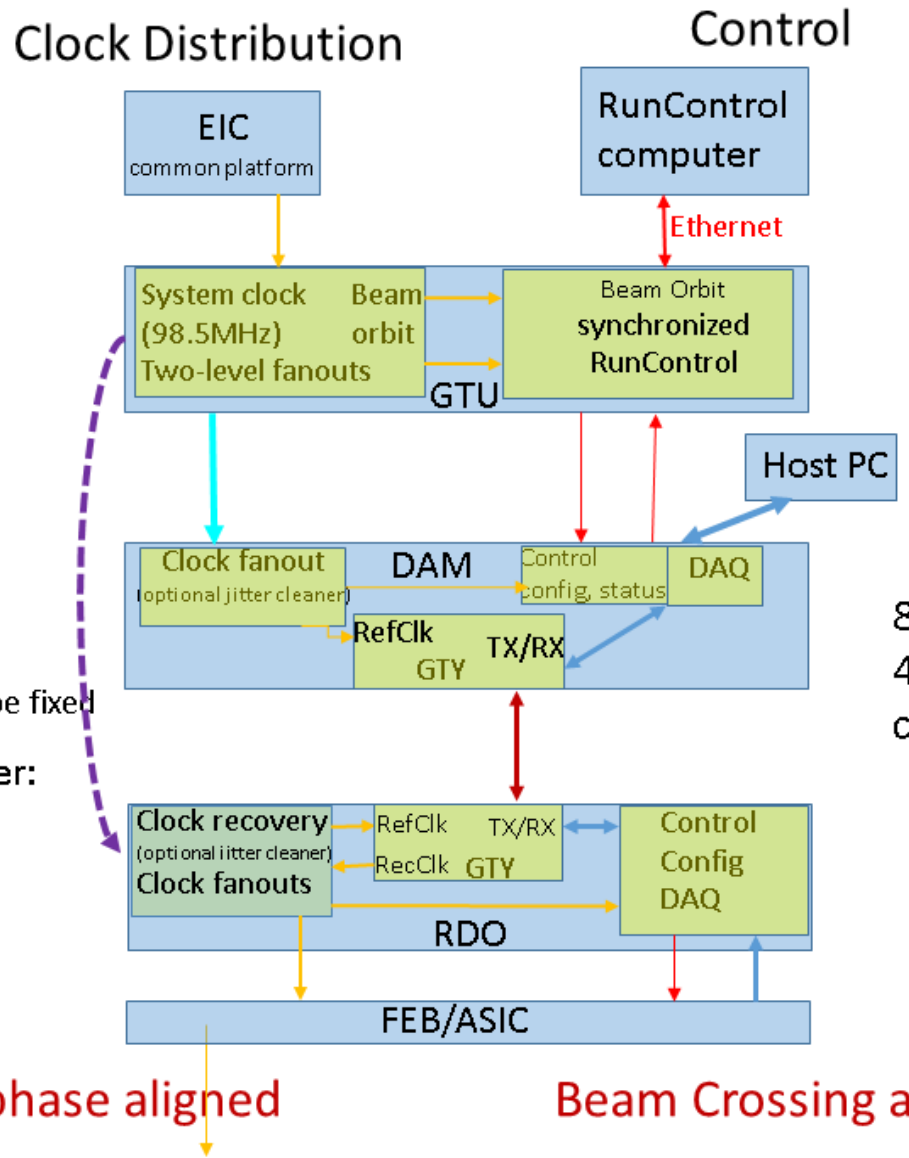
GTU fanouts (1:~200):
Additive Jitter <1ps; Phase: fixed

Dedicated (clock only, 197 Mbps) fiber
Additive Jitter <1ps; Phase: fixed

DAM fanouts (1:12):
Additive Jitter <1ps; Phase: fixed
MGT Clock/Control encoding (1:4):
Additive Jitter <~ps; Phase: stable, can be fixed

1:1 (Clock/Control, 7.88 (/3.94)Gbps) fiber:
Additive Jitter <1ps; Phase: fixed

RDO RECovered Clock:
Additive Jitter <3ps; Phase: stable,
fixed with PseudoClock



8-bit, 24-bit, 32-bit,
48-bit, 64-bit every
clock cycle (10.15ns)