Istituto Nazionale di Fisica Nucleare
INFN BOLOGNA

dRICH RDO – VTRX+
Interface document

V 1.0
June 6th 2024

Revision History

Rev.	Date	Description	Author
1.0	June 6, 2024	First version	P. Antonioli

1. Introduction

The VTRX+ is an optical transceiver engineered by CERN: it has been designed as implementation of a generic front-end link for HL-LHC applications.

All R&D and qualification procedures for this component are under CERN responsibility. The reader of this document should always refer to CERN documentation for VTRX+ specifications.

The ePIC dRICH DSC pointed out to EIC project/DAQ group already in June 2023 the advantages of using this component in dRICH RDO and the need of an early procurement (given the production schedule foreseen by CERN for this component).

The VTRX+ is selected by dRICH DSC as the optical transceiver for dRICH RDO because addresses several requirements:

- small size (20 x 10 x 1.25 mm^3)
- radiation tolerance (up to 1 MGy)
- enough bandwitdh (10 Gbps on TX)
- low power consumption (1 TX + 1 RX: 156 mW)

2. VTRX+ specifications

CERN main entry points for VTRX+ documentation are:
https://espace.cern.ch/project-versatile-link/public/default.aspx
https://espace.cern.ch/project-Versatile-Link-Plus/SitePages/Home.aspx

Relevent documents are:

- Versatile Link Plus Specifications
- VTRX+ Application Note
- VTRX+ Power Consumption

3. VTRX+ interface with RDO

The VTRX+ will be mounted on dRICH RDO. Current pre-placement of components in dRICH RDO design uses 3D CAD model of VTRX+ and footprint available from CERN documentation. The VTRX+ (highlighted in red rectangle in Fig. 1) is placed on RDO TOP side, right corner.

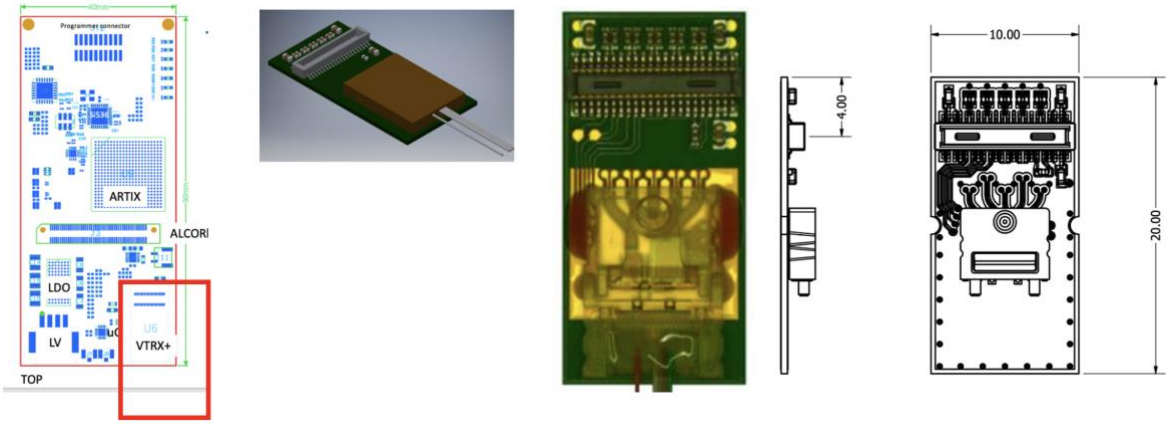

Fig. 1: RDO components pre-placement (left) andVTRX+ 3D model and footprint of the connector HIROSE DF40HC(4.0)-40DS-0.4V

Table 2 reports all signals that will be connected to the RDO.

Pin #	Name	Description	Pin #	Name	Description
1	VCCR2V5	2.5V Power supply for TIA	2	n/c	
3	VCCR2V5	2.5V Power supply for TIA	4	RSSI	RSSI current output from TIA, to be pulled up via a resistor to VCCR2V5
5	GND	Ground	6	GND	Ground
7	RXN	Rx output	8	SDA	I2C data (to be pulled-up to VCCT1V2)
9	RXP	Rx output	10	SCL	I2C clock (to be terminated to VCCT1V2)
11	GND	Ground	12	GND	Ground
13	TX1N	Tx Ch.1 input	14	RSTN	Laser Driver Reset
15	TX1P	Tx Ch.1 input	16	DIS	Laser Driver Disable
17	GND	Ground	18	GND	Ground
19	TX2N	Tx Ch.2 input	20	n/c	
21	TX2P	Tx Ch.2 input	22	n/c	
23	GND	Ground	24	GND	Ground
25	TX3N	Tx Ch.3 input	26	n/c	
27	TX3P	Tx Ch.3 input	28	n/c	
29	GND	Ground	30	GND	Ground
31	TX4N	Tx Ch.4 input	32	TH1	10k Thermistor Terminal 1
33	TX4P	Tx Ch.4 input	34	TH2	10k Thermistor Terminal 2
35	GND	Ground	36	GND	Ground
37	VCCT2V5	2.5V Power supply for Laser Driver	38	VCCT1V2	1.2V Power supply for Laser Driver
39	VCCT2V5	2.5V Power supply for Laser Driver	40	VCCT1V2	1.2V Power supply for Laser Driver

Table 2: signals connection of VTRX+

Connections to FPGAs are already set with all the 4 TX lines connected to MGT Artix I/O pins (even if dRICH RDO will use just 1 TX line). I2C interface will be connected to Polarfire FPGA due to reference voltage compatibility (no 1.5 V bank on Artix FPGA).

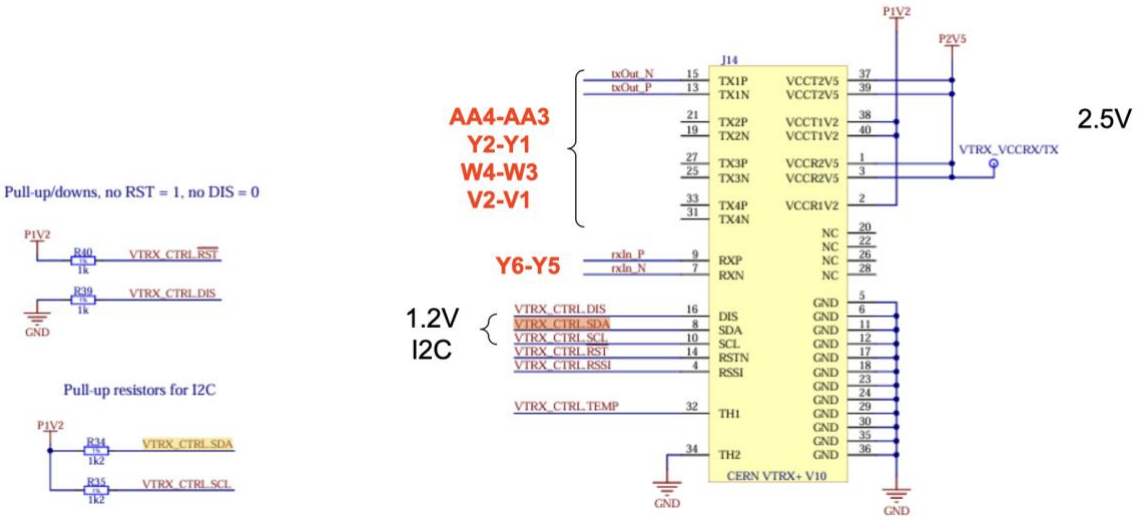

Fig. 3: connections to FPGA

Pigtail length has not yet been decided: CAD modelling of cables within dRICH detector box will be completed by December 2024, in time for CD-3B procurement. It is likely to be set to few cm.

4. Procurement and summary

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- INFN-BO has already in hands 20 VTRX+ (for RDO prototypes in 2024/2025) (and a VLDB+ card from CERN)
- VTRX+ procurement for dRICH from the project via CD-3B→ expected delivery end of 2026 fits dRICH RDO timeline
- consistently with RDO, dRICH needs **1500 VTRX+**
- if changes will happen to RDO design, the interface with VTRX+ will not change
- any RDO changes can easily adapt to the VTRX+ specifications (which are fixed) and described in section 3 of this document
- VTRX+ specifications are final

/ENDS