

# ppRDO Status – quick update for the TOF Electronics WG, 24-May-2024

- Received the H2GCROC evaluation board from Norbert (Calorimeters/ORNL), photo ⇒
  - We will use it to vet the FMC connector and also as an example of yet another CERN ASIC
    - ASIC is from the Omega group – same group which will design EICROC – advantage!
  - some issues with their placing of signals on the FMC connector (not as we previously agreed)
    - salvageable but postponed for now until TL has further discussions with Miklos et al (engineers of the board)
- Started discussing the EICROC digital backend with Omega designers
  - had a fruitful meeting → some outcomes:
    - 200 MHz clock
    - 200 MHz FCMD data lane (not DC balanced), can be distributed to 3+ ASICs, possible I2C-like configuration over the much faster FCMD link?
    - 400 Mbs data lanes, not DC balanced; 1 data link is enough for us
      - need to check Roman Pots and FF detectors
    - 32 bit words: header, data, trailer, idle
      - final(ish) data format should be decided ~end of June
    - I2C: 4 bits address, 1 MHz SCL max
  - same interfaces will be implemented for the CALOROC ASIC which will be available sooner than EICROC2
  - should get the VHDL model from the designers
  - also, possible involvement of TL in providing VHDL models of our liking to the ASIC group... TBD...
- ETROC integration using the ETL board (Mike, TL)
  - setup installed in a Rice lab, ready for remote development (Mike)
    - NB: I'd rather like to have our own PC and setup (hint to Wei :-))
  - IDLE token data decoded successfully at 320 Mbs... (TL)
  - NOTE: main goal is to gain understanding on the CERN ASIC interfaces...
  - in progress right now (TL)
- Setting up a common Xilinx project scheme (TL)
  - should be ready today for William's use next week(s)
  - [https://docs.google.com/document/d/1bdo2RbXJdUwK\\_nxDsXr\\_IFWeVSjTV-fdiJ-1Zg\\_IFHc/edit?usp=sharing](https://docs.google.com/document/d/1bdo2RbXJdUwK_nxDsXr_IFWeVSjTV-fdiJ-1Zg_IFHc/edit?usp=sharing)
- Other topics
  - Electronics & DAQ Preliminary Design & Safety Review – June 10/11
    - William for timing, TL for ppRDO eRD109
      - page turning – next Fri
      - rehearsal – June 5
  - DC/DC radiation evaluation (Tim & Gerard)
    - all DC/DC converters performed poorly – died at <~ 30% of expected fluence
    - looking again at CERN's bPOL48 & bPOL12
    - further testing will be necessary, should include all sorts of other parts
      - we should be involved
    - discussions in progress...

