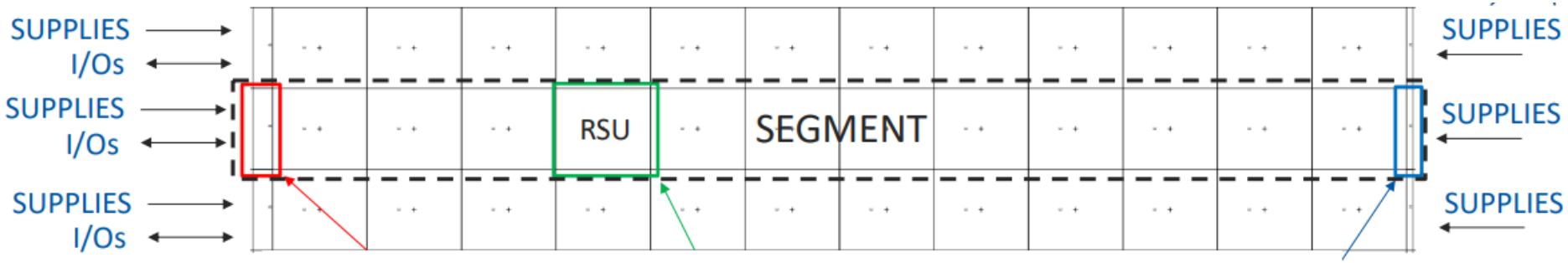
MOSAIX

Design / Block Status

João de Melo - BNL

MOSAIX - Top Integration Diagram



Alice/ITS3

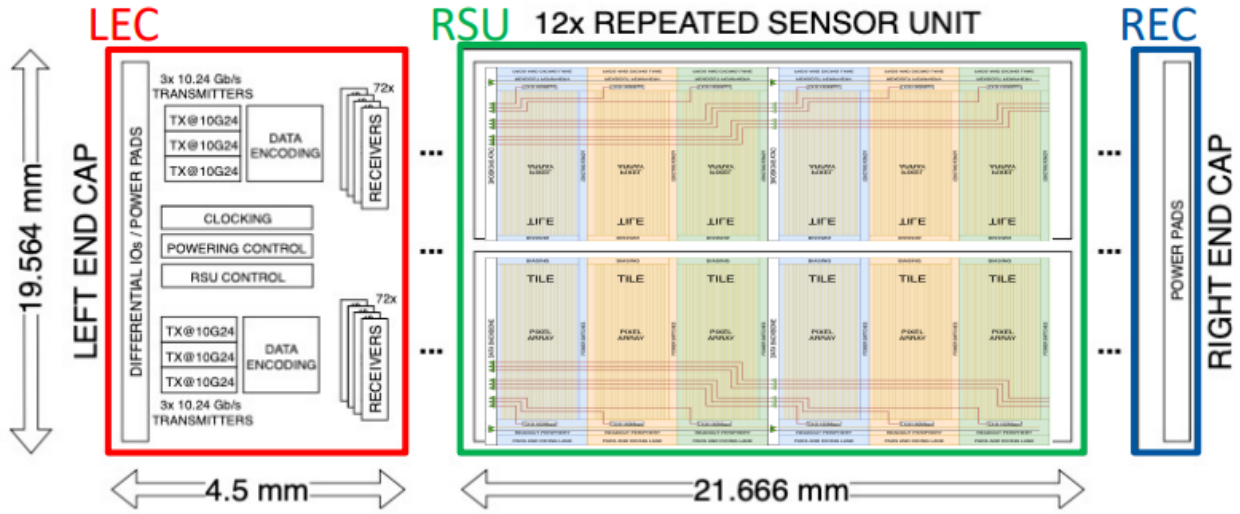
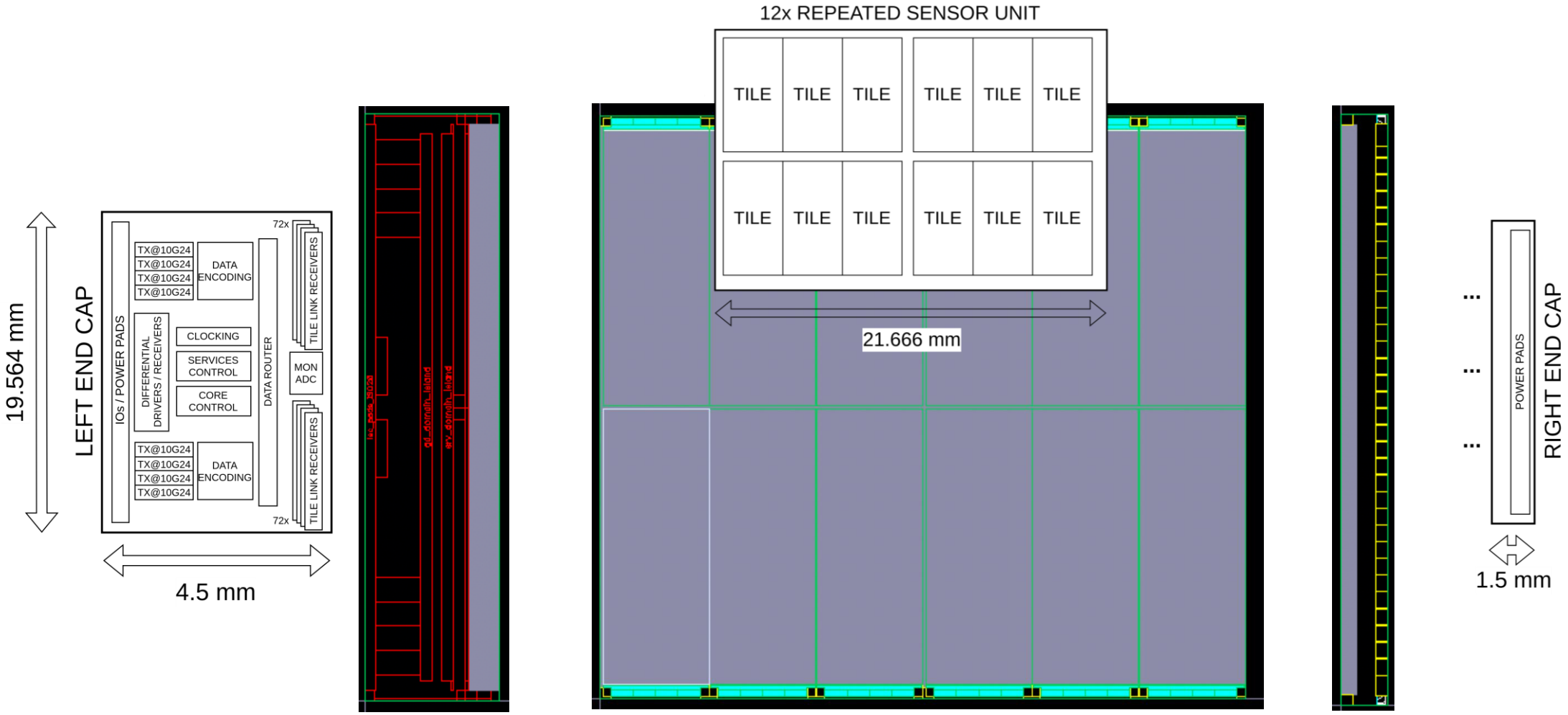
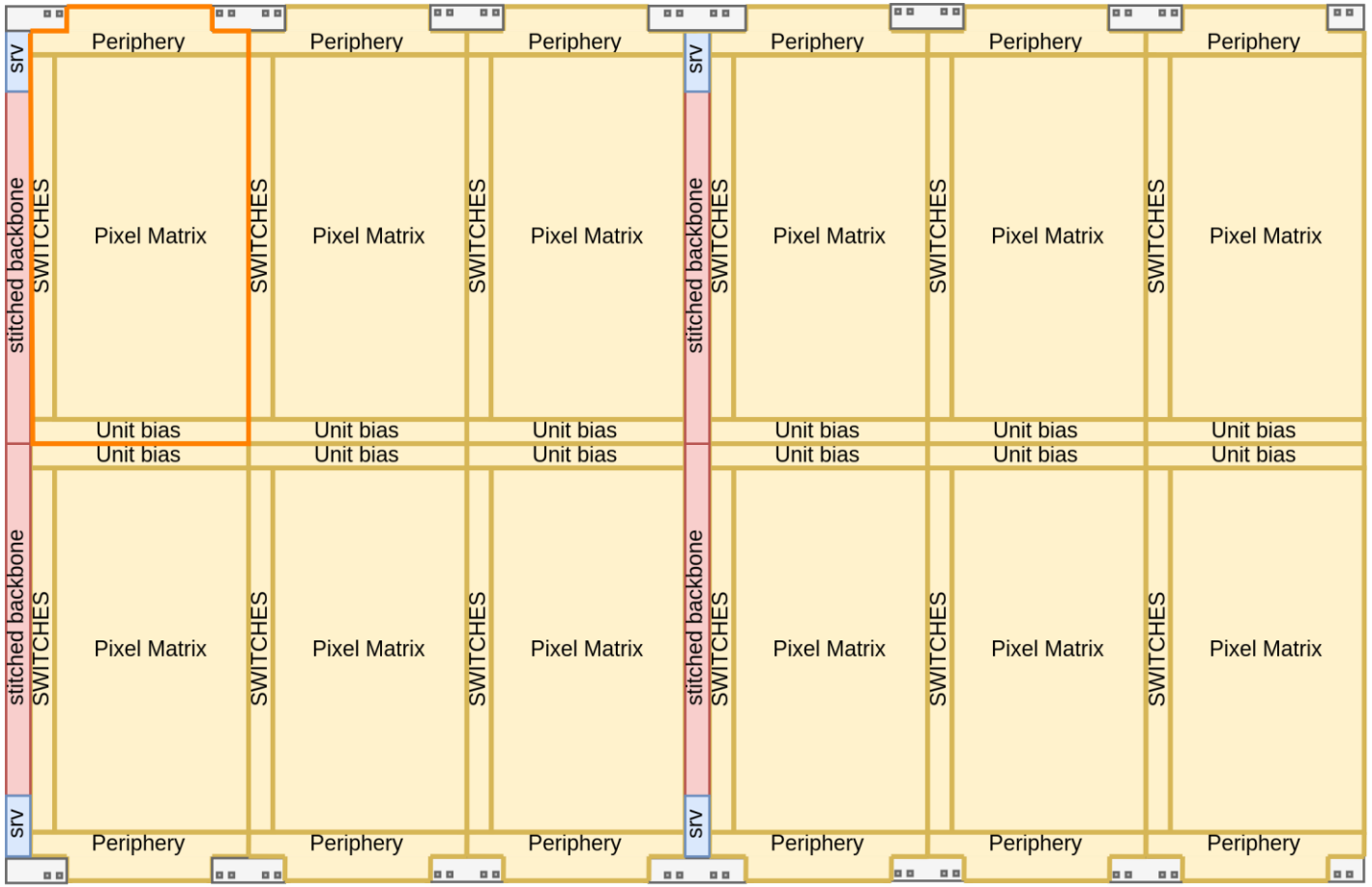


Figure 3.34: Block diagram of the sensor segment.

MOSAIX: Floorplan Views



MOSAIX: RSU Blocks



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MOSAIX: RSU Status

L0	L1	L2	Type	Status	Next milestone
RSU					
	Pixel Matrix		DIGITAL	INTEGRATING	Complete full matrix available
		Digital Pixel	DIGITAL	DONE	Verification
		Digital Column Basic	DIGITAL	DONE	Verification
		Digital Column Decoder	DIGITAL	DONE	Verification
		Analog Pixel Baseline	ANALOG	DONE	Verification
		Analog Pixel Variants	ANALOG	SPECIFYING	Design
	Biasing Unit DACs, Mon, Temp		ANALOG	INTEGRATING	Fully routed layout
	Power Switches		ANALOG	DONE	Verification
	Stitched Backbone RSU Block		ANALOG	LAYOUT	Complete layout
	Service Node		DIGITAL	RTL ONGOING	PnR flow
	Periphery		DIGITAL	PnR FLOW AVAILABLE	Complete PnR
		Pico Island	MIXED-SIGNAL	SPECIFIED	Design
		Readout and Control	DIGITAL	RTL ONGOING	Complete RTL
	RSU Floorplan and Powerplan		DIGITAL	DONE	Nothing
	RSU Implementation		DIGITAL	DRAFT FLOW	Complete implementation

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MOSAIX: LEC Status

L0	L1	L2	Type	Status	Next milestone
LEC					
	Stitched Backbone LEC		MIXED-SIGNAL	SPECIFIED	Schematic and Layout
	Monitoring ADC		ANALOG	STUDIED AND SPECIFIED	Schematic and Layout
	Serializer		MIXED-SIGNAL	COMPONENTS DESIGN	
		Analog Blocks	ANALOG	SCHEMATIC DONE. ENTERING LAYOUT	Complete layout
		Regulators	ANALOG	SCHEMATIC DONE. ENTERING LAYOUT	Complete layout
		Digital Blocks	DIGITAL	RTL DONE. DOING TMR	Complete block level design
		Top Integration	MIXED-SIGNAL	DRAFT PARTIAL FLOW	Complete flow
	LEC Core		DIGITAL	DRAFT FLOW	Complete implementation
		Data receivers	DIGITAL	RTL DONE	Verifying
		Data Encoder	DIGITAL	RTL DONE	Verifying
		Data Router	DIGITAL	RTL DONE	Verifying
		Slow Control	DIGITAL	RTL ONGOING	Complete RTL
		GWT-PSI controller	DIGITAL	RTL ONGOING	Complete RTL
		Testability features	DIGITAL	RTL ONGOING	Complete RTL
	Differential Transceivers		MIXED-SIGNAL	TODO	ASSIGN
	Pad Ring		ANALOG	DONE	

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MOSAIX: REC Status

REC				
	Stitched Backbone REC	MIXED-SIGNAL	SCHEMATIC DONE	Layout
	Pad Ring	ANALOG	DONE	

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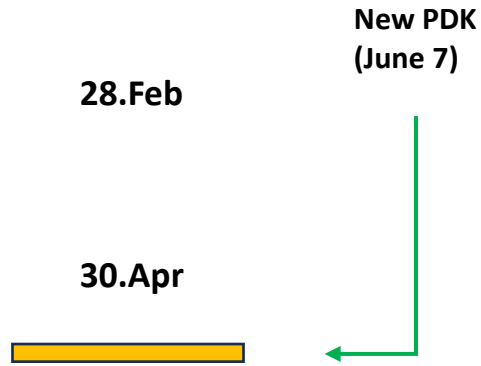
Top Level Design Milestones

❑Estimation plan (November 2023)

MOSAIX Top Integrated - Early stage	All top-level views include the early-stage schematic and layout views of the RSU, LEC, REC. Variants of tiles are foreseen. Missing blocks possible. Current (6M2Y) metal stack.	**28.Feb**
MOSAIX Top Integrated - Advanced stage	All top-level views include the advanced stage views of the RSU, LEC, REC. All blocks should be included. 6M2Y metal stack.	**30.Apr**
MOSAIX Top Integrated - Candidate	All top-level views include the candidate views of the RSU, LEC, REC. All blocks must be included and signed-off at block level. New (7M2L1F) metal stack. Mock submission possible.	**30.Jun**
MOSAIX Top Integrated - Ready to Submit	All design side sign-off criteria met. DRC, LVS, DFM, EMIR, Functional	**31.Oct**
ER2 GDS - Ready to Submit	Integration of MOSAIX and chiplets in full wafer gds	**31.Oct**



Thanks!