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U.S. DEPARTMENT OF ENERGY

Negative Voltage Generator (NVG)

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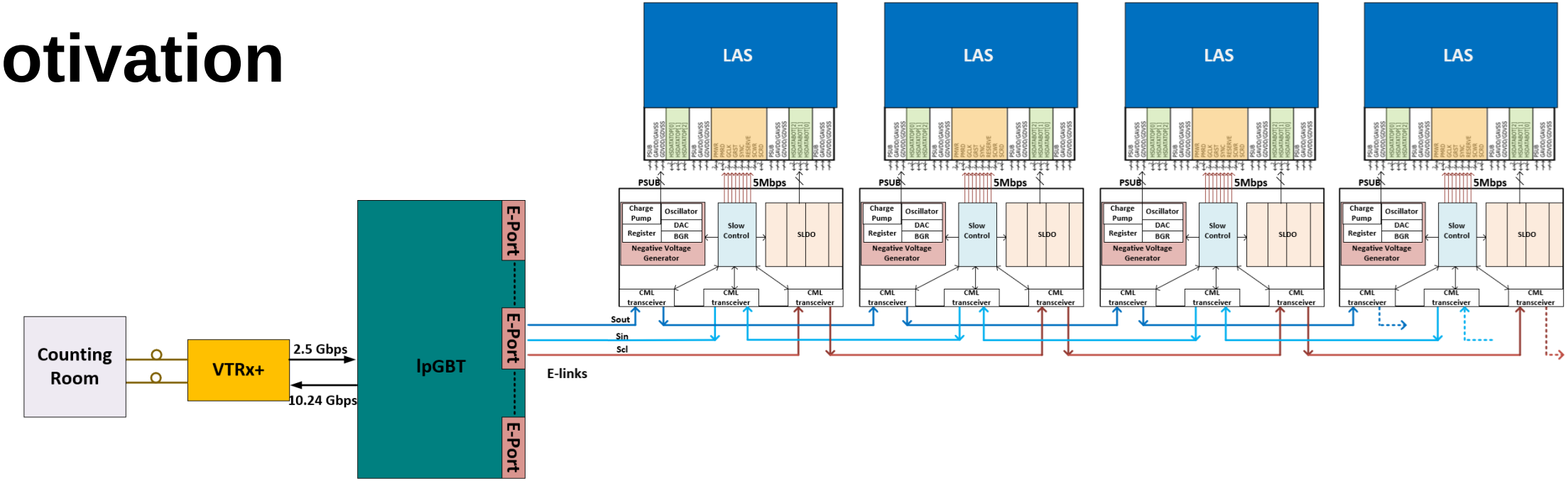
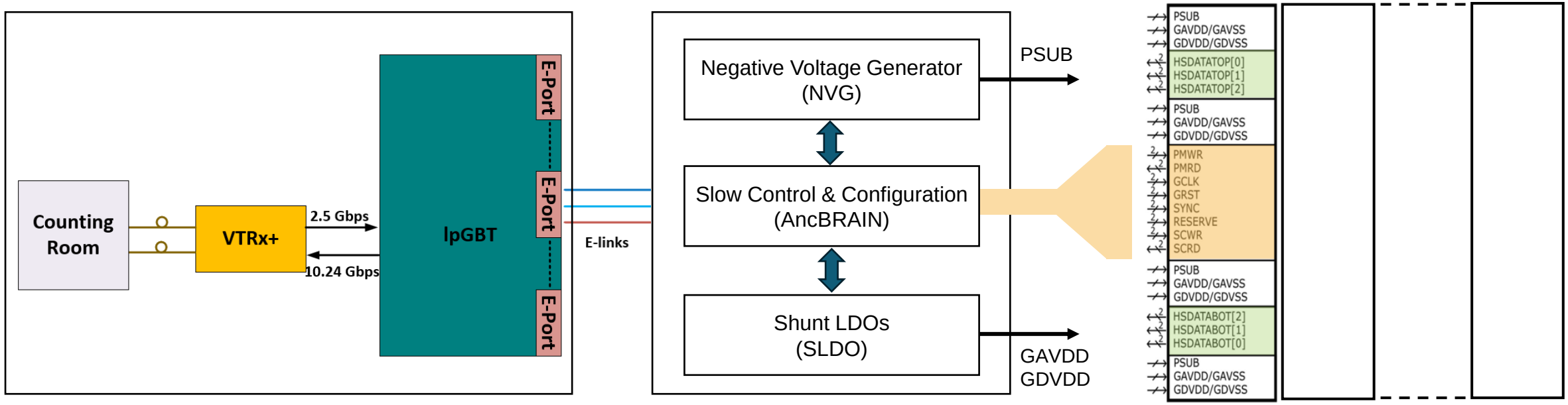
Motivation



- Serial powering has been selected as the powering scheme for ePIC SVT outer barrel & disks
- Current-based powering scheme
  - module are powered in series by a constant current
- Each module is at a different ground potential inside the chain
  - needs separate substrate bias for each module

Ancillary ASIC



Readout / Control **Ancillary ASIC** **LAS**

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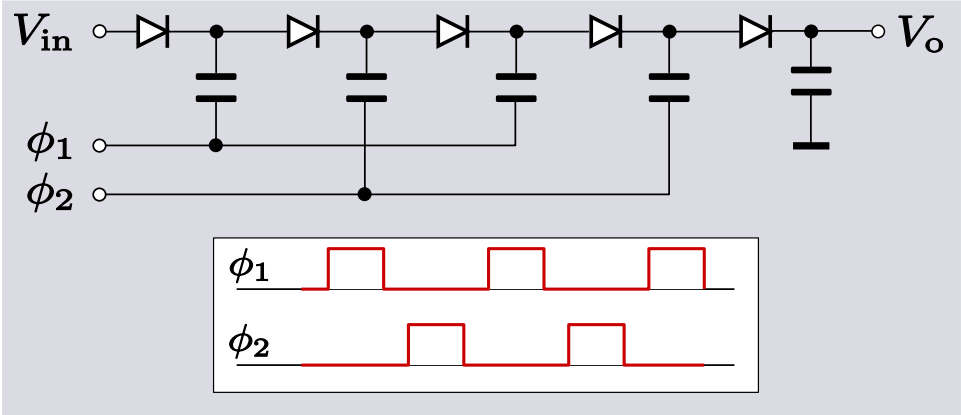
Negative Voltage Generator (NVG)

- MOSFET-based charge-pump circuit
- Dickson-style
  - RF signal is fed in parallel
  - DC voltage across each capacitor equals V_{OUT}, limiting the maximum output voltage.
  - Output impedance increases less rapidly since the capacitors are in parallel.



Dickson charge pump

Specification	Value
Voltage range	0 to -6 V
Current capacity	1 mA
Voltage ripple	< 0.1 mV

Negative Voltage Generator (NVG)

- Simple ring VCO using current-starved inverters to adjust the RF drive frequency
- Allows the oscillation frequency range to be adjusted to ensure a monotonic response

- Input
  - Enable/Pause
  - Coarse digital control + fine analog control
- Output
  - RF clock (100 – 800 MHz, 1.2V)

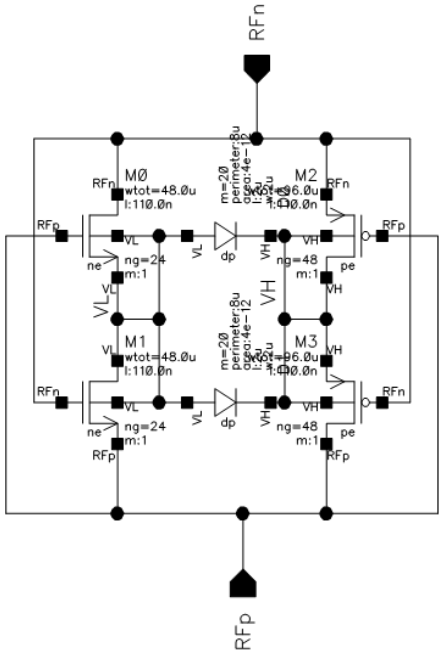
Negative Voltage Generator (NVG)

- Provides sufficient drive strength to distribute RF clock across the charge-pump
- RF driver split into 16 identical branches
  - Provides coarse control over output voltage
  - Reduces the required control range of the feedback loop

- Input
  - 4-bit control (thermometer coded)
  - RF clock (100 – 800 MHz, 1.2V)
- Output
  - RF clock (100 – 800 MHz, 1.2V)

Negative Voltage Generator (NVG)

- Four-transistor charge-pump cell
- DC output signal builds up between VL and VH
- RF signal injected between RFn and RFp
- Deep trench isolation (DTI) allows the negative output voltage (V_L) to go below the substrate potential
- Auxiliary diode between V_L and V_H ensures initial start-up



BUT, how to control the output?

We need to make sure V_{NEG} is equal to the desired PSUB voltage

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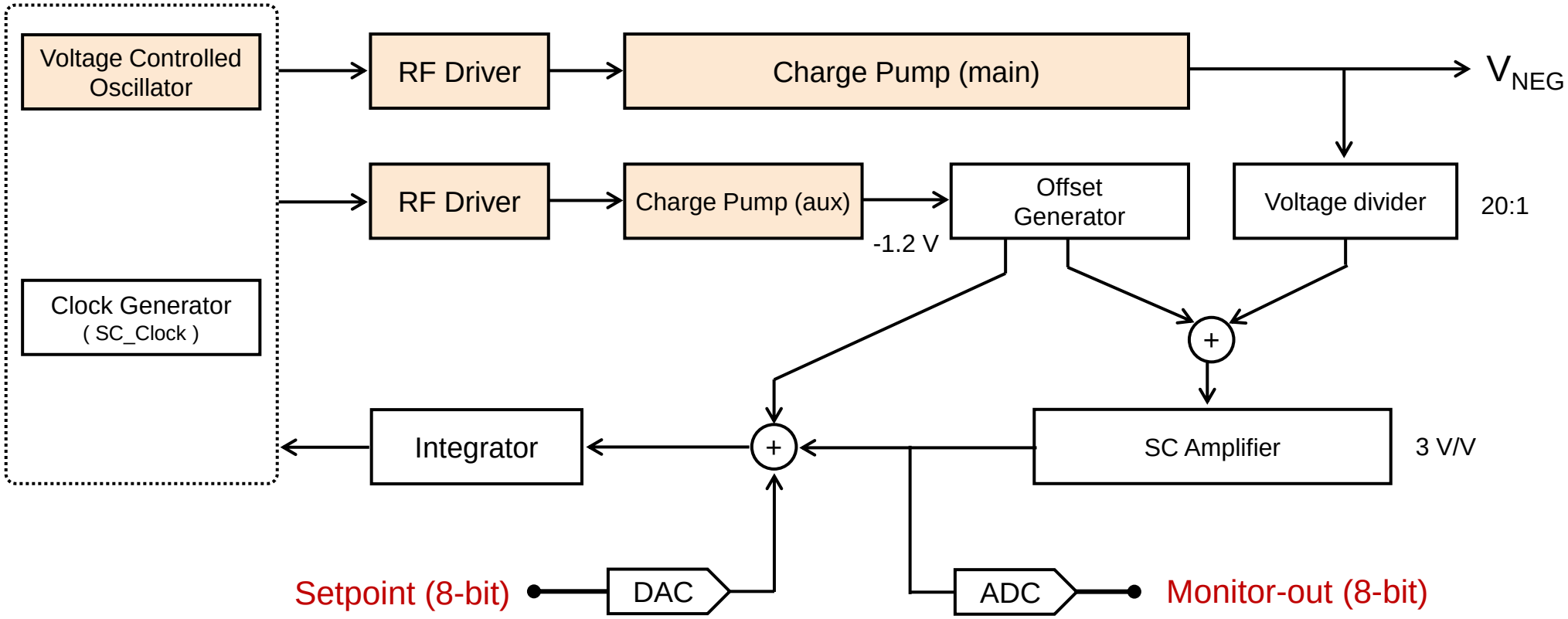
Negative Voltage Generator (NVG)

(with feedback control)



Blocks planned for September 2024 fabrication run

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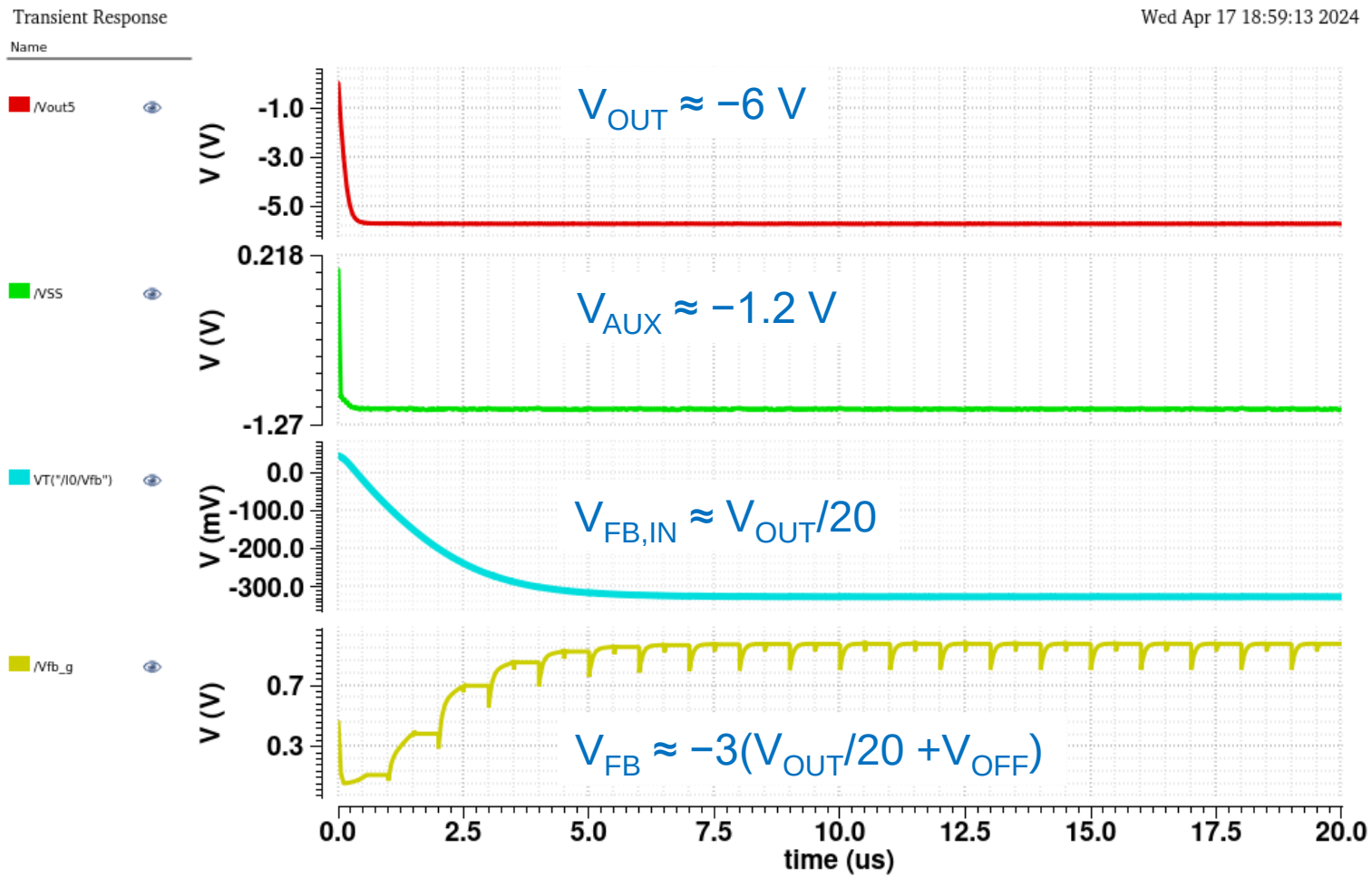
Current status

- **Open-loop simulation**

- RF frequency = 500 MHz
  Chosen to keep pump capacitor size reasonable
- Load current = 200 µA
- SC Clock Frequency = 1 MHz

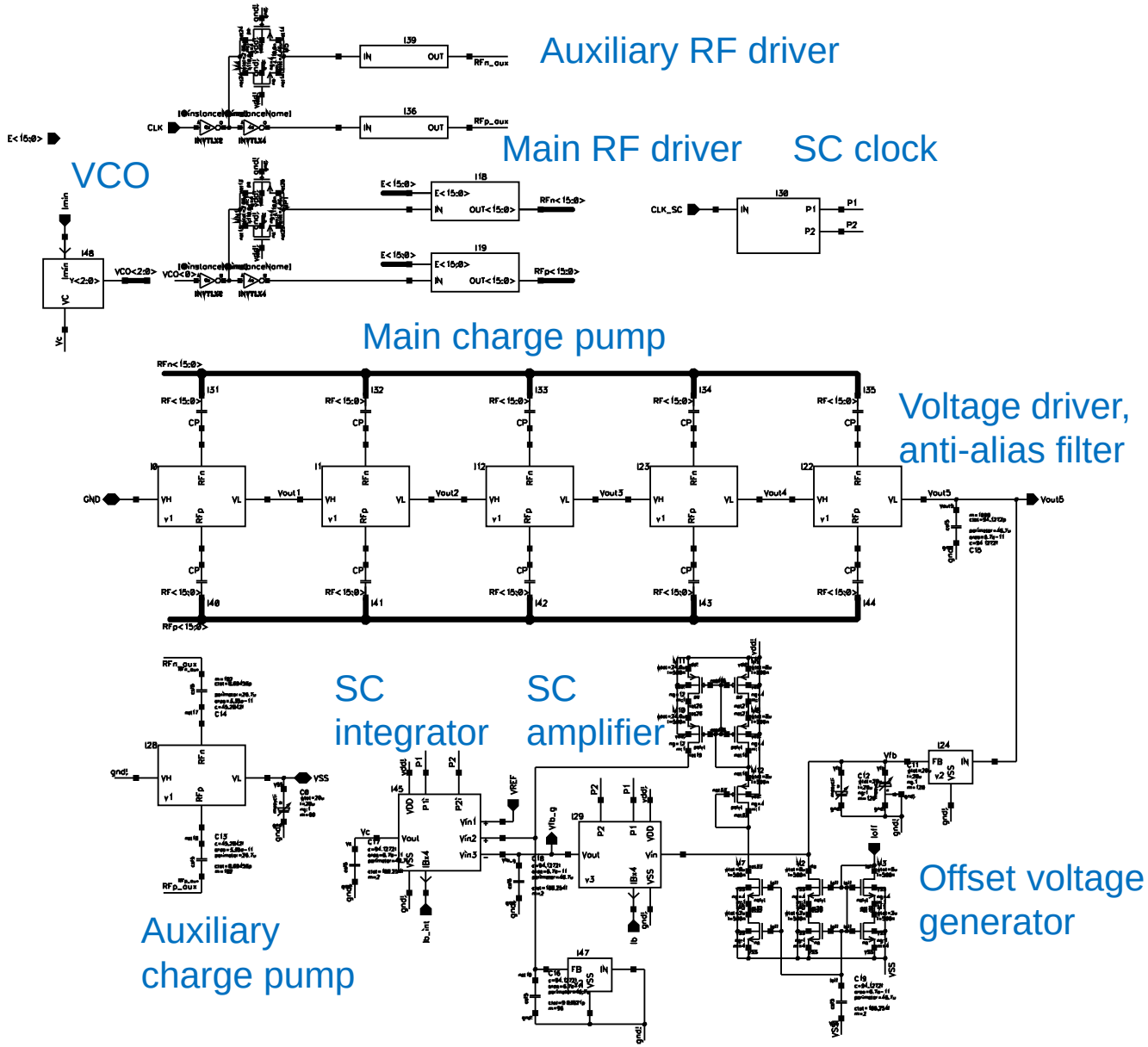


$V_{OFF} = I_{OFF}R_{FB} \approx 43$ mV

Current status

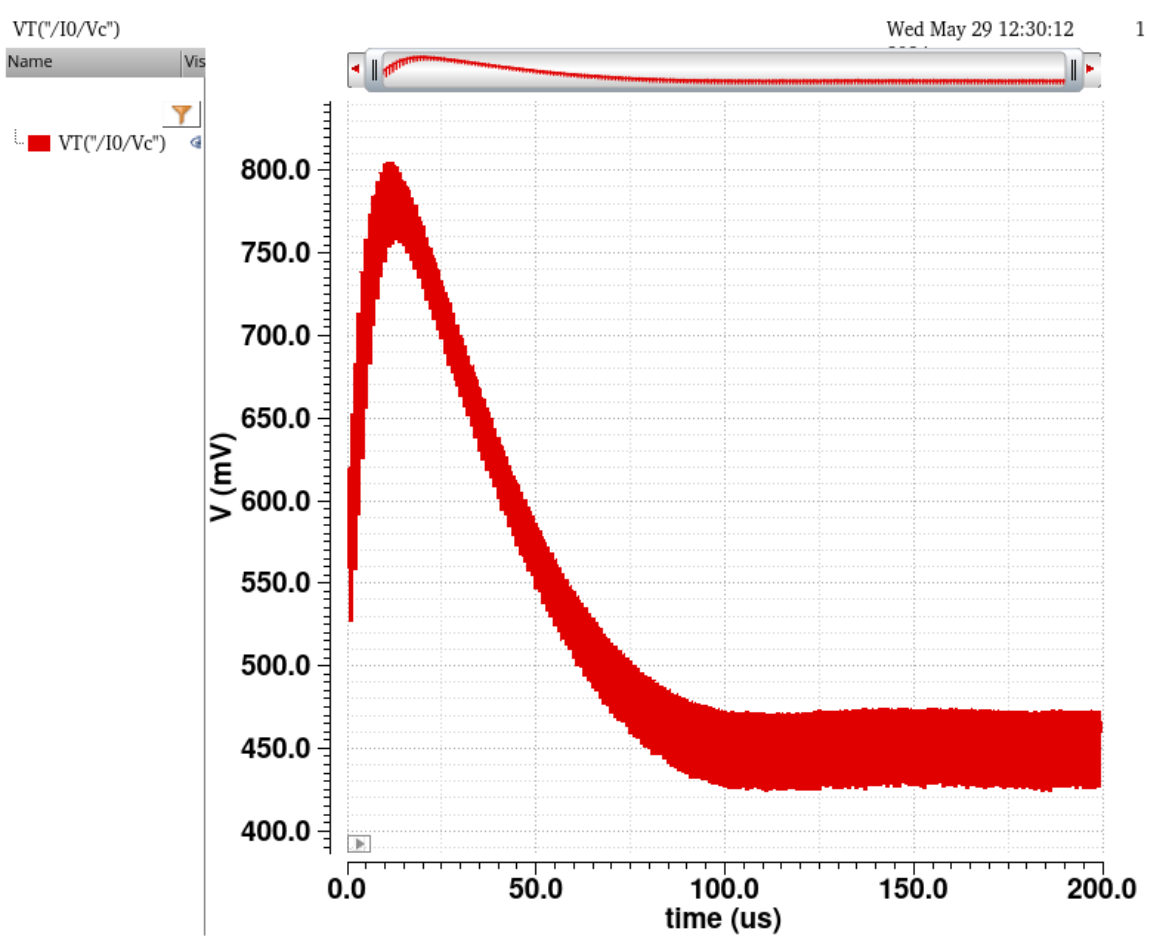
- **Closed-loop simulation**

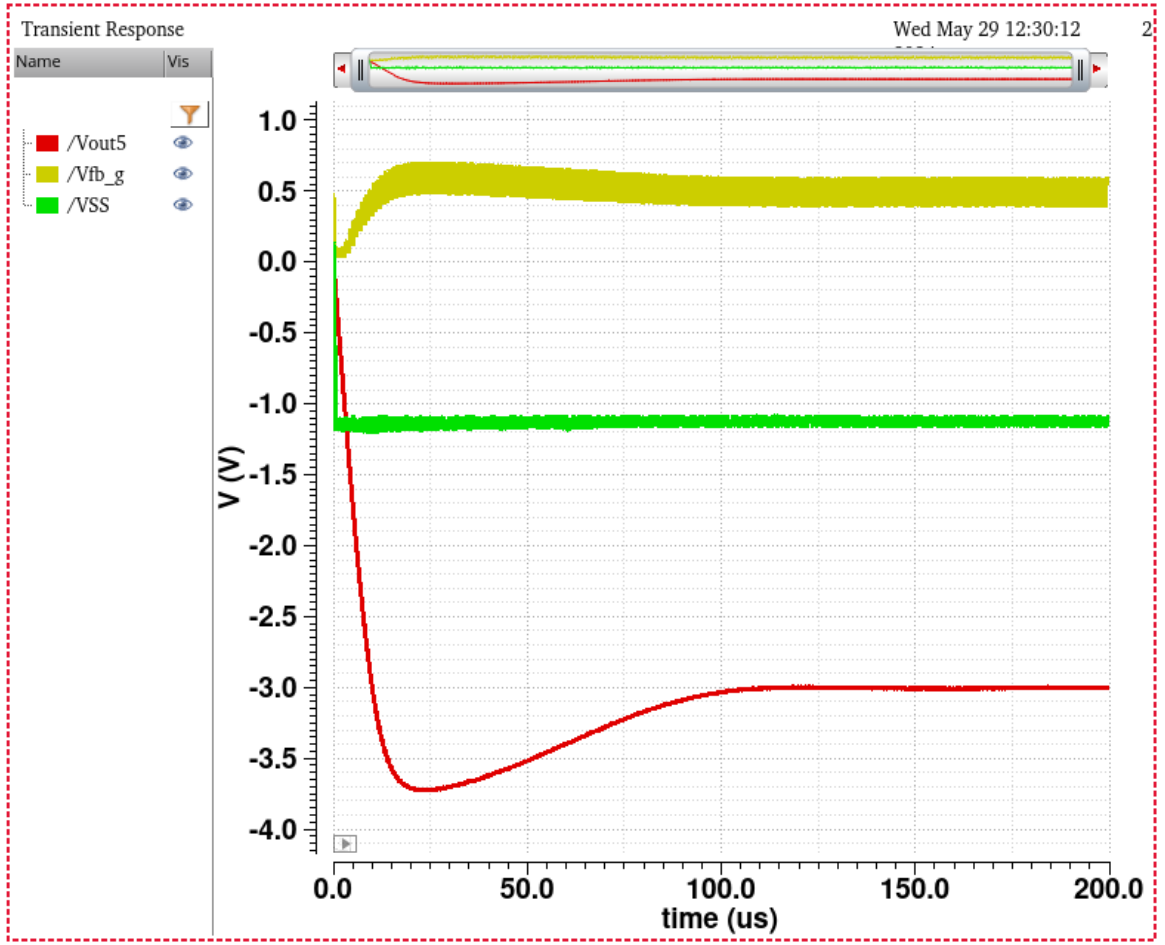
Completed preliminary simulations of the conceptual design



Current status

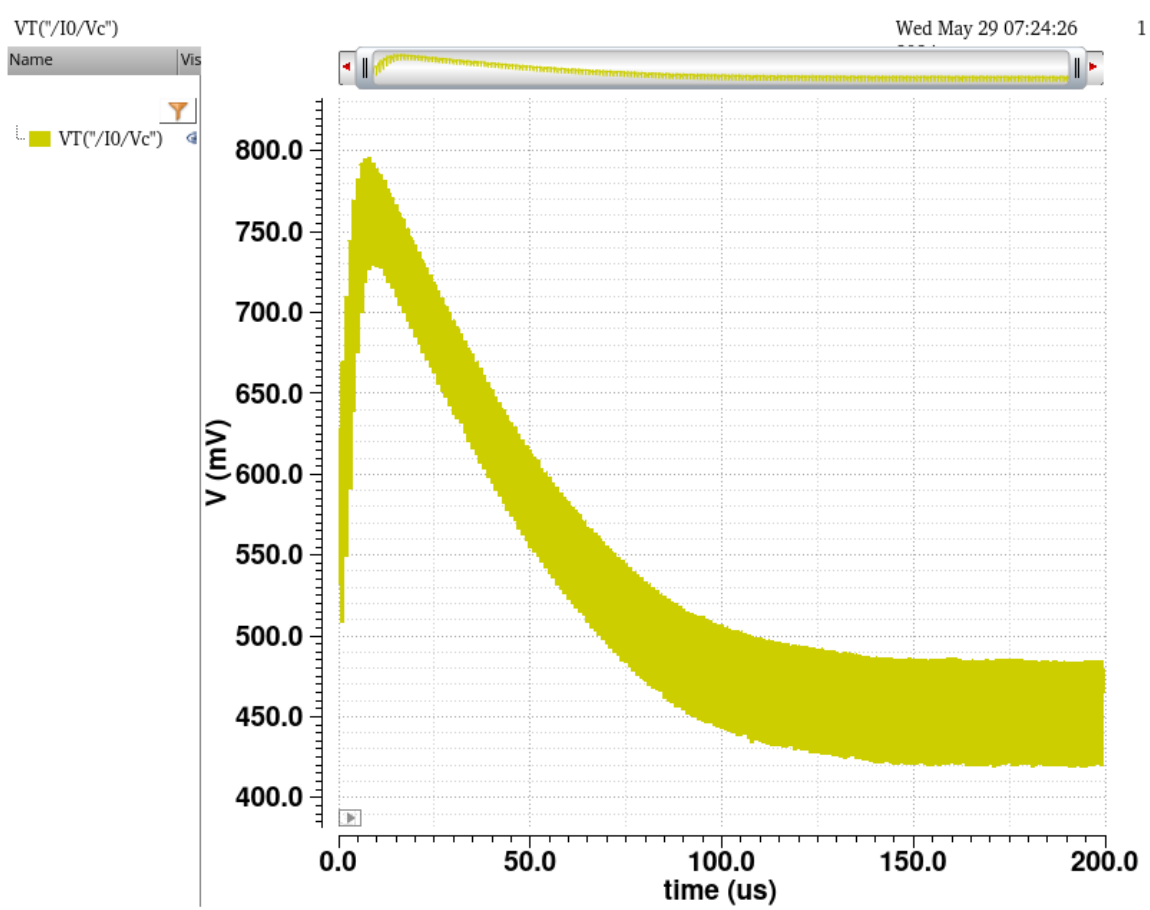
- **Closed-loop simulation**
  - Drive strength = 2, V_{REF} = 3 x (3/20) V = 0.45 V, should produce -3V

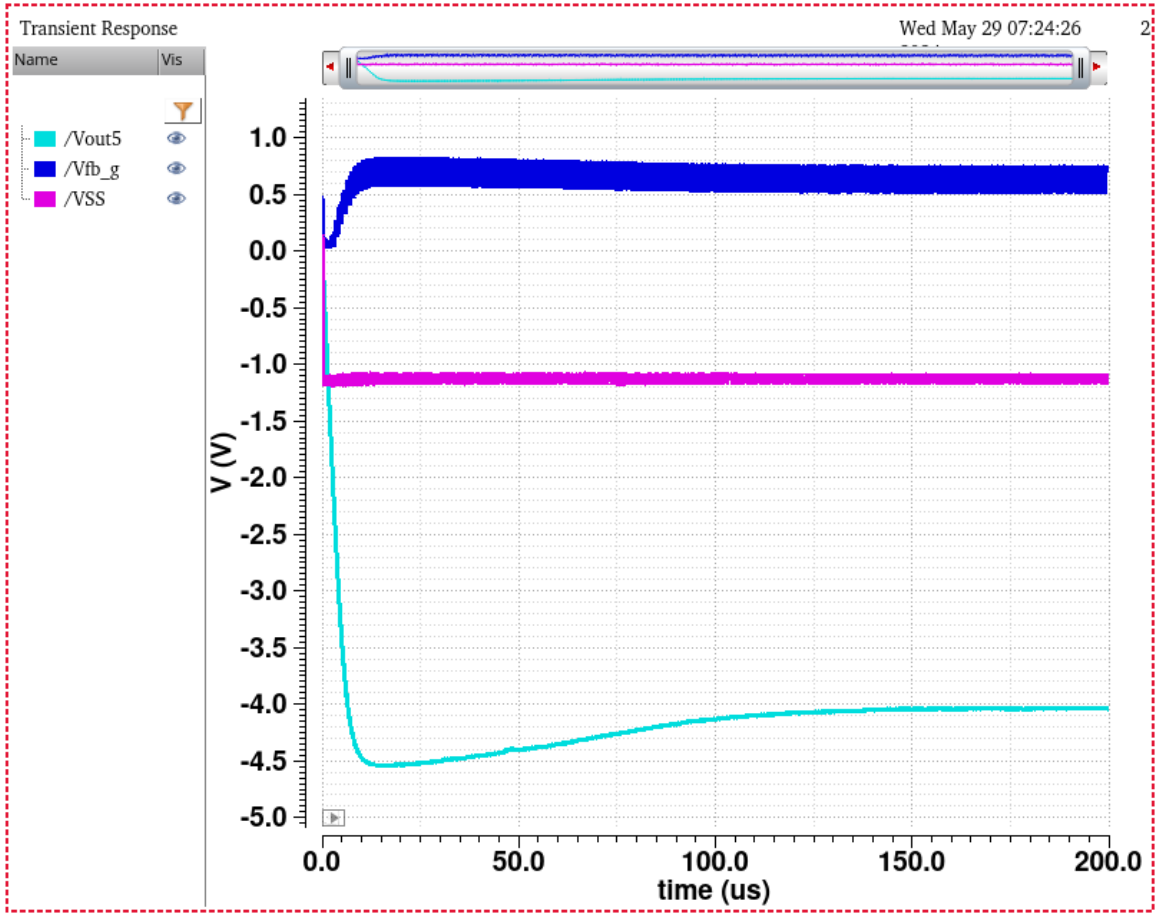




Current status

- **Closed-loop simulation**
  - Drive strength = 4, V_{REF} = 4 x (3/20) V = 0.6 V, should produce -4V

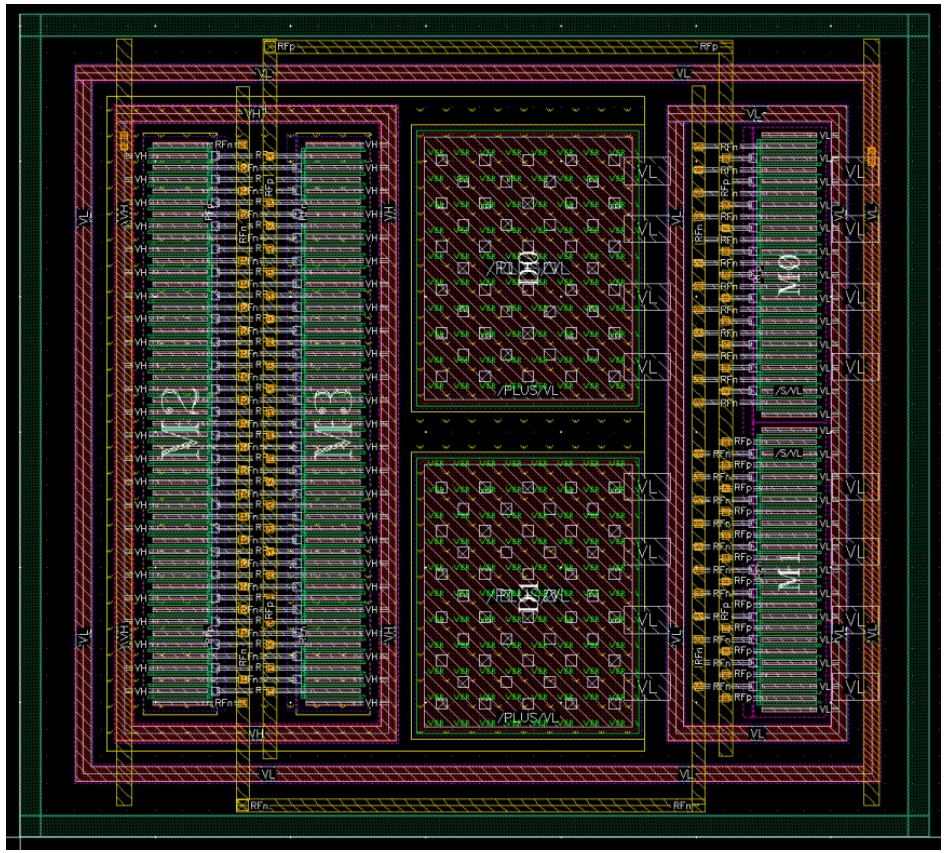




Current status

- **Layout design**

- **Started layout for September submission**
  - Finished initial layout of the charge-pump cell
  - DRC, LVS clean
  - Working on extracted simulations



Next Steps

- Obtain a more realistic estimate of the output load and capacitance, and optimize the design accordingly.
- Complete a trial layout and evaluate impact of layout parasitics.
  - Use TMR within digital blocks to improve radiation hardness.
- Evaluate alternate feedback mechanism using RF duty cycle
- Perform corner and Monte Carlo simulations
  - Document results for design hand-off

Required Design Efforts!

- Preliminary design ready
  - Two designers and one layout engineer working on NVG
  - Blocks needed for open-loop voltage regulation will be taped-out in September 2024
- Lot of work still needed on detailed simulation / layout design
  - Support for two people in FY25 is critical for on-time design completion
  - More is always better ☺

Thank you!