MOSS: MOnolithic Superconducting Spiking Readout for Scalable Single-Photon Detector Arrays

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FOA: LAB 24-3305, Area: Smart Detectors

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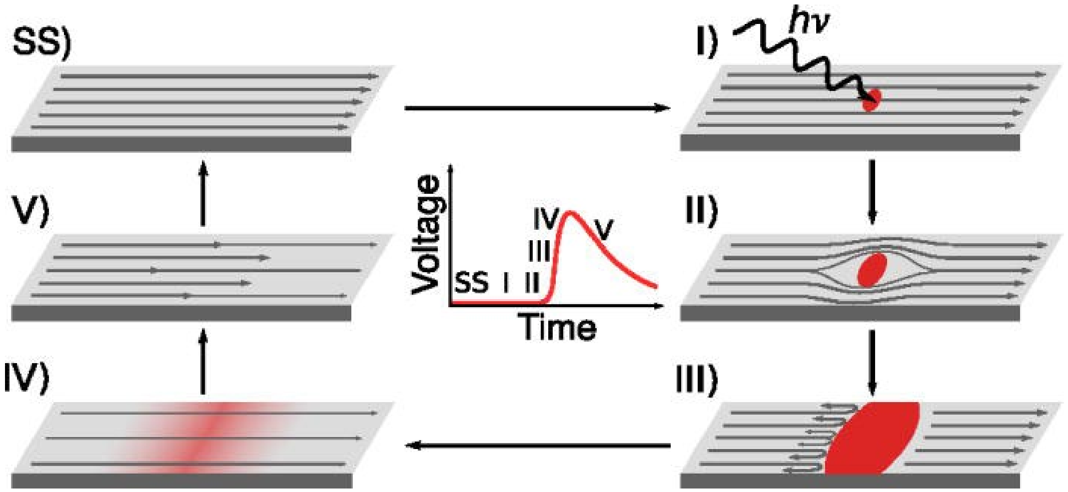
Properties of SNSPDs

- Superconducting-nanowire single-photon detectors (SNSPDs) have many scientific applications, including cosmology and dark matter searches
- They offer unrivaled performance metrics for photon counting, including:
  - Single-photon sensitivity, low drift
  - Broadband response (X-ray to mid-IR)
  - Relatively high-temperature operation (~1K)
    - NbTiN allows operation from 4-7K [1]
  - Very low timing jitter (<3 ps)
  - High quantum efficiency (>98%)
  - Very low dark count rates ($<10^{-3}$/sec)
  - Fast recovery times (<10 ns)
  - Monolithic fabrication on large arrays

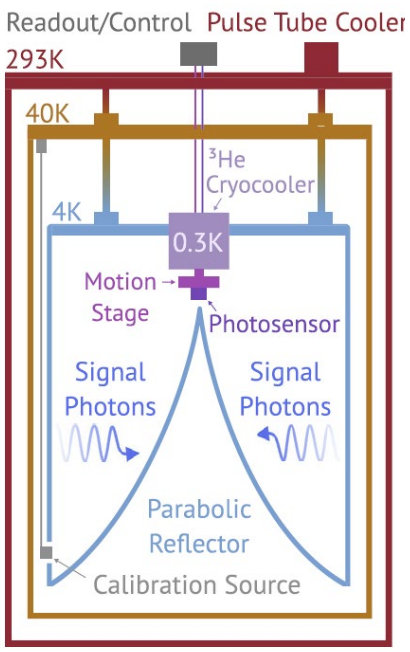


Summary of SNSPD detection mechanism [1]

[1] Esmaeil Zadeh, Iman, et al. "Superconducting nanowire single-photon detectors: A perspective on evolution, state-of-the-art, future developments, and applications." *Applied Physics Letters* 118.19 (2021).

SNSPDs for HEP experiments

- SNSPDs are crucial in searches for bosonic dark matter in the 0.1-10 eV range
  - Low dark count provides sensitivity for studying parameter space not yet excluded by stellar astrophysics models, while also excluding QCD axion models [2]
  - Large-area SNSPDs have been developed by a MIT / NIST / Fermilab team for the BREAD (Broadband Reflector Experiment for Axion Detection) experiment [3]
- SNSPDs also enable infrared astronomy at longer wavelengths, which is critical for cosmology
  - Single-photon counting possible at wavelengths up to 29 μm [4]
- SNSPDs are also promising for improving the sensitivity of tabletop-scale quantum gravity experiments, such as GQuEST
  - Provide photon counting readout for Michelson laser interferometers used to probe for fluctuations in space-time (predicted by "geontropic" models) [5]



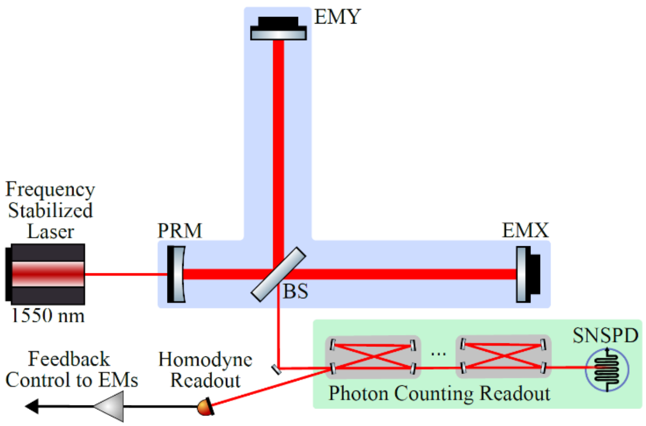
Structure of the BREAD haloscope [3]

[2] Hochberg, Yonit, et al. "Detecting sub-GeV dark matter with superconducting nanowires." *PRL* 123.15 (2019): 151802.

[3] Liu, Jesse, et al. "Broadband solenoidal haloscope for terahertz axion detection." *PRL* 128.13 (2022): 131801.

[4] Taylor, Gregor G., et al. "Low-noise single-photon counting superconducting nanowire detectors at infrared wavelengths up to 29 μm." *Optica* 10.12 (2023): 1672-1678.

[5] Vermeulen, Sander M., et al. "Photon Counting Interferometry to Detect Geontropic Space-Time Fluctuations with GQuEST." *arXiv preprint arXiv:2404.07524* (2024).



Experimental design for GQuEST interferometer [5]

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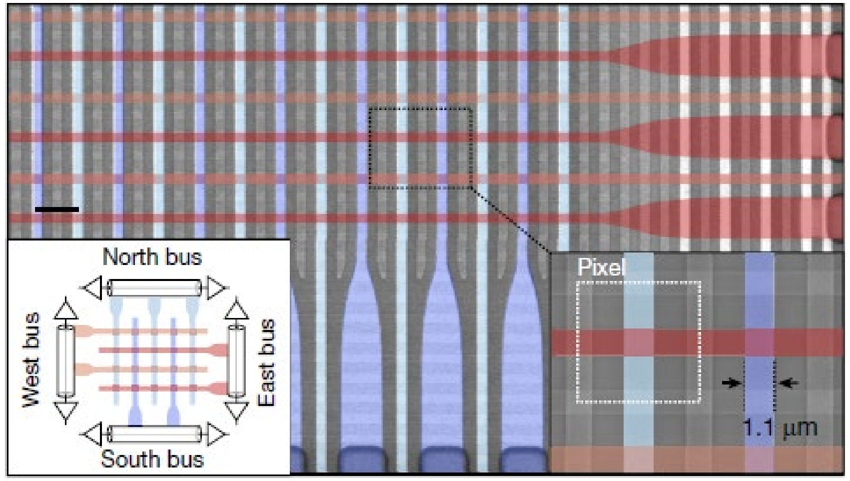
SNSPD readout challenges

- Readout of SNSPD arrays currently relies on room-temperature electronics, which creates a major input/output (I/O) bottleneck
  - Limited number of available feedthroughs for practical cryostats
  - Prevents scaling to larger arrays (into the megapixel range)
- Existing readout techniques:
  - Other superconducting sensors produce continuous-valued outputs suitable for frequency multiplexing, but this is not suitable for SNSPDs due to their broadband pulsed outputs
  - CCD-like serial readout is also not easy to implement
  - Time-of-flight measurement of photon position along detector requires only two readout lines, but results in long reset times and yield issues
  - Row-column architectures detect time-coincident pulses on 2*N* readout lines to detect photon position on *N* x *N* arrays with thermal coupling between rows and columns

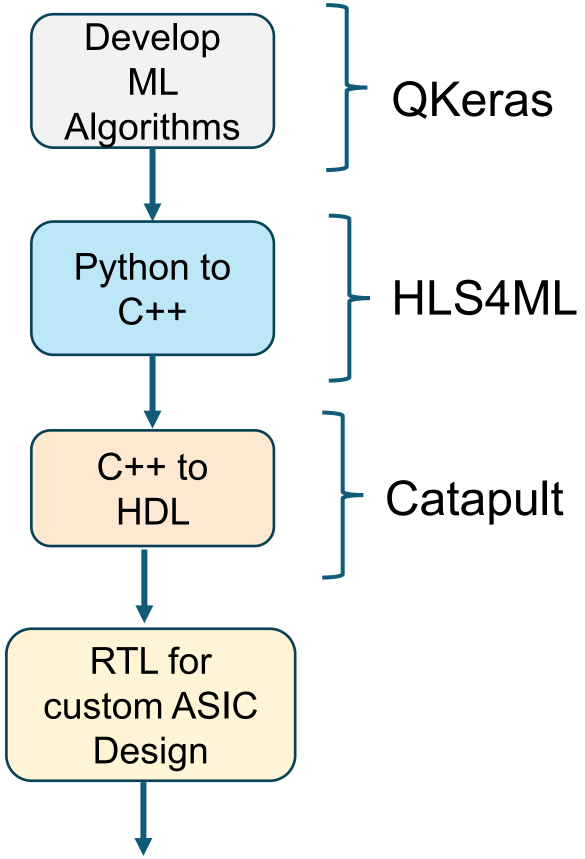


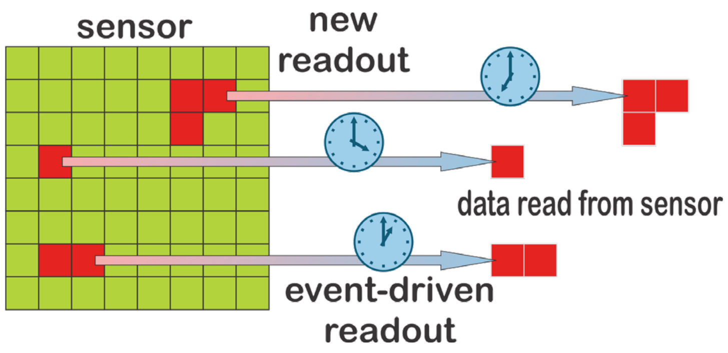
SEM of a 400k-pixel SNSPD array with row-column readout [6]

[6] Oripov, Bakhrom G., et al. "A superconducting nanowire single-photon camera with 400,000 pixels." *Nature* 622.7984 (2023): 730-734.

Proposed readout strategy

- Key concept: Address the I/O bottleneck by using near-detector signal processing to embed artificial intelligence (AI) within the cryogenic chamber.
    - Requires superconducting edge-AI hardware to perform feature selection (multiplexing and coincidence detection), denoising, and classification/regression tasks (photon counting and addressing), thus providing data compression
    - SNSPD outputs are asynchronous pulses, suggesting that they can be efficiently processed by a neuromorphic event-driven processor
    - Accordingly, we propose to implement a superconducting spiking neural network (SNN) to process the neuron-like outputs of SNSPD arrays
    - Builds upon decades of experience within the ASIC group on event-driven readout [7] and edge AI [8] for pixelated detectors





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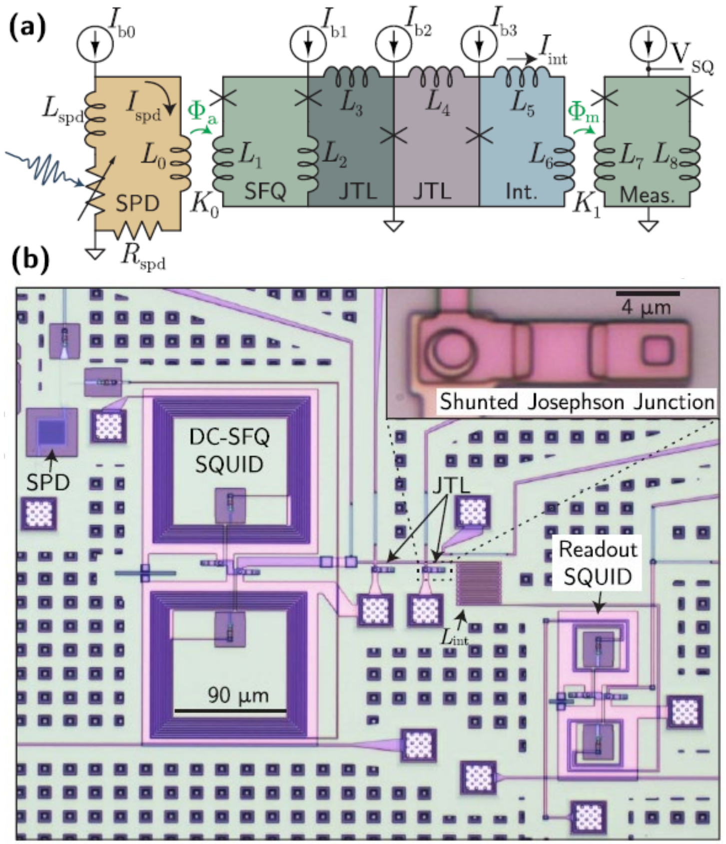
[7] Gorni, D. S., et al. "Event driven readout architecture with non-priority arbitration for radiation detectors." *JINST* 17.04 (2022): C04027.
[8] Miryala, Sandeep, et al. "Design and challenges of edge computing ASICs on front-end electronics." *ISQED*. IEEE, 2022.

Superconducting SNN implementation

- Proposed approach: Use superconducting circuits based on Josephson junctions (JJs) and single-flux quantum (SFQ) logic
  - Information stored as magnetic flux quanta and transferred as quantized voltage pulses
  - Energy-efficient alternative to transistors for computing in cryogenic environments
  - Established technology with well-known circuit design techniques, model libraries, and CAD tools
  - High-speed pulse-based dynamics naturally maps to the asynchronous and event-driven networks needed for implementing SNNs
  - Can be monolithically integrated on the same substrate as the SNSPD array, which greatly improves the energy efficiency of sensor-processor data transfer

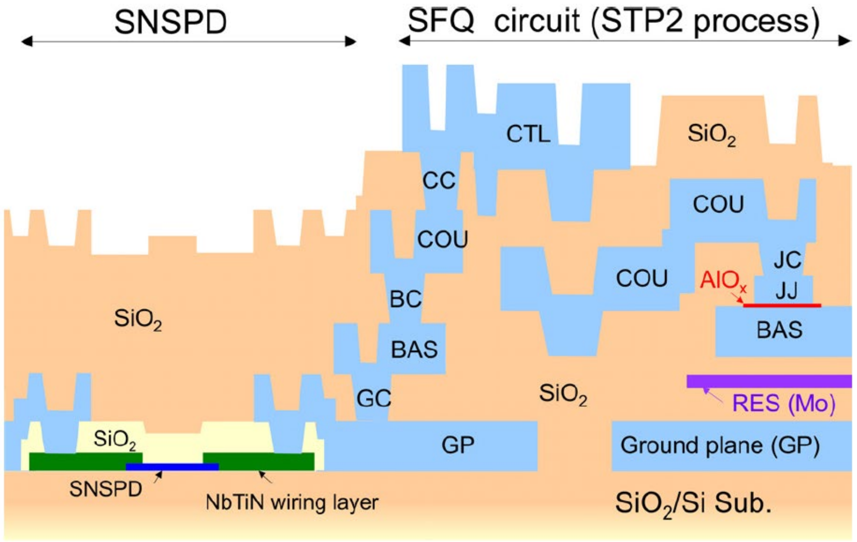


Superconducting single-photon counter [9]

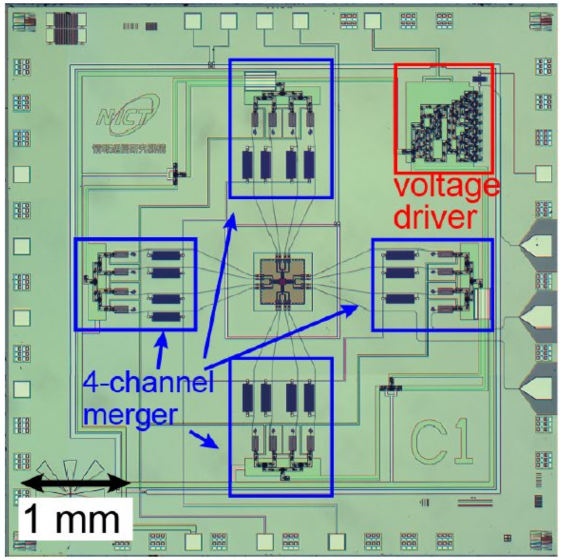
[9] Khan, Saeed, et al. "Monolithic integration of superconducting-nanowire single-photon detectors with Josephson junctions for scalable single-photon sensing." *Superconductor Science and Technology* (2024).

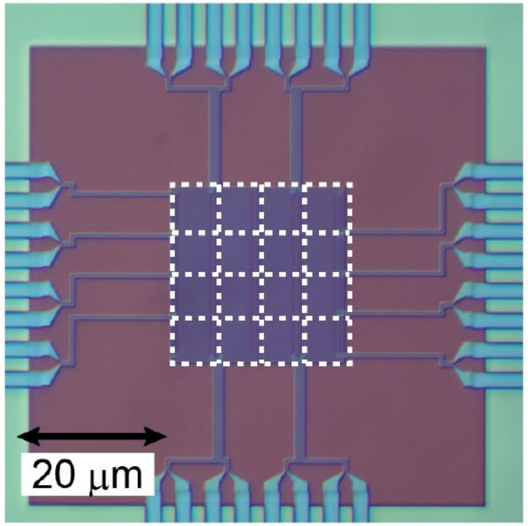
Superconducting SNN implementation (2)

- Monolithic integration of SNSPD arrays with SFQ readout circuits has recently been demonstrated [10]
  - The power dissipation of the SFQ circuit did not result in significant degradation of SNSPD quantum efficiency or timing jitter
  - Sensitivity of the SFQ circuits to magnetic fields can be an issue for some HEP applications



Process cross-section





Die photograph of a prototype chip containing a 4 x 4 SNSPD array and an SFQ multiplexer circuit [10]

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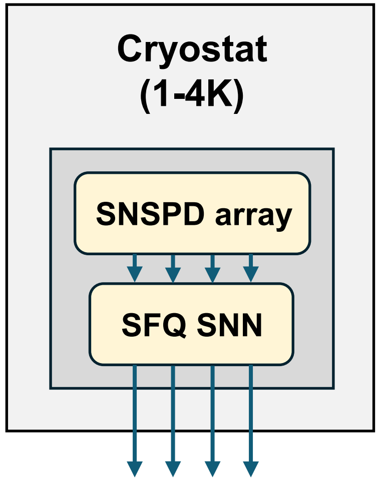
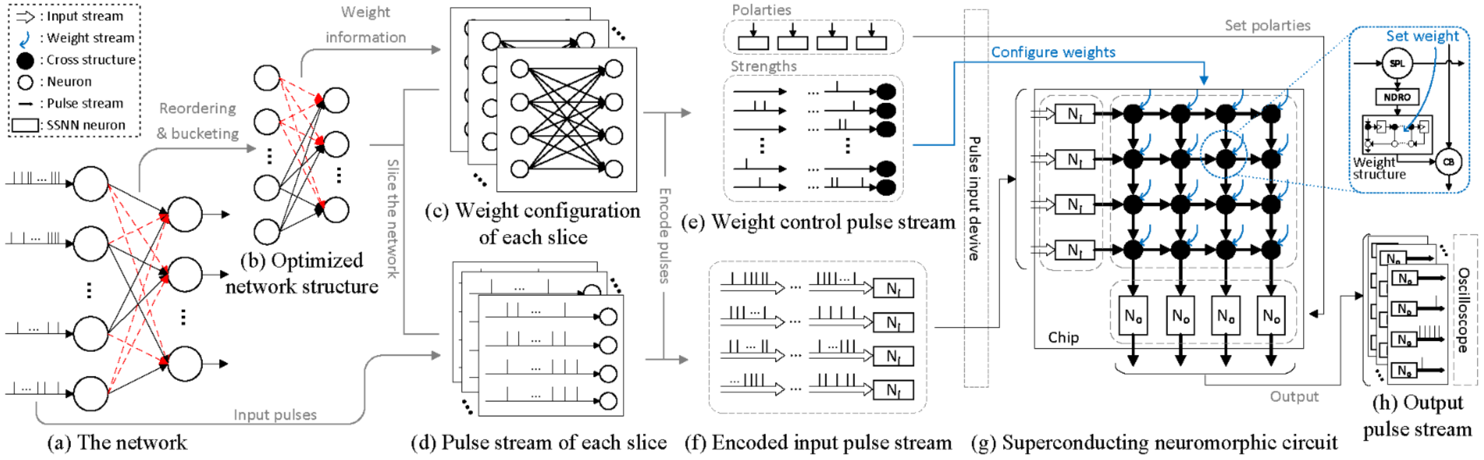
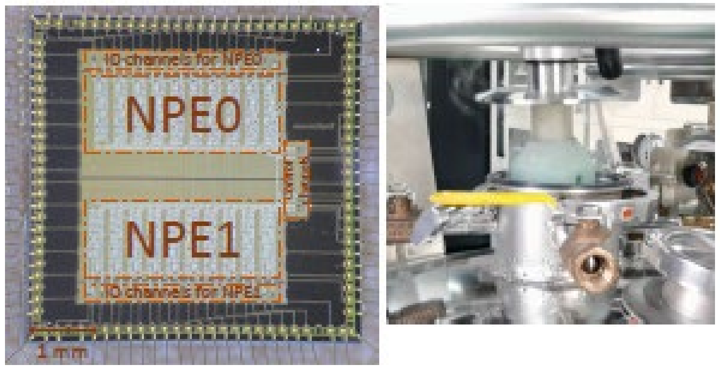
[10] Miyajima, Shigeyuki, et al. "Single-flux-quantum signal processors monolithically integrated with a superconducting nanostrip single-photon detector array." *Applied Physics Letters* 122.18 (2023).

Superconducting SNN implementation (3)

- Recent years have witnessed a rapid growth in interest in SFQ-based SNNs
- For example, a recent SFQ-based single chip SNN containing ~10^5 JJs achieved an experimental energy efficiency of 32.4 TSOPS/W [11]
  - About 100x better than state-of-the-art neuromorphic processors in CMOS technology
  - Requires efficient mapping of states to transitions to minimize on-chip memory
- The proposed project will build upon such earlier work to develop the world's first monolithically-integrated smart SNSPD array with on-chip SNN readout
  - Key enabling technology for large-scale (Mpixel-size) SNSPD arrays
  - High potential for follow-on funding







Neuromorphic workflow for SFQ-based SNN (left), chip and test setup (top) [11]

[11] Liu, Zeshi, et al. "SUSHI: Ultra-High-Speed and Ultra-Low-Power Neuromorphic Chip Using Superconducting Single-Flux-Quantum Circuits." *Proceedings of the 56th Annual IEEE/ACM International Symposium on Microarchitecture*. 2023.

Project team and budget

- BNL (IO): Soumyajit Mandal (PI), Gabriella Carini, Grzegorz Deptuch, Piotr Maj, Prashansa Mukim
  - Main roles: SFQ processor development, system integration and testing
- BNL (CSI): Shinjae Yoo
  - Main roles: SNN architecture development, hardware-software co-optimization
- NIST: Joel Ullom
  - Main roles: SNSPD design and optimization
- NY CREATES: Satyavolu Papa Rao
  - Main roles: SNSPD and SFQ array fabrication
- Florida International University* (FIU): Arjuna Madanayake
  - Main roles: Signal processing, simulation tool development

*Minority-serving institution (MSI)

	Year 1	Year 2	Year 3
BNL	$750k	$750k	$750k
NIST	$250k	$250k	$250k
NY CREATES	$300k	$300k	$300k
FIU	$200k	$200k	$200k
Total	**$1.5M**	**$1.5M**	**$1.5M**

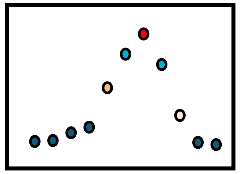
Key milestones

- Year 1: System modeling, SNSPD and SNN design
- Year 2: Fabrication of SNSPD and SNN prototypes
- Year 3: Fabrication and testing of monolithic smart detector (SNSPD + SNN)

Also looking for collaboration with the physics department

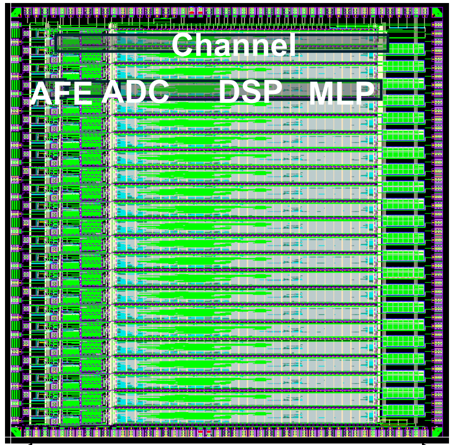
Relevant experience and facilities

- Investigating extraction of features from sampled pulse waveforms (waveform snippets) using edge AI within the front-end ASIC

Charge sensor → Front-End (Amplifier + Shaper + ADC) →  → Neural Network

Digital Signal Processing

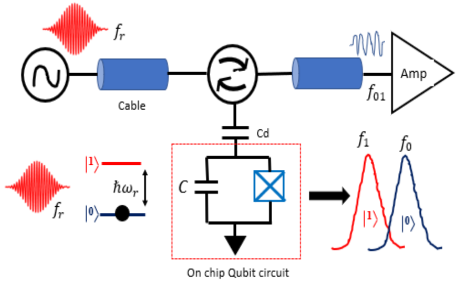
- Collaboration between IO and CSI (part of earlier LDRD-A)

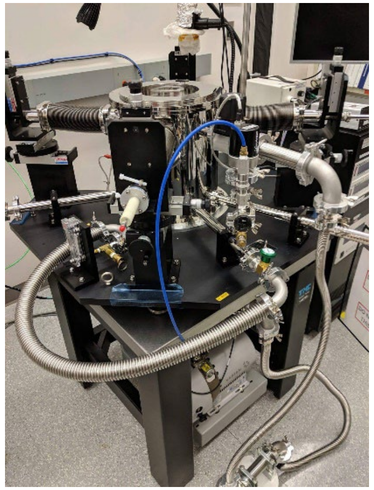


5 mm

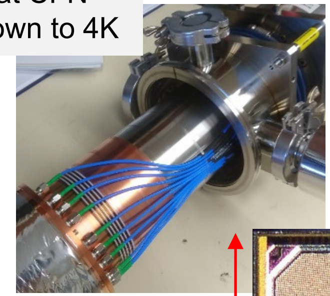
Smart multi-channel front-end ASIC with on-chip ANN [12]

[12] S. Mandal et al., “A Smart Readout ASIC with Real-Time Digital Waveform Processing and Machine Learning”, submitted to *IEEE NSS*, 2024.





RF readout of qubits or quantum sensors / probe station at CFN cryostat at IO operating down to 4K



Layout of 4K RF tests structures CryoCMOS
With 5.12 GHz center frequency VCO and QVCO for PLL with CML divider and interfaces
QRFIC_P1

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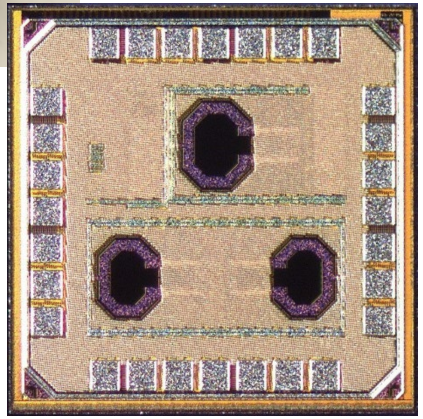

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- Studying use of cryogenic CMOS circuits (operating at 4K) for QIS applications [13]

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[13] V. Manthena et al, “A 1.2-V 6-GHz Dual-Path Charge-Pump PLL Frequency Synthesizer for Quantum Control and Readout in CMOS 65-nm Process”, *2020 11th IEEE Annual Ubiquitous Computing, Electronics & Mobile Communication Conference (UEMCON)*, 2020, pp. 0570-0576