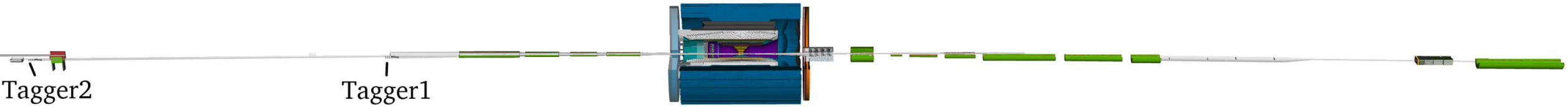
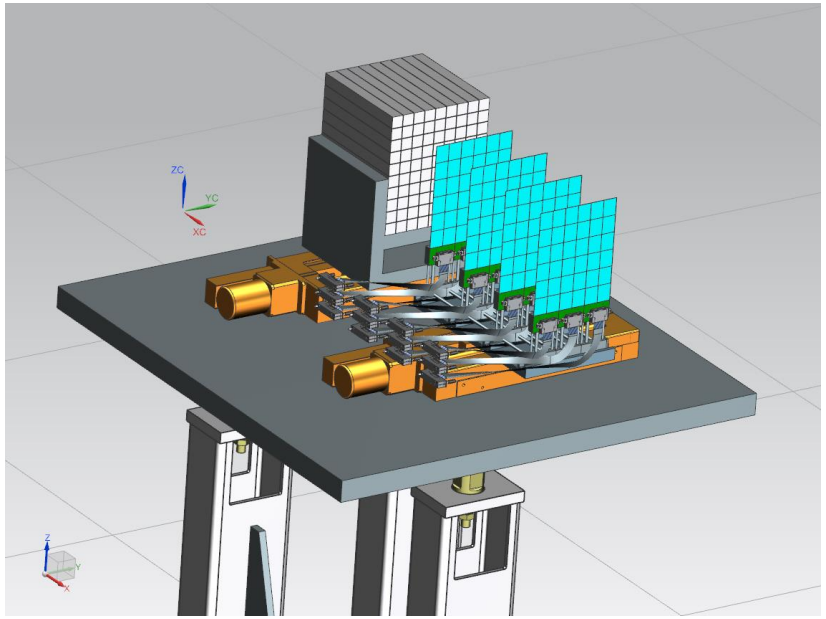
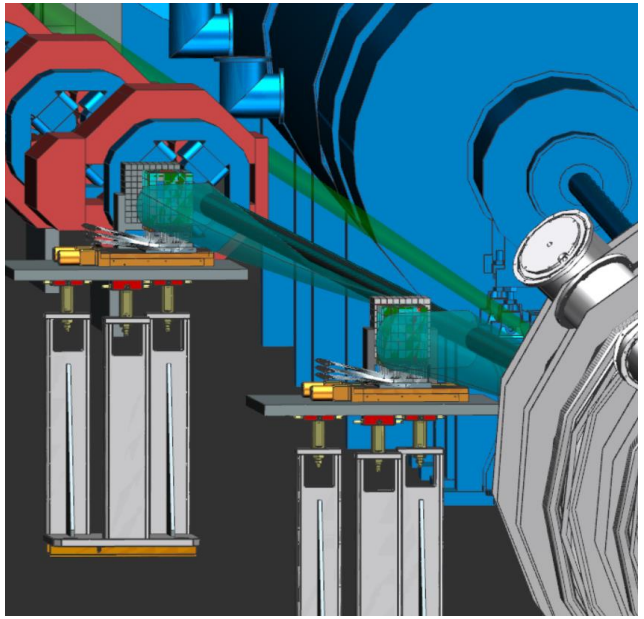
TimePix4 for the Low-Q^2 Tagger Tracker



Simon Gardner

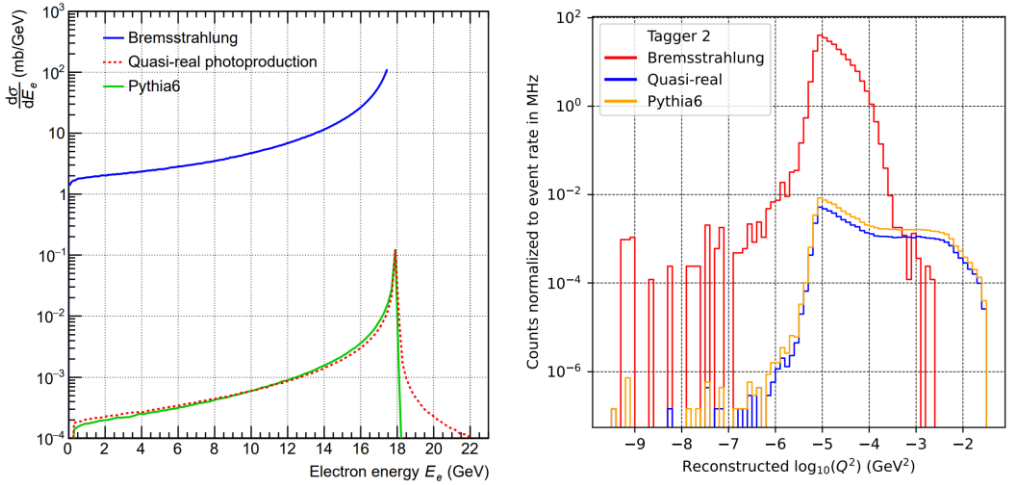
ePIC TIC meeting
24th June 2024



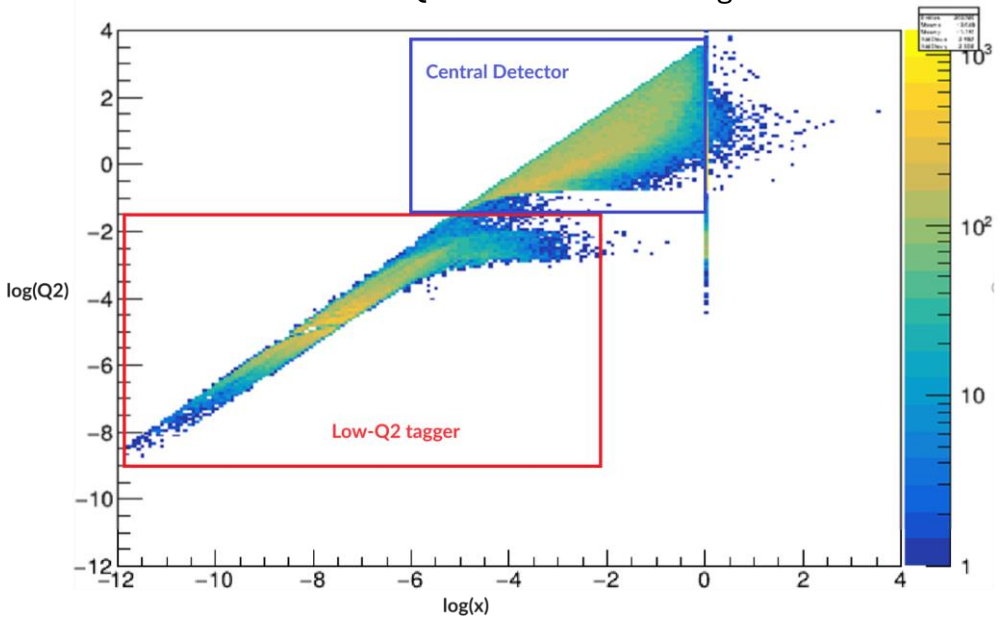


Low-Q^2 Tagger - Requirements

- Extend the acceptance of the experiment, $Q^2 \rightarrow 0$ GeV
  - Covering quasi-real photoproduction processes
- Backgrounds
  - Below $Q^2 \approx 0.0005$ GeV, scattering angle smaller than beam divergence.
    - Bremsstrahlung cross section dominates.
    - Electron kinematics alone cannot be used to identify DIS electron.
    - Need to handle statistically with exclusivity variables and background only samples.
  - Synchrotron background hits in single layer – no track
  - Electron beam gas originates at non-IP vertices – track usually will be distinguishable.
- Rates - At highest luminosity e-p conditions
  - O(20) IP Bremsstrahlung per 10 ns bunch crossing, ~12 in tagger acceptance.
  - Electrons beam gas interactions (Bremsstrahlung also) acceptance with around the same frequency as photoproduction.
  - Synchrotron radiation backgrounds concerning but possible mitigation approaches under investigation by Andrii.



Relative cross section of QR and Bremsstrahlung interactions



x-Q^2 acceptance of Low-Q^2 and central detectors

Low-Q^2 Tagger – Bremsstrahlung Rates

- Bremsstrahlung rates highest concern while Synchrotron being investigated.
  - Highest rates greater than 10 kHz per pixel in current geometry
  - Will be significantly larger in high luminosity ion collisions.
  - Detector planes to be able to move around to match with beam conditions

Total maximum Brem data rates

(Need updating – Divide by about 17)

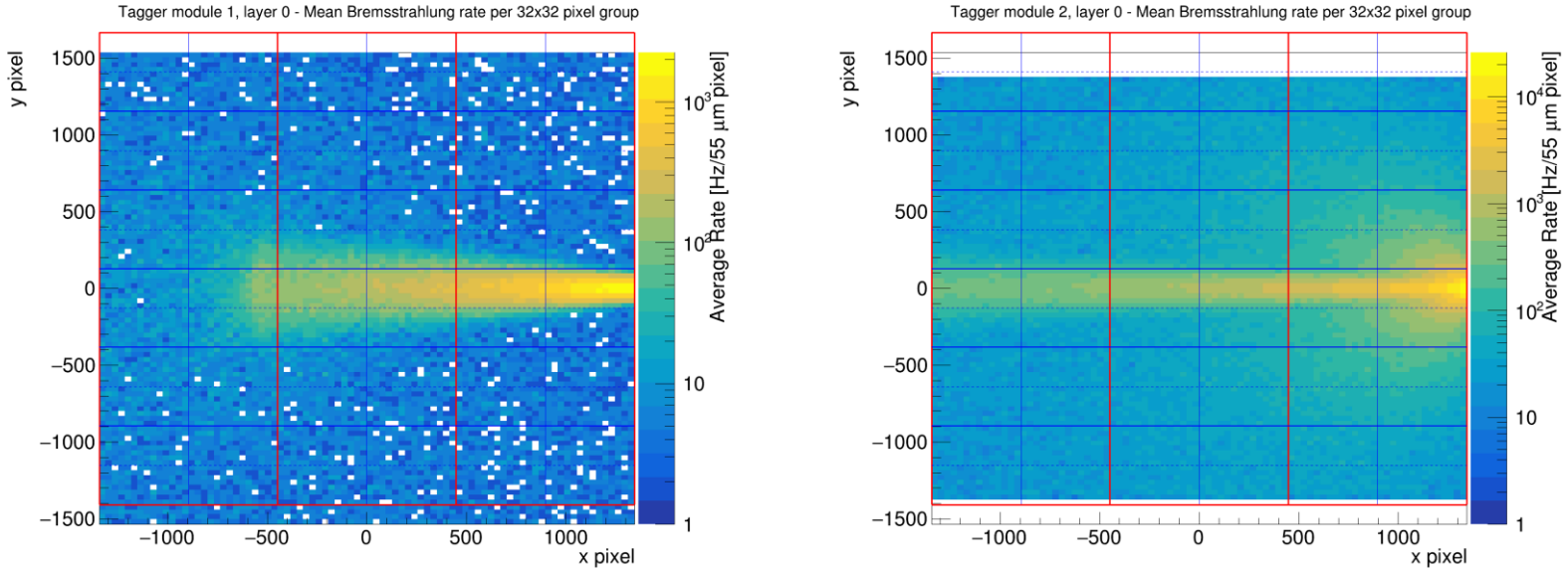
Maximum rates

Pixel (P1)	70 kHz	
2 column (C1)	8 MHz	
Tpix4 (T1)	600 MHz	38 Gb/s
Board (B1)	1500 MHz	96 Gb/s
Layer (L1)	2500 MHz	160 Gb/s

Total integrated rates

Tagger 1	2 GHz	130 Gb/s
Tagger 2	7 GHz	480 Gb/s
Total	**9 GHz**	**600 Gb/s**

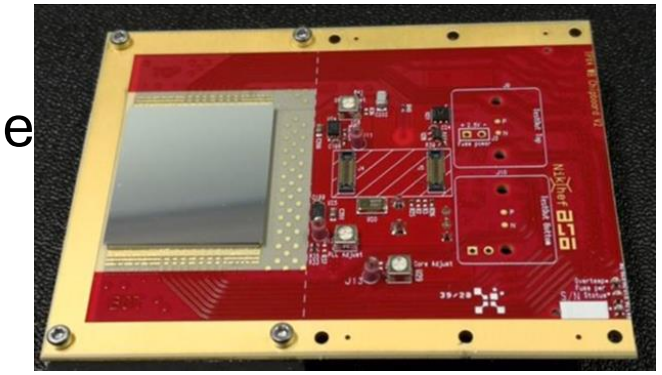
Data buffered & filtered: need a hadron in main detector
Trigger rate: 500 kHz: 99.4% rejection (brem only)
Data rate (signal): 4 Gb/s
Data rate (incl BG and rand sample) **<20 Gb/s** To tape



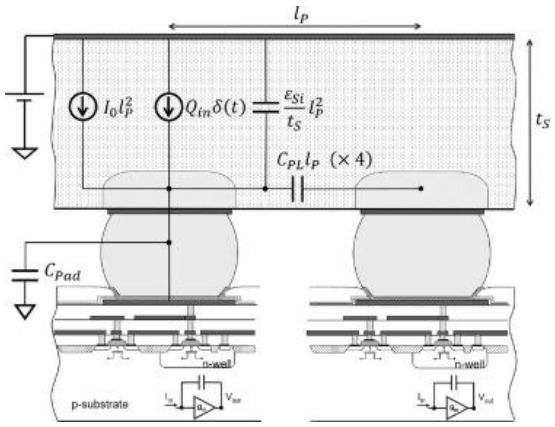
Hit rates in the first layer of both Low-Q2 tagger modules – needs updating

Timepix4 - Technology

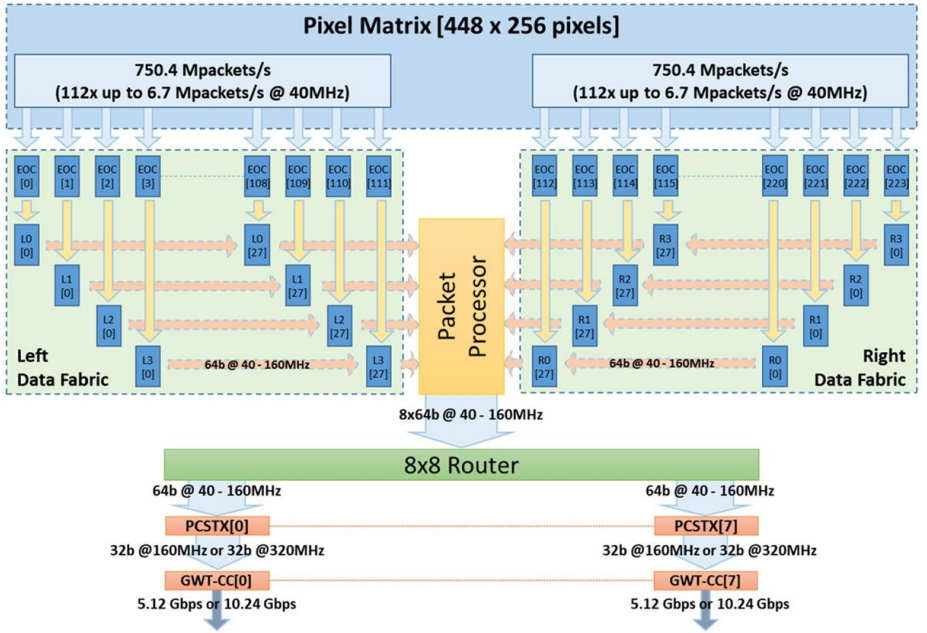
- Timepix4 is the most recent ASIC from the CERN based Medipix collaboration.
- Hybrid pixel detector
  - Sensor separate from the electronics
  - Can select sensor based on requirements
- 448x512 array of 55µm square pixels
  - 6.94 cm^2 sensitive area
  - Data driven readout – Only reads out pixels which register a hit
  - 4 side buttable using TSV technologies – Read out through bottom of chip rather than wire bonds allowing tiled layer of detectors.
- 200 ps - Time of arrival clock binning
- 25 ns - Time over threshold clock binning (energy measurement)
- Up to 16, 10.23 Gbps readout lines
  - 64-bit event packet.
  - 10.8 kHz maximum (average) rate per pixel.
  - Absolute maximum single pixel rate limited by 25 ns clock



Timepix4 wire bonded to Nikhef carrier board



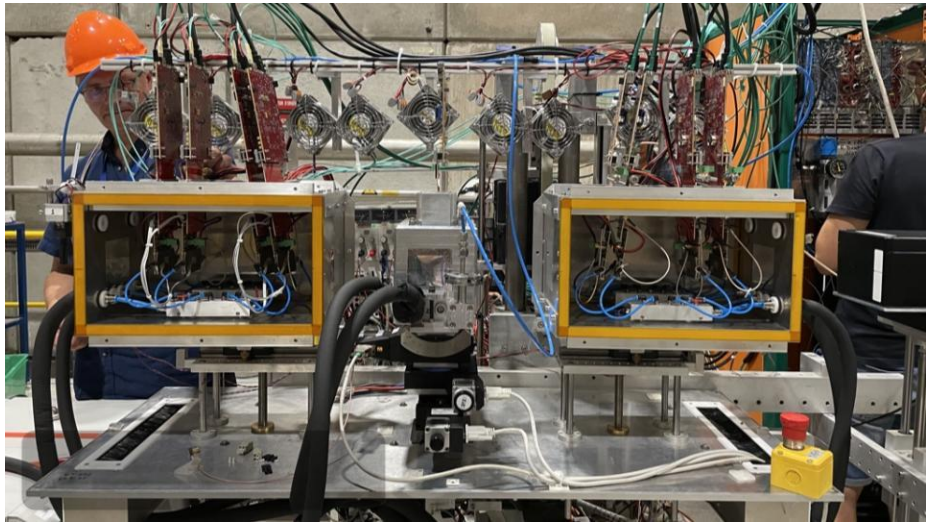
Hybrid pixel detector schematic. From: The Timepix4 analog front-end design: Lessons learnt on fundamental limits to noise and time resolution in highly segmented hybrid pixel detectors - ScienceDirect

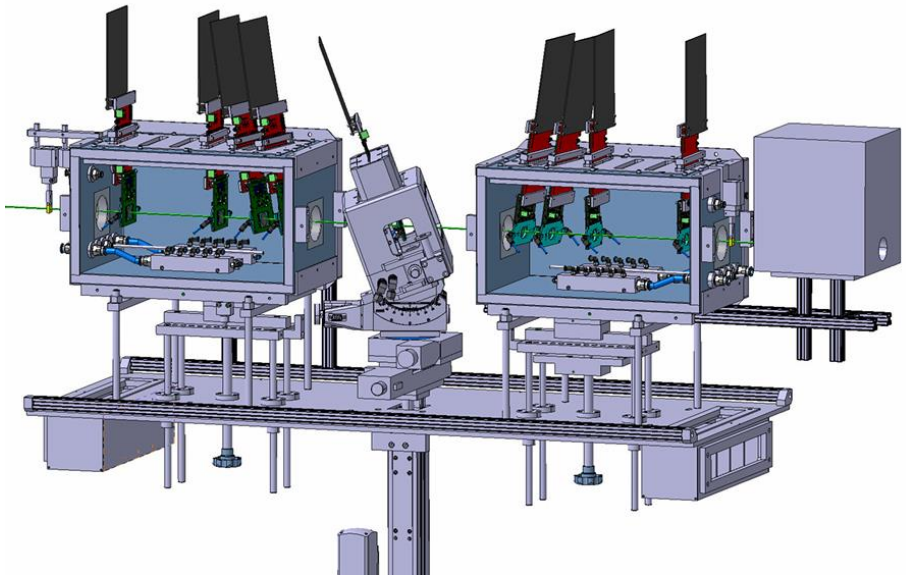


Readout path for periphery on one side. From: Timepix4, a large area pixel detector readout chip which can be tiled on 4 sides providing sub-200 ps timestamp binning - IOPscience

Timepix4 - Technology

- Only mature technology capable of meeting requirements
- Large community testing ASIC and developing tools
  - Multiple iterations of ASIC already fixed issues.
- Timepix4/SPIDR4 telescope deployed at SPS-CERN
- Early studies with setup in Glasgow
  - Tests planned in Europe this summer using SPIDR4
  - Tests planned at Jlab with prototype EIC DAQ early 2025
  - Decision between SPIDR4/simpler EIC readout boards
- TSV processed chips being tested





SPS Timepix4 telescope photo and CAD. From: TDCPix test (26 April 2023) · Indico (cern.ch)

Test setup in Glasgow

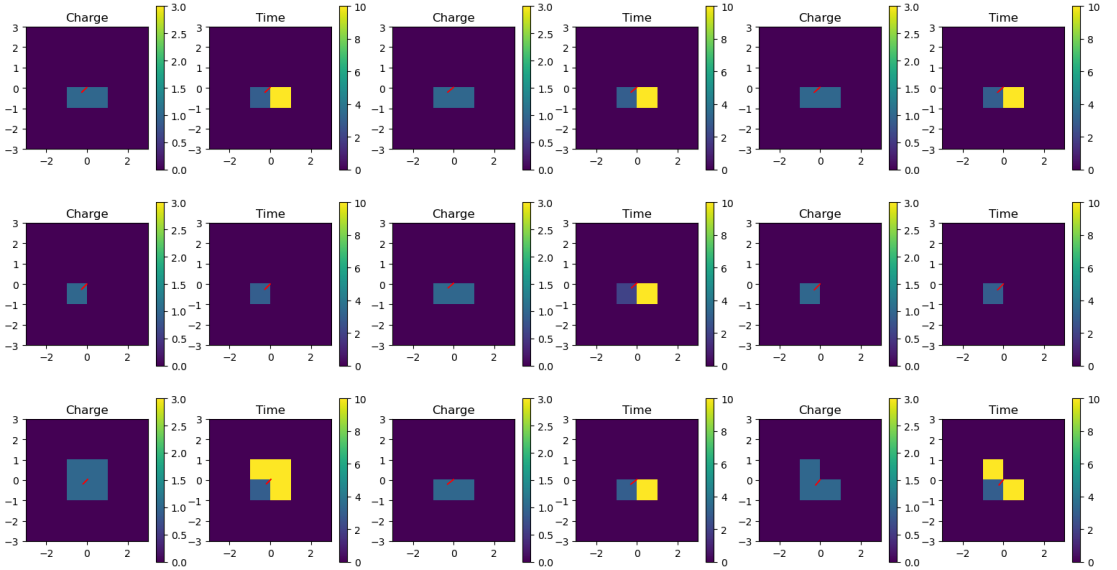
Technical Challenges

- The highest rates are at the limit of the ASICs design capabilities
  - Need an accurate model of the background environment.
  - Need realistic digitization, modelling detector response e.g. charge sharing and time over threshold.
- Huge amount of data being read out
  - Reduce this as early as possible to relieve stress on the DAQ.
  - FPGA/hardware cluster and track based background removal
    - Graph Neural Networks for constant latency.
  - Bunch crossing matching to an “event” in the central detector
- Timepix4 while mature is highly configurable so need to understand how to get the most out of it for our application.

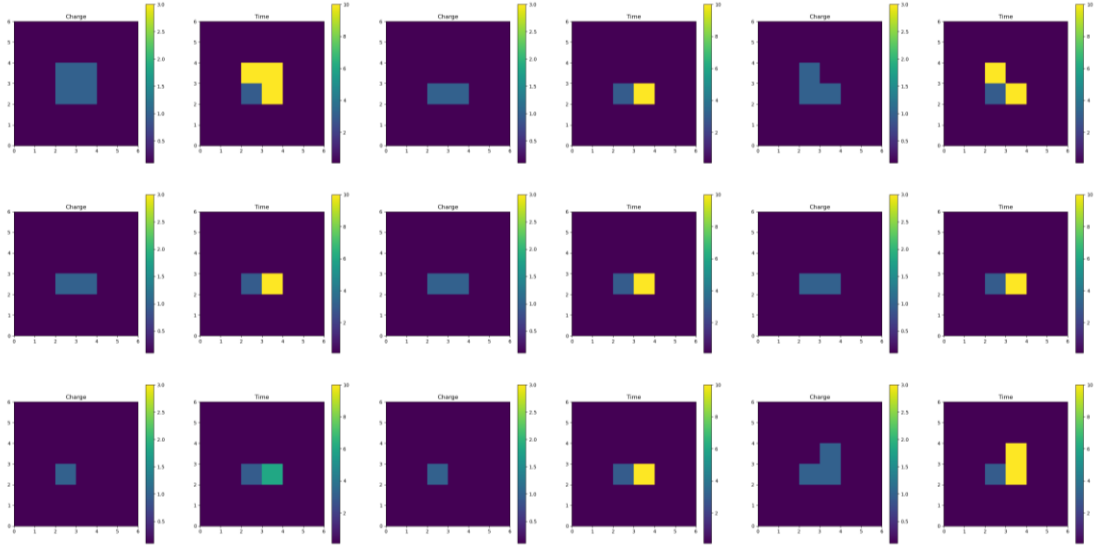
Digitization with fast simulation

- Allpix2 framework model used to generate realistic events
  - 10M events ~ 8 hours = 350 Hz
  - Not using the most realistic available detector modules
  - Outputs 6x6 grid of ToA and ToT values.
  - Has significant user base, frequent meetings and many demonstrations using timepix/maps/other silicon detectors
- Conditional Variational Autoencoder trained to reproduce distribution of events
  - 10M events ~ 70 seconds = 150 kHz
  - Model not yet optimized
  - Saved as onnx so would be simple to add to eicrecon.
- Realistic events will be essential to better understand rates and reconstruction limits

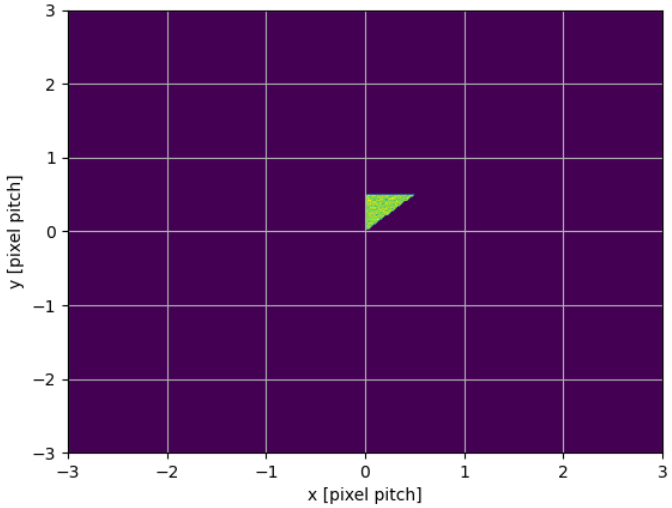
x=0.0, y=0.0, px=-0.05, py=-0.05



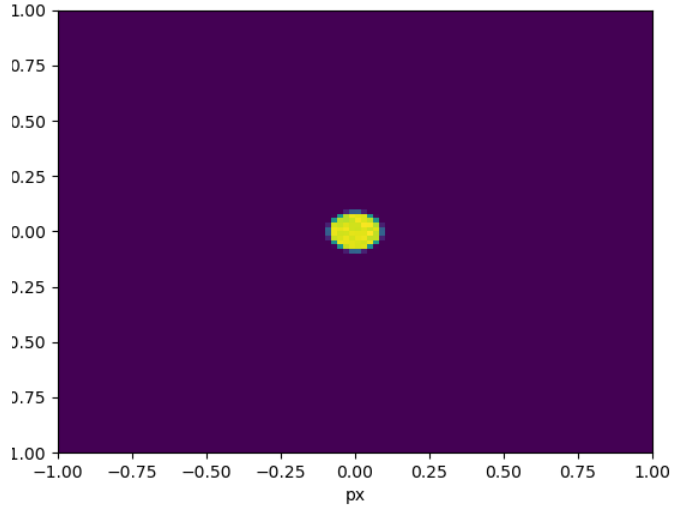
Example simulated events



Example generated events

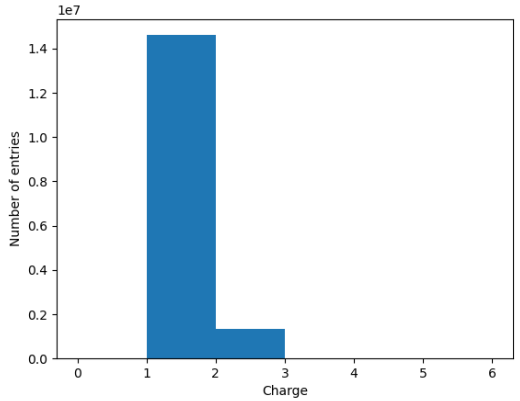


x/y position distribution of generated events

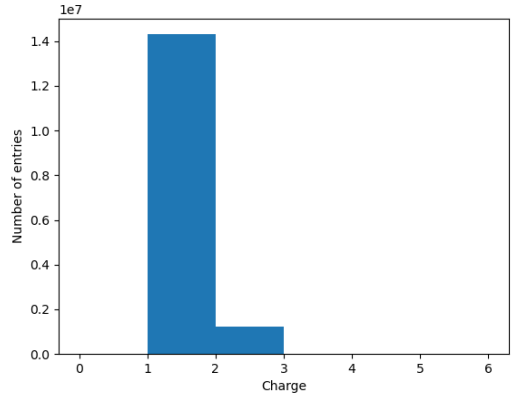


x/y direction component of generated events

Digitization with fast simulation



Charge (ToT 25ns) simulated values



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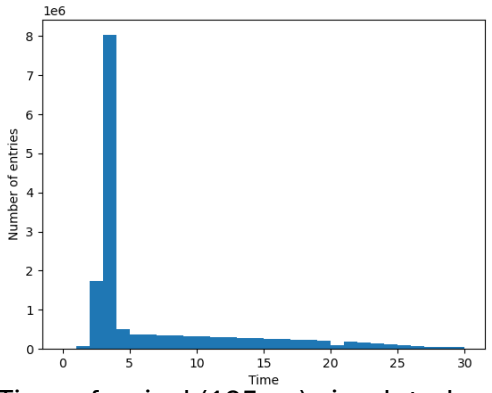
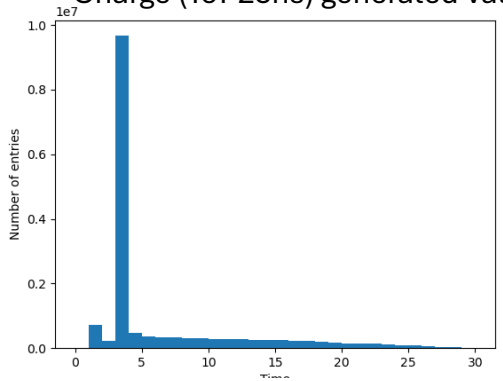
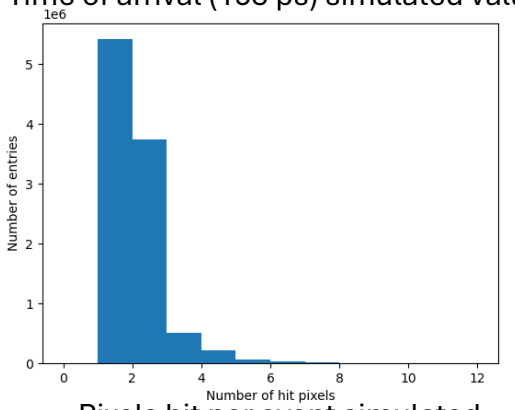


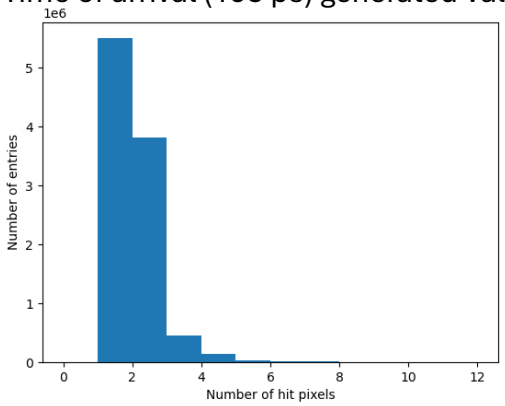
Time of arrival (195 ps) simulated values



Time of arrival (195 ps) generated values



Pixels hit per event simulated



Pixels hit per event - generated

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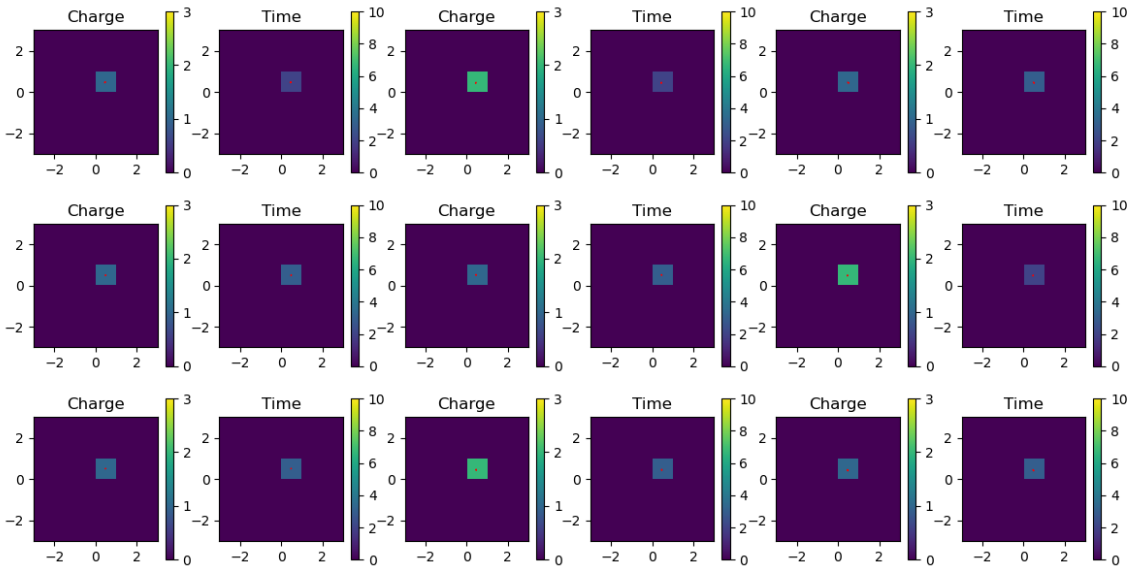
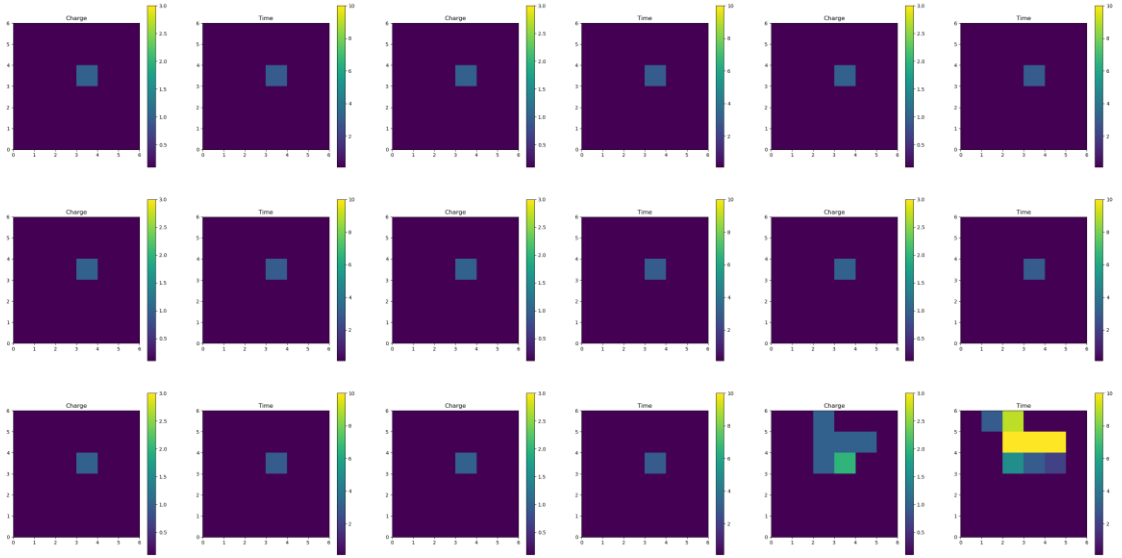


Example simulated events



Example generated events

Non-Timepix related challenges

- Integration with the accelerator/beampipe remains challenging
  - Studies into balancing impedance/synchrotron backgrounds and detector acceptance/resolutions underway.
  - Latest updates - Low-Q2 Tagger weekly meeting (18 June 2024) · Indico (bnl.gov)

End