Los Alamos NATIONAL LABORATORY

ePIC SVT WP3
Updates on Q-Flex evaluation

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General introduction

- We are waiting for the final paperwork approval to receive funding for the eRD113 work
- Joellen bio and introduction
  - Electrical Engineer at LANL
  - Expertise in FPGA firmware development with some experience in PCB design
  - Worked on designs for space, sub-orbital flights, and ground testing applications
- Layout of the work plan
  - Contribute to the FPC evaluation and characterization
  - Contribute to the ancillary chip development and readout integration

Results so far on reaching out to Q-Flex

- Started conversation with electrical engineer at Q-Flex to check the possibility of manufacturing OB Bridge FPC type A prototype provided by STFC UKRI
- Initial constraints stated by Q-Flex:
  - Can create 2-layer Aluminum flex circuits
  - Can not electroplate vias or have PTHs for Aluminum designs
- Engineer wants a condensed CAD model with CAD layers only corresponding to stack up layers (i.e., 4 layers)
  - Simpler model can either be provided by UK or created by LANL by merging and deleting layers in UK provided CAD model
- After simpler model is provided, Q-Flex will provide feedback on stack up
  - Potentially will propose a revised stack up