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FPC prototype V1 testing

Test plan for testing signal integrity of connections via the prototype FPC

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Signal Types

There are 3 type of connection to test

- Low speed clock and data from LHS to AncASIC via bridge
  - 80 Mb/s
  - Multi drop
  - Alternatively accessible on RHS test card
- Low speed read data from AncASIC to LHS.
  - 160 Mb/s
  - Multi drop
  - Alternatively accessible on RHS test card
- High Speed data from AncASCI (or sensor) via bridge to LHS
  - Point to point
  - 5 Gbits/s or 10 Gbits/s

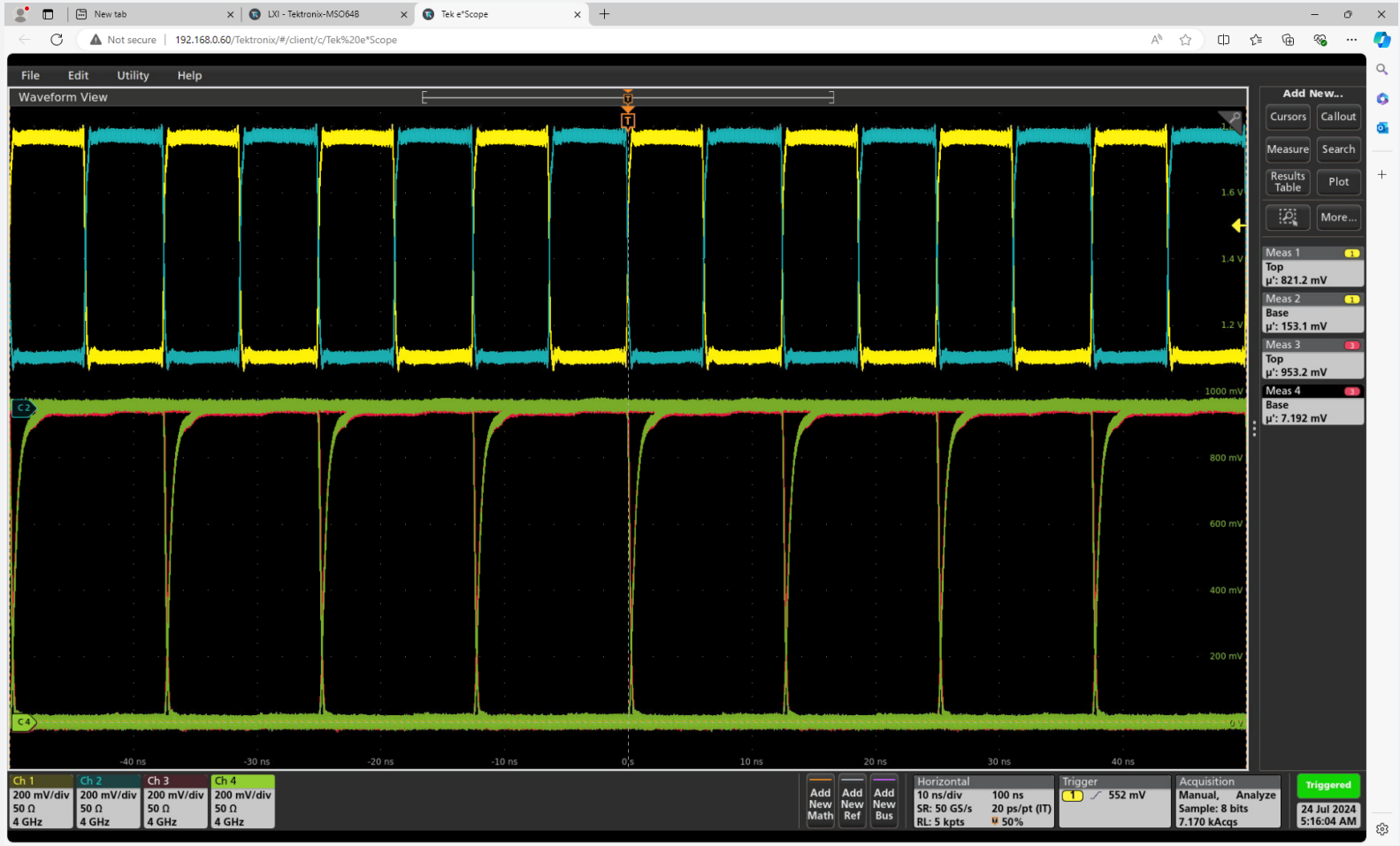
Low speed signals

The Xilinx iBert tool and MGT can only be used at > 1 Gbits/s
Hence using custom VHDL PRBS via conventional SelectIO pins
Two user pairs available via SMA connectors.

Signal	Pad	Bank	VCC	Comments
USER_SMA_GPIO_P	H27	65 (HR)	VCC1V8_FPGA	Fixed 1V8
USER_SMA_GPIO_N	G27	65 (HR)	VCC1V8_FPGA	
USER_SMA_CLOCK_P	D23	67 (HP)	VADJ_1V8_FPGA	External 100Ω termination
USER_SMA_CLOCK_N	C23	67 (HP)	VADJ_1V8_FPGA	

Chose DIFF_SSTL18_I (minimum 8mA drive)
Higher drive voltage than lpGBT, so scale results accordingly.
Does not allow provision of pre-emphasis.

Cabling directly to ‘scope



Clock 80 MHz
Data 80 MBits./s
Coupling: DC
Termination: 50 Ω

Note DC 50 Ω path to GND is not correct for SSTL18, hence top and base lower than normal.
With test fixture this will be AC coupled.
Note faster rising edge on clock (HP bank)
Note lower amplitude on Clock due to additional 100Ω

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User control

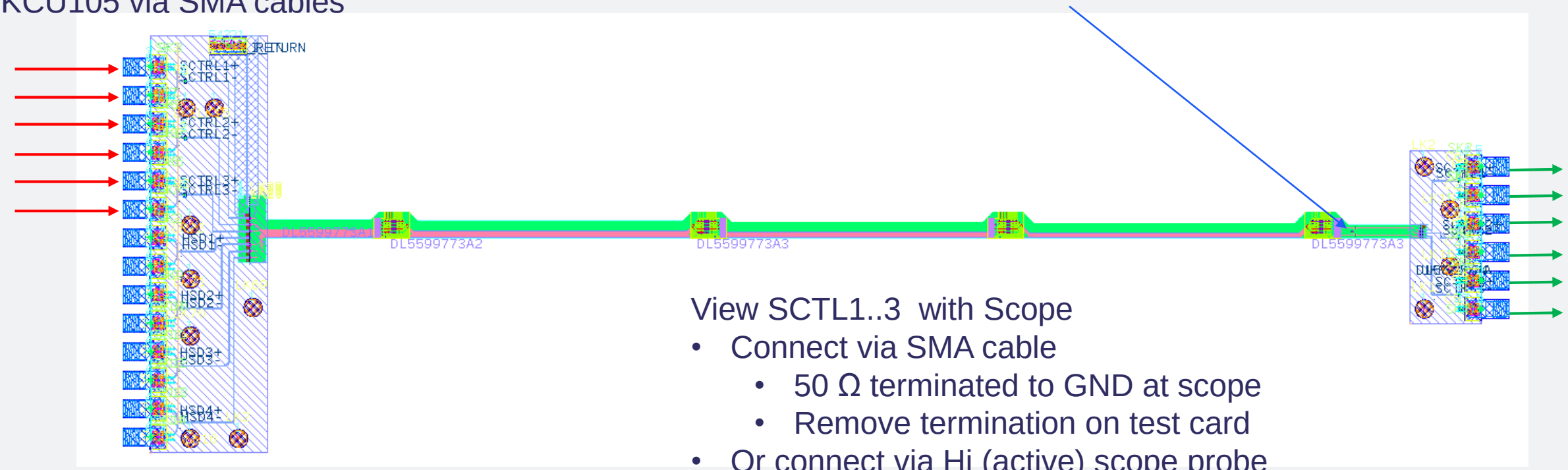
A microblaze program allows control via USB-UART

Command	Function	
0x50 0	PBRS length 7 bits	
0x50 1	PBRS length 9 bits	
0x50 2	PBRS length 15 bits	
0x50 3	PBRS length 23 bits	
0x51 0	Clk = Clk gpio=data	
0x51 1	Clk = data gpio=Clk	
0x52 0	80 MHz	
0x52 1	160 MHz	
0x52 2	320 MHz	

Main FPC only, slow control

Inject Data or Clock and data into SCTL1…3 from KCU105 via SMA cables

Remove termination from Main FPC



View SCTL1..3 with Scope

- Connect via SMA cable
  - 50 Ω terminated to GND at scope
  - Remove termination on test card
- Or connect via Hi (active) scope probe
  - With termination on test card.
- Also consider test in reverse direction.
- Additionally test these lines at > 1 Gbits/s using iBert bitstreams and MGT.

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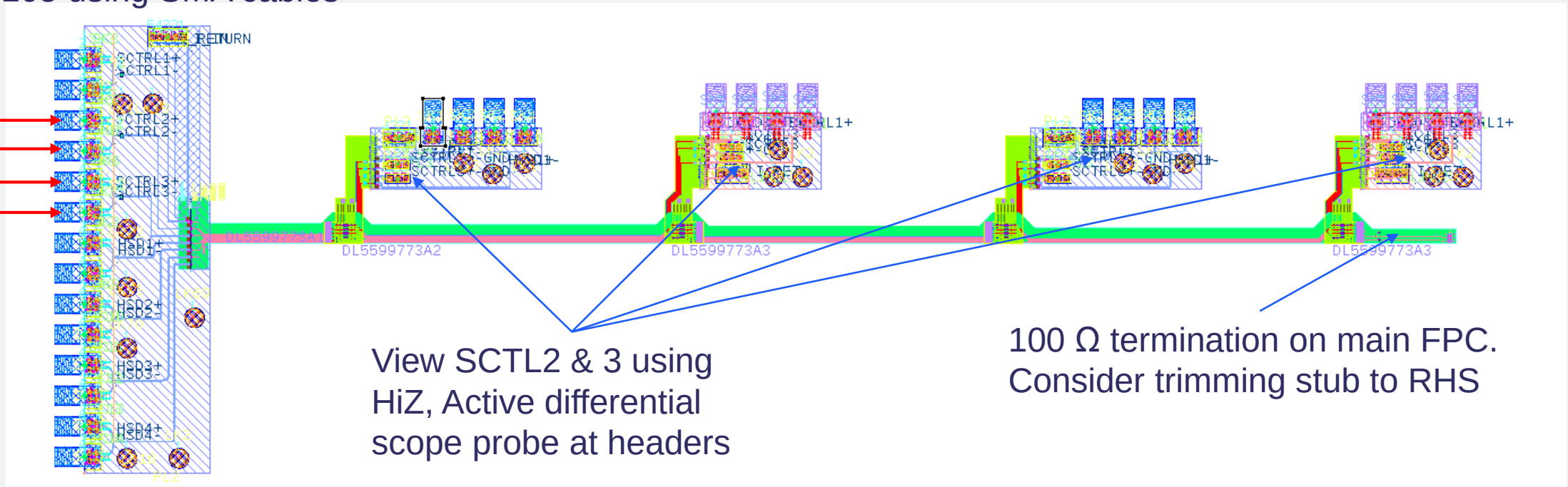
Slow Control Clock and TX data SCTL2 & 3

Inject Data or Clock and data into SCTL2…3 from KCU105 using SMA cables



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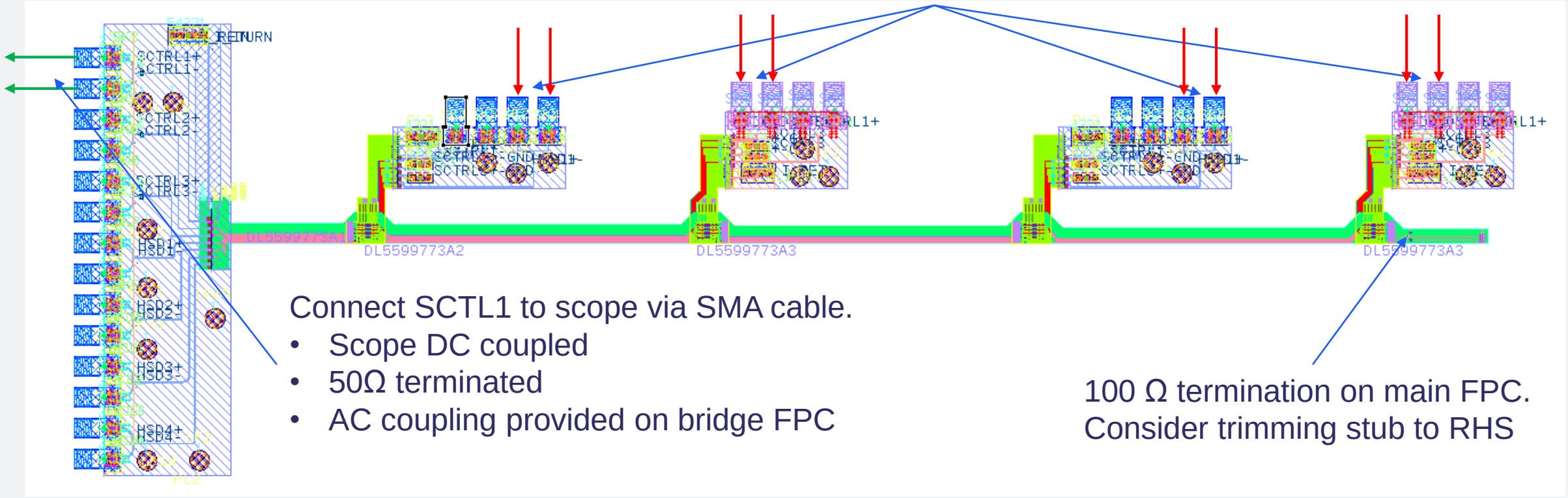
Slow Control RX data SCTL1

Inject Data into SCTL1 from KCU105 via SMA cable.



Connect SCTL1 to scope via SMA cable.

- Scope DC coupled
- 50Ω terminated
- AC coupling provided on bridge FPC

100 Ω termination on main FPC.
Consider trimming stub to RHS

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Viewing and measuring slow control signals

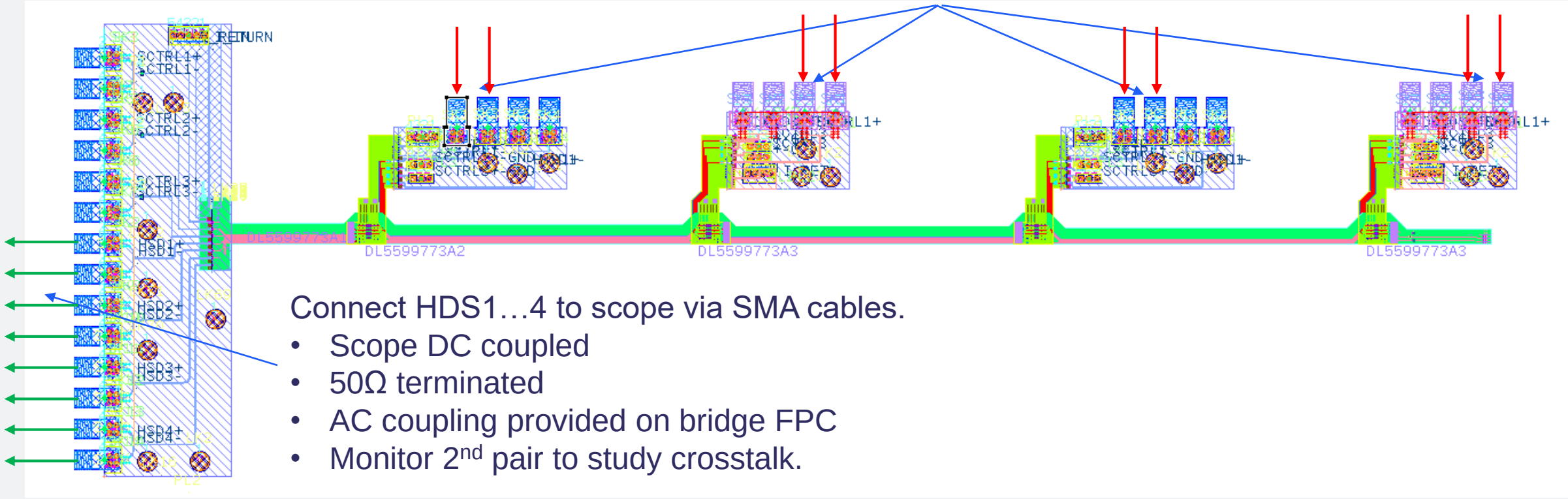
- Trigger ‘scope off the clock
  - Persistence view will create an eye diagram
  - Compare supplying clock via FPC and directly to scope
  - Consider scope with eye diagram tool and clock recovery or cleaning.
- Test swapping USER_SMA_CLOCK_P and USER_SMA_GPIO_P to see effect of 100 Ω source termination

High speed signals

- Xilinx iBert test designs have been built for 1, 2 … 10 Gbits/s
- Create Link from Quad_226 MGT_X0Y11 to itself.
- Choose PRBS7, 9 .. Fast clock or Slow clock patterns
- View data with scope.
  - Fast/slow clock can be measured with standard scope measurements.
  - PRBS patterns need scope with Eye diagram tool with Clock Data Recovery.
- View data using KCU105 iBert tool.
  - Disable equaliser to get measure of raw signal.
  - Perform 1-d bathtub or 2-d full eye diagram scans.
- Consider exploring pre-cursor and post-cursor.

High speed signals

Inject Data into HSD1..4 from KCU105 via SMA cables.



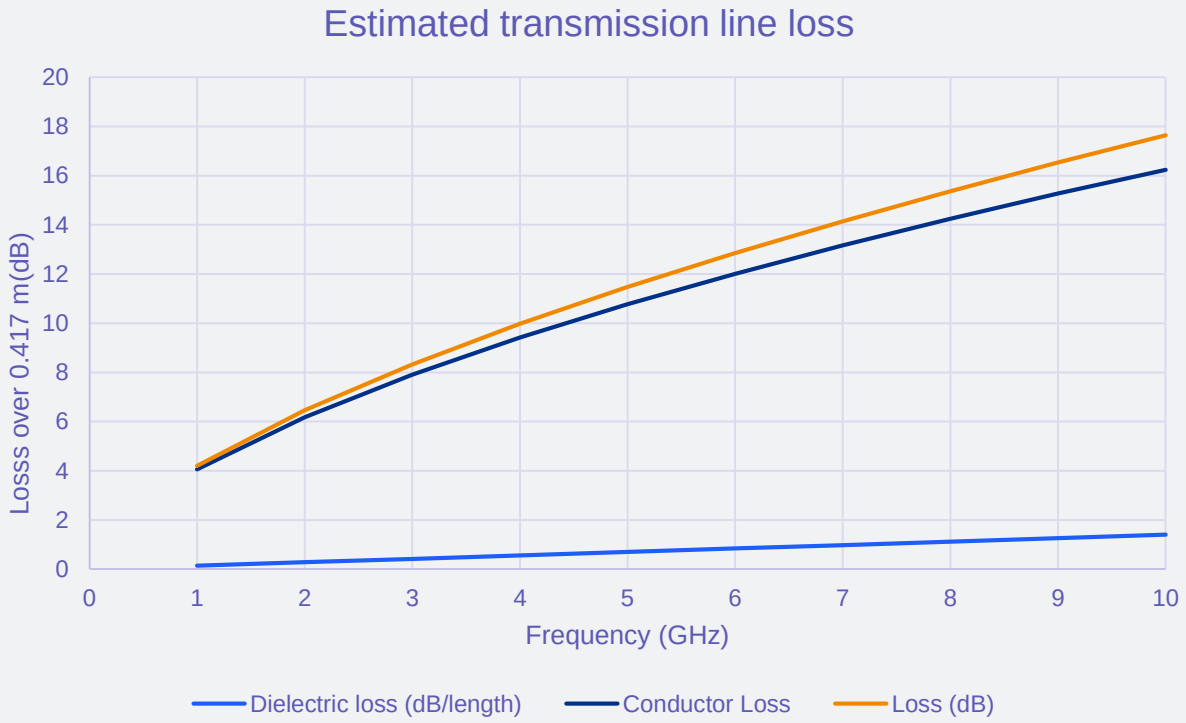
Connect HDS1…4 to scope via SMA cables.

- Scope DC coupled
- 50Ω terminated
- AC coupling provided on bridge FPC
- Monitor 2nd pair to study crosstalk.

Equipment

EK-U1-KCU105-G	https://www.digikey.co.uk/en/products/detail/amd/EK-U1-KCU105-G/5080514	KCU105
CCSMA-MM-SS402-24	https://www.digikey.co.uk/en/products/detail/crystek-corporation/CCSMA-MM-SS402-24/2137809	24 inch cable.
CCSMA-MM-SS402-36	https://www.digikey.co.uk/en/products/detail/crystek-corporation/CCSMA-MM-SS402-36/2137810	36 inch cable.
ADP-SMAF-BNCM	https://www.digikey.co.uk/en/products/detail/linx-technologies-inc/ADP-SMAF-BNCM/9826665	BNC to SMA adapter

Estimated transmission line loss



- Following equations from https://www.microwaves101.com/encyclopedias/transmission-line-loss
- Using Dk=3.4, Df=0.002 form Kapon HN film
- Al resistivity=3.77×10^{7} S/m
- What is acceptable loss?
  - JESD204 6 dB @ 0.75 line rate.
  - ATLAS ITk OB (1.28 GBit/s)
    - Spec. 20 dB @ line rate/2
    - Actual: 14 dB @ 640 MHz
  - VTRx+ Spec v2.9
    - TX diff input 200 mV to 1200 mV
    - Input jitter 0.26 UI

VTRx+ TX input Eye mask

Specification	Value
X1 @ UI=97.66ps	10.7 ps
X2	30.3 ps
Y1	95 mV
Y2	350 mV

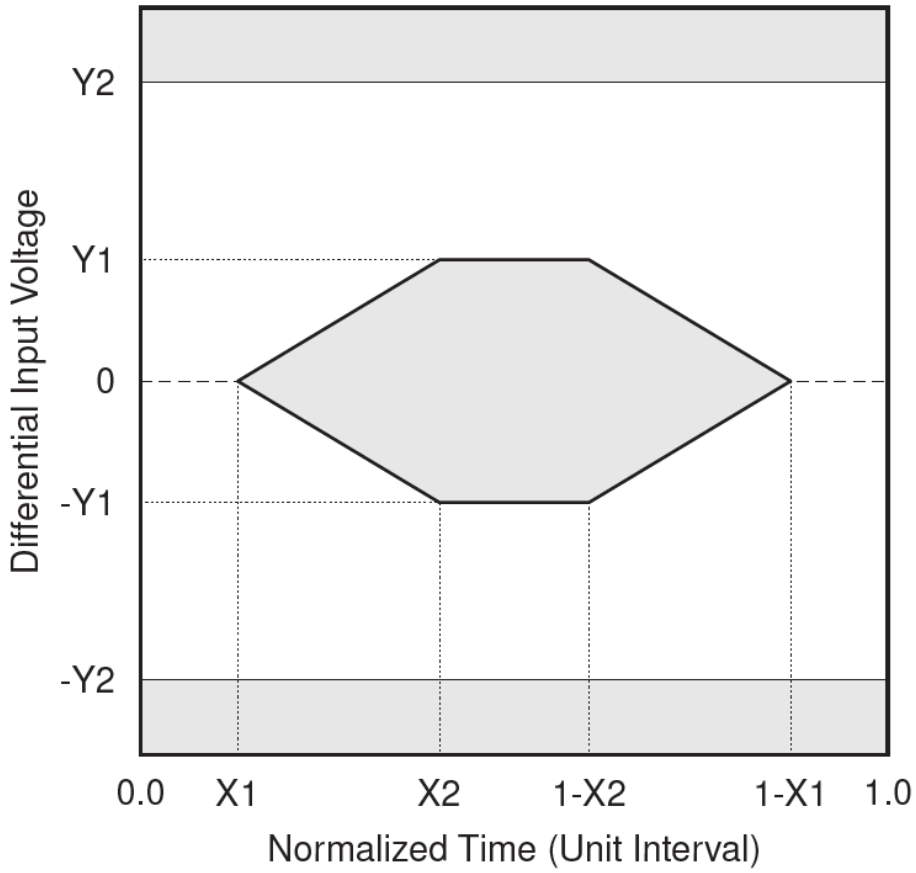
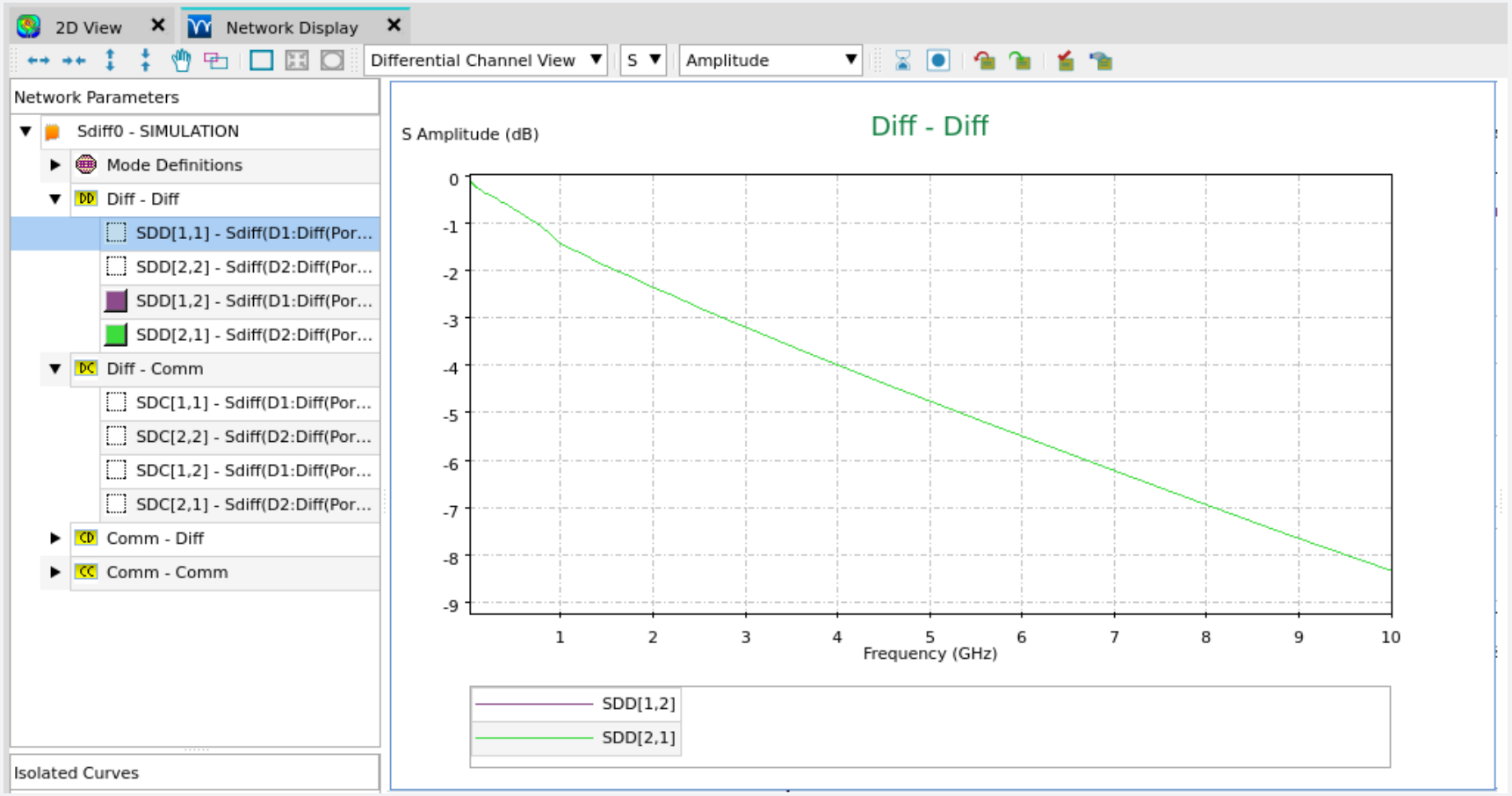


Figure 6: Electrical Eye Mask for 4.2.5 Tx Input & 4.4.5 Rx Output

Clarity3d layout simulations of 100 mm pair



- -0.076 dB at 10 MHz
- = 0.99 transmission
- expect 0.97 at DC
- -8.4 dB @ 10 GHz
- Predicted -4.23
- Explained by different values of Df.
- Clarity material: Df= 0.035 @ 10 GHz

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Thank you