Cross-talk evidence in EIC HRPPD backplane

(hopefully not in the anode plate itself)

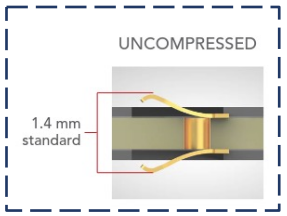
EIC HRPPD assembly

Fused silica window

MCPs, spacers, etc

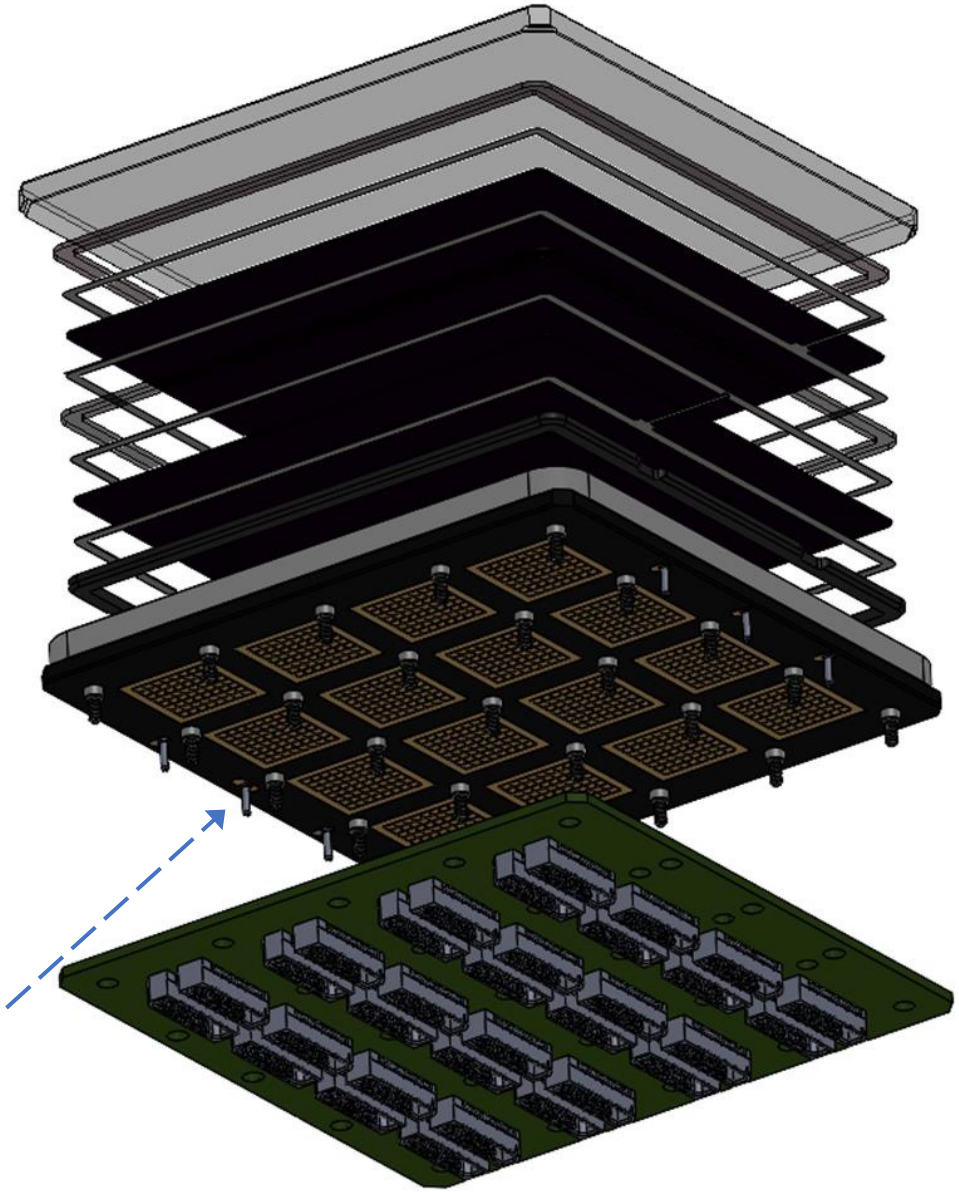
Side wall

Anode plate (Y03h),
a pre-routing ceramic circuit board



Compression interposers
(not shown)

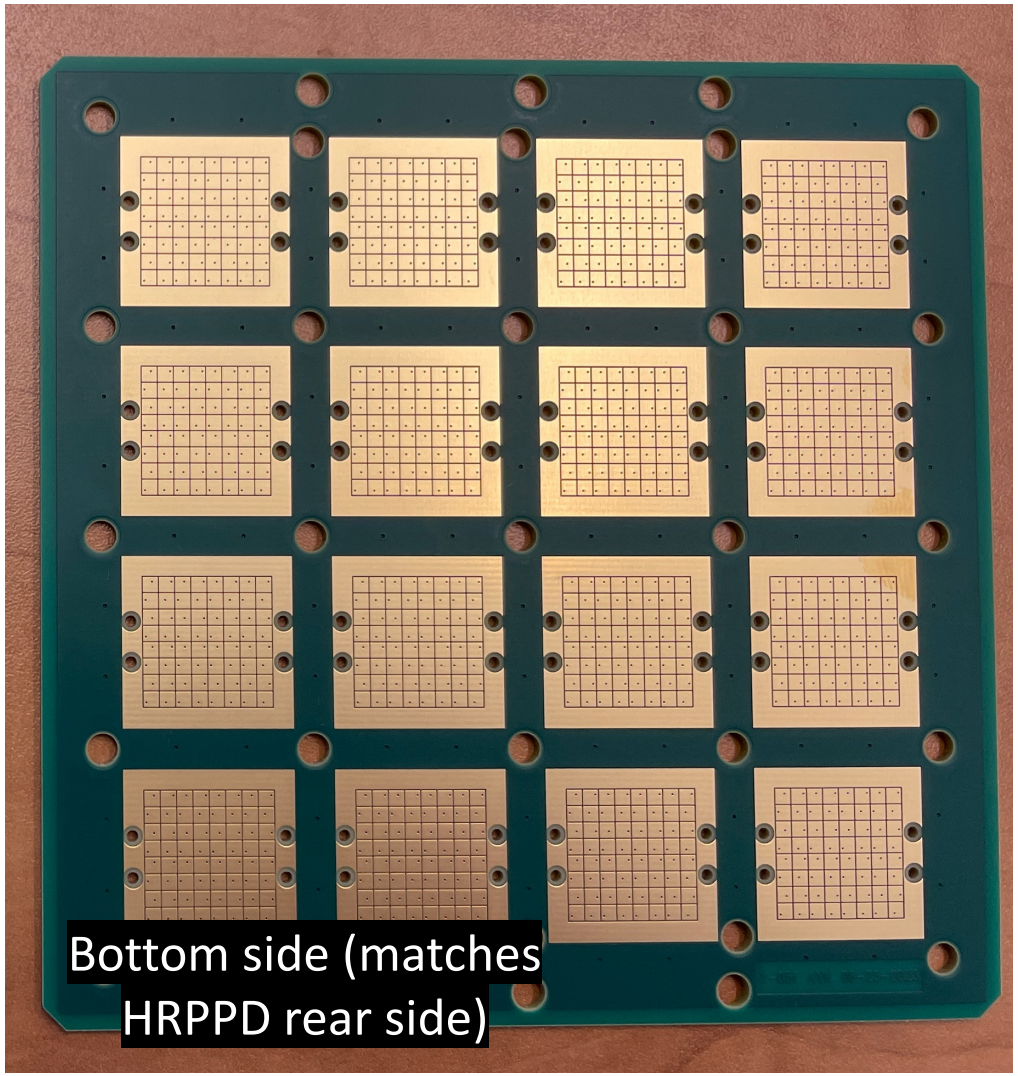
Interface PCB (Y05f)



4x4 spots, each with 8x8 square pads; 3.25mm pitch

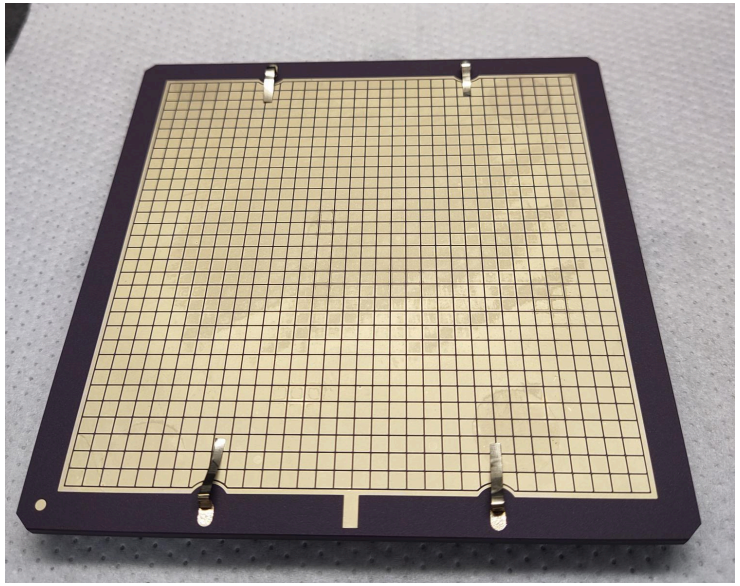
Charge path: (1) vacuum side anode pads -> anode plane stackup -> air side pads -> compression interposers -> (2) interface PCB -> MMCX adapter PCB -> pigtail RG-316 (?) cables -> 6” RG-174 cables -> V1742 digitizer

HRPPD passive interface backplane PCB (Y05f)

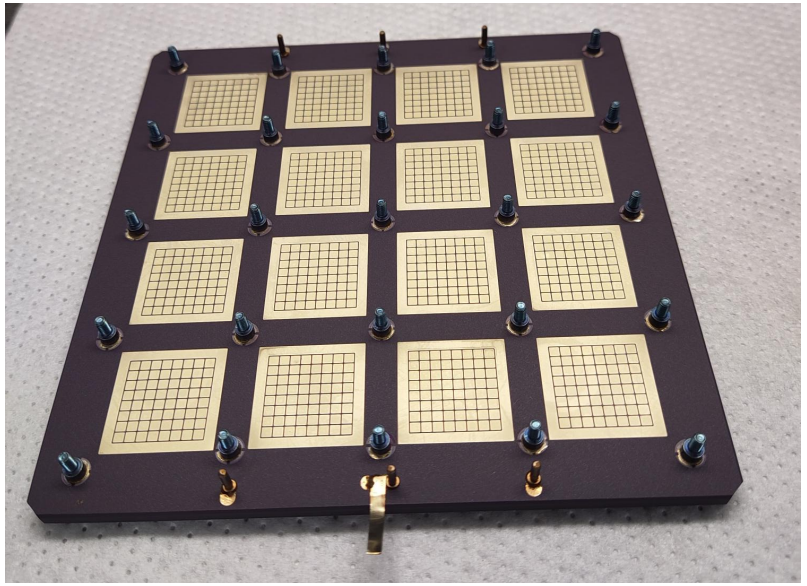


- A simple 119mm x 119mm two-layer board (through vias; Samtec ERF8 connectors)
- MPGD-style design (no signal line isolation in the Samtec connectors)

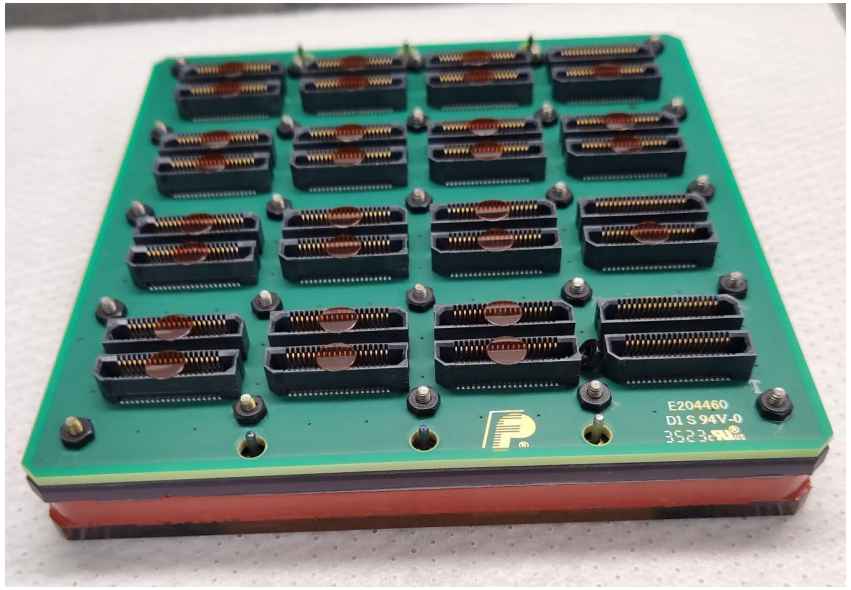
HRPPD picture gallery



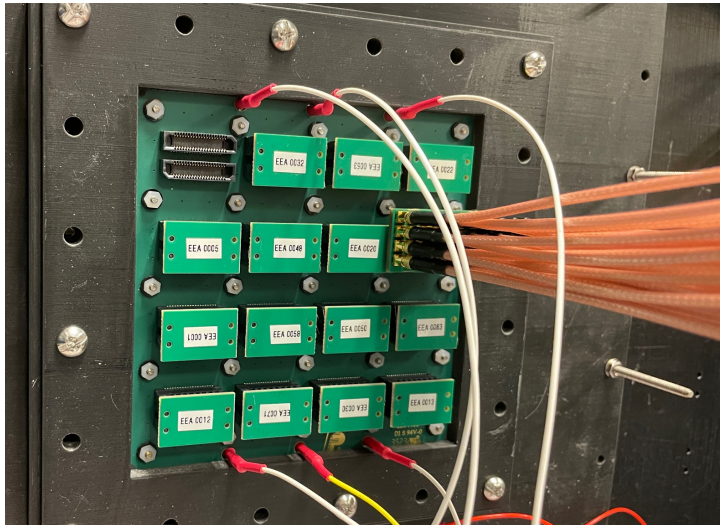
Anode plate vacuum side



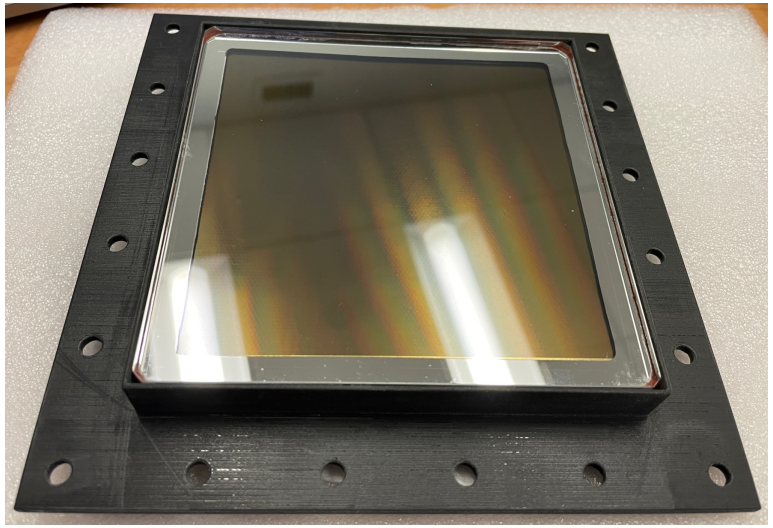
Anode plate air side



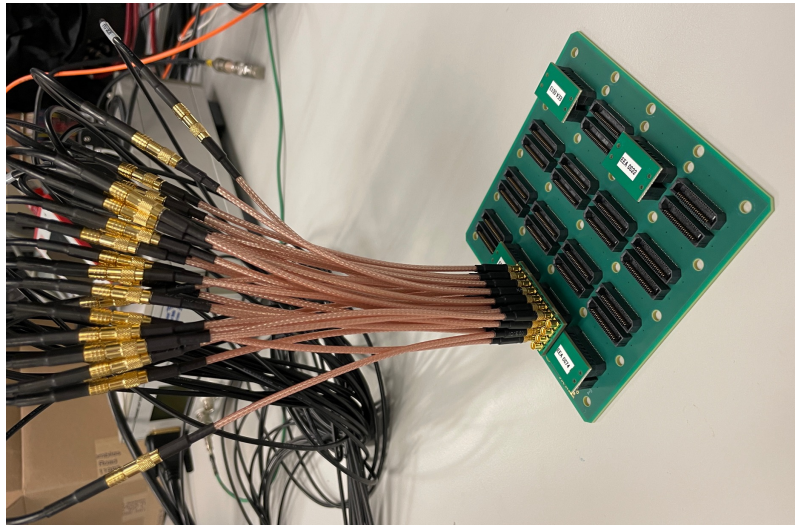
With Y05f board mounted



With MMCX interface

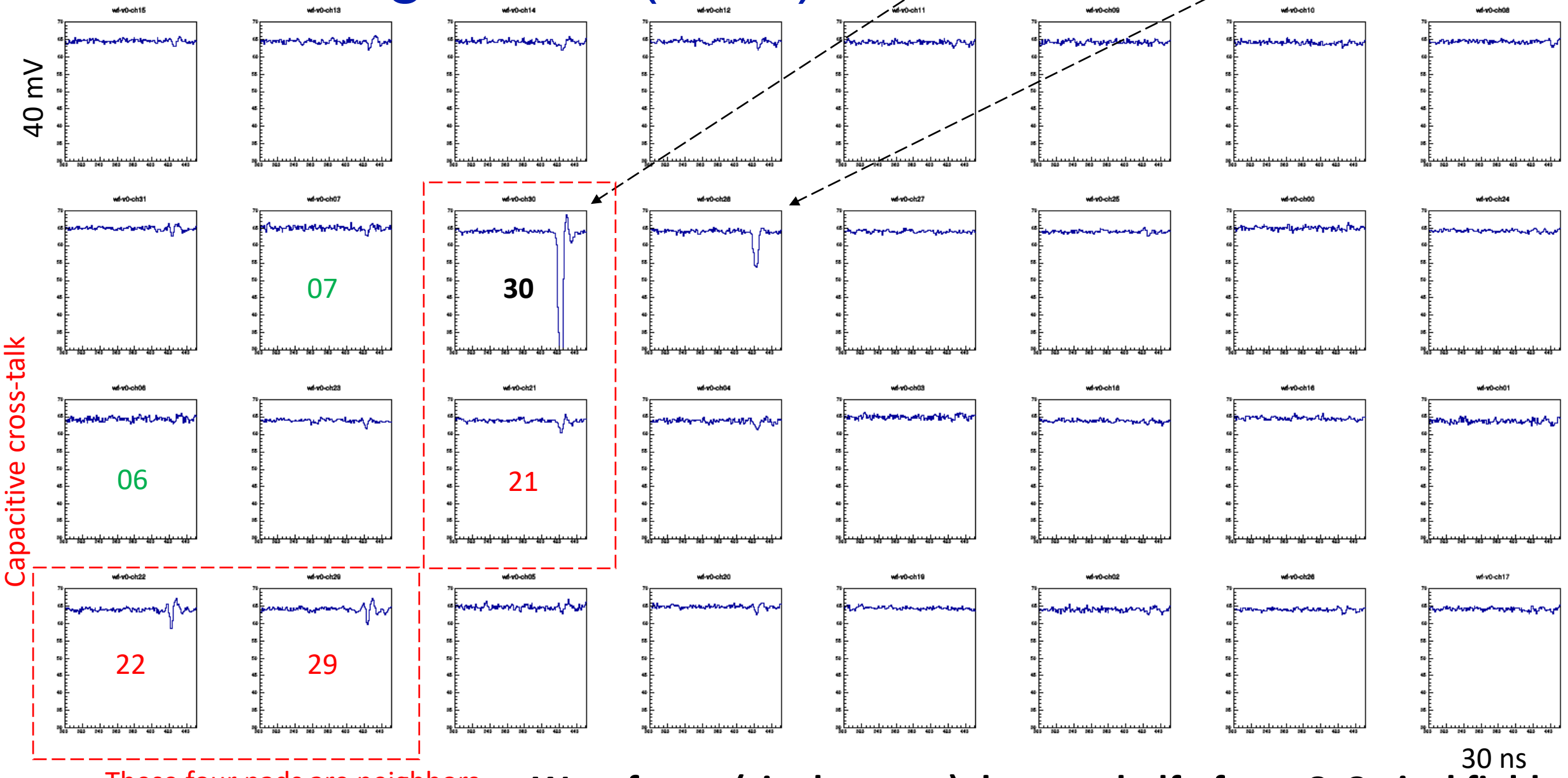


Fused silica window



Y05f board & MMCX -> MCX pigtail cables

Cross-talk signature (SPE)



These four pads are neighbors on a Samtec ERF8 connector

Waveforms (single event): bottom half of one 8x8 pixel field

Electronics channel routing of a single 4x8 pad area

Channel numbering 00 .. 31 as connected to a single V1742 digitizer

Neighbors on the Samtec connector (cross-talk evidence)

15	07	G	14	06	13	05	G	12	04	11	03	G	10	02	09	01	G	08	00
31	23	G	**30**	22	29	21	G	28	20	27	19	G	26	18	25	17	G	24	16

Samtec ERF8 / ERM8 connector pinout

Neighbor on the air side anode surface (no cross-talk)

15	14	13	12	11	10	09	08
07	06	05	04	03	02	01	00
31	**30**	29	28	27	26	25	24
23	22	21	20	19	18	17	16

Y05f -> HRPPD interface

Neighbor on the vacuum side anode surface (no cross-talk)

15	13	14	12	11	09	10	08
31	07	**30**	28	27	25	00	24
06	23	21	04	03	18	16	01
22	29	05	20	19	02	26	17

Physical HRPPD pad map
(bottom half of one of the sixteen 8x8 pad spots, as seen on the previous slide)

Mitigation efforts

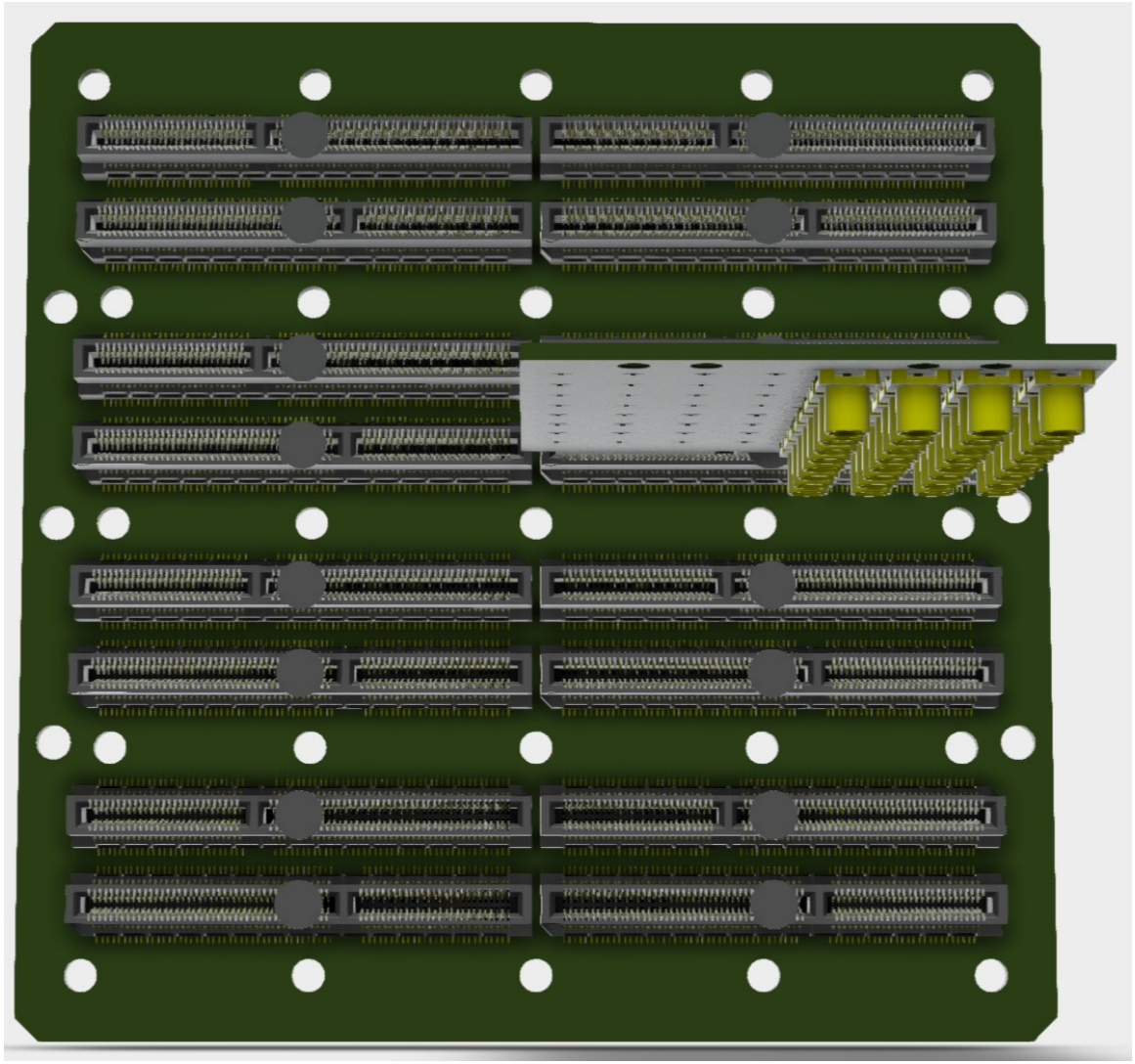
- A matter was being extensively discussed with EIC / ePIC experts over the last two weeks
- A meeting with BNL IO experts (Kayla Hernandez, John K.) was set up by Takao two days ago
  - Kayla and John are coming to 510D next week with a spectrum analyzer to measure the cross-talk in situ (assuming it does originate in the backplane connectors)
  - Will also perform these measurements on a different HRPPD interface with Samtec DV connectors

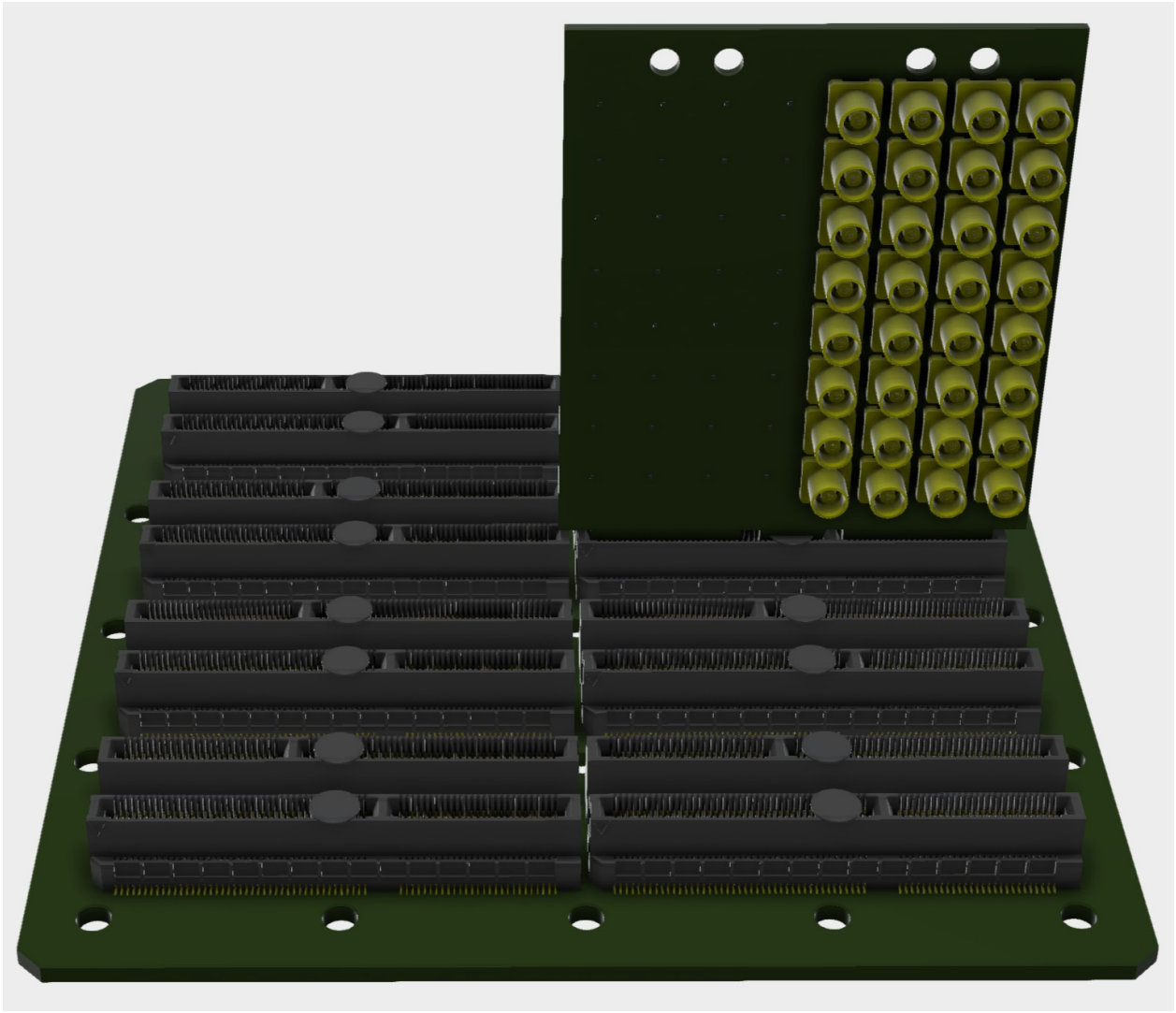
- In parallel, a new backplane design was being developed
  - A 12-layer backplane with a proper trace isolation in the stackup
  - 12-layer 32-channel MCX adapter edge cards of a similar stackup
    - Samtec MEC6-DV connectors with interleaved signal & ground pins and a separation ground plane
  - 50 Ohm termination plugin cards

  - Will be circulated for comments / suggestions by the end of this week

- If everything goes as expected:
  - Confirm the cross-talk origin and frequency spectrum next week
  - Converge on the new backplane design over the next week as well
  - Obtain quotes and apply for PED funds to produce N sets by the end of June

Preview of a new design (backplane & a single adapter)





- Backplane must be usable for ASIC plugin edge cards as well (if this is ever needed)