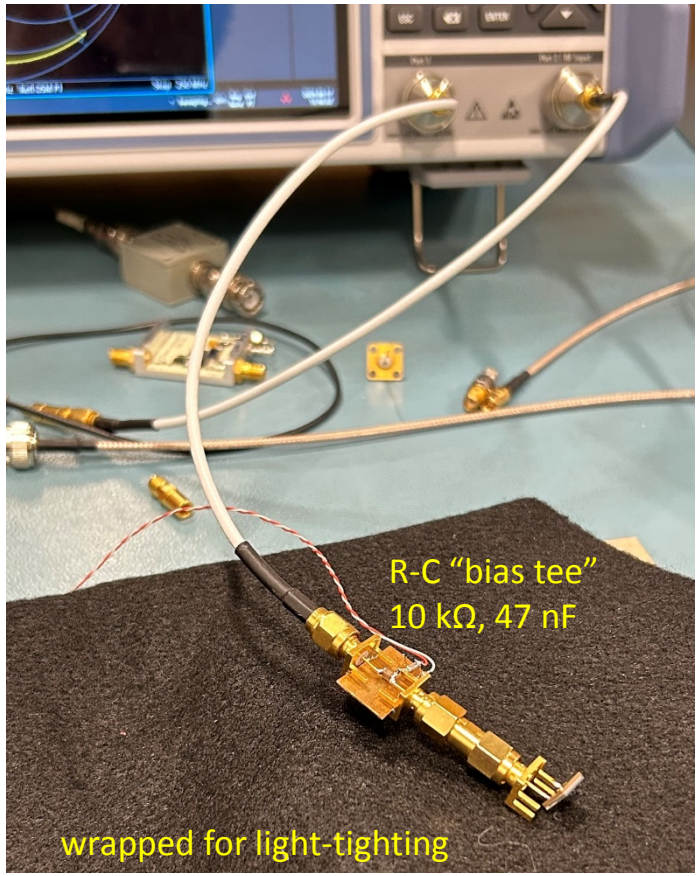
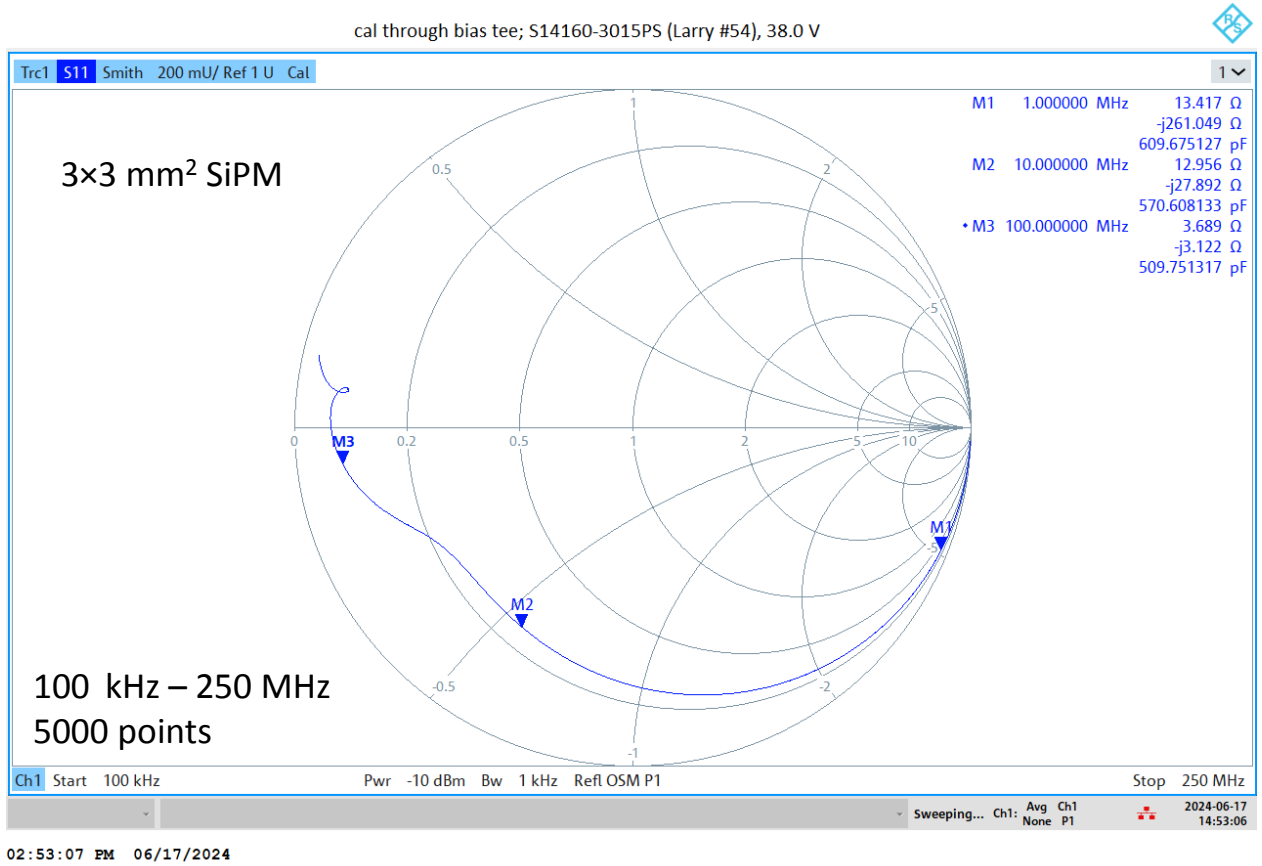
SiPM capacitance (and more) measurement

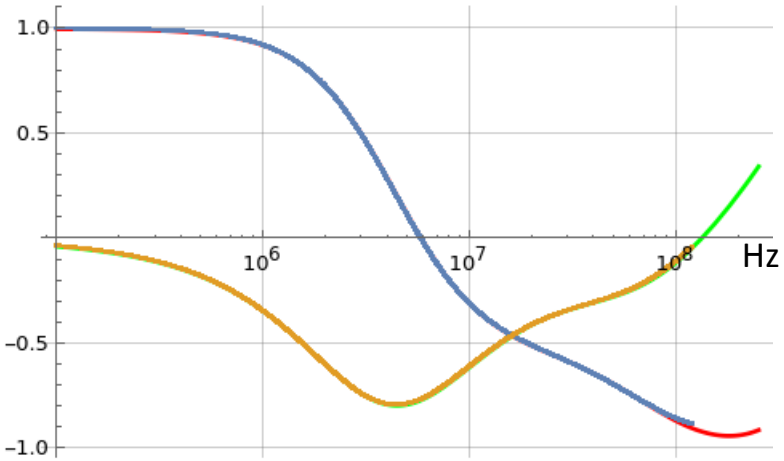
Can be done in various ways, but one good way that fits available tools here is to measure the reflection coefficient of SiPM on a 50 Ω cable. And then fit the reflection data with a circuit model of SiPM. Not shown here but a known value resistor + capacitor was also measured to verify the method.





6×6 mm² SiPM shown

reflection coefficient (S11) vs. frequency, and fit

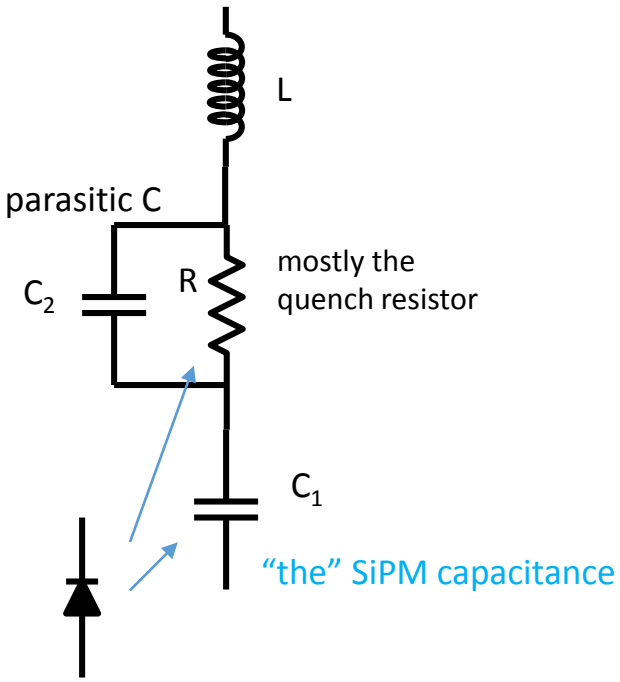


Fit results

3×3 mm^2 – a randomly chosen S14160-3015PS; 6×6 mm^2 – a randomly chosen S14160-6015PS

Size, mm^2	bias, V	C_1, pF	C_2, pF	R, Ω	L, nH
3×3	20	886.3	192.0	15.25	8.392
3×3	38	609.0	205.8	13.32	8.368
3×3	40	592.4	207.3	13.19	8.358
3×3	42	577.7	208.6	13.04	8.357
6×6	20	3544	574.4	4.957	10.143
6×6	38	2428	598.0	4.407	10.113
6×6	40	2363	600.5	4.361	10.109
6×6	42	2307	603.2	4.318	10.104

SiPM circuit model (simplified). Net equivalent of N cells in parallel.



diode contributes capacitance and some resistance

- 6×6 mm^2 device indeed is mostly just like 4× 3×3 mm^2 devices in parallel
  - somewhat higher R and much higher L than naïve value; probably makes sense (bigger chip)
  - C_2 is 25% smaller than expected? I don't understand that
- C_2 and L are fairly independent of bias, as expected since they should be predominantly connection parasitics
- C_1 has expected dependence on bias voltage, roughly ~ 1/sqrt(V)
- R is weakly dependent on bias voltage (at higher bias, thicker depletion → thinner bulk → expect lower R)

Details matter for circuit design / simulation, but executive summary is these devices are the same excepting size; capacitance & all that *depends only on overall area implemented in the system (in a parallel connection)*.

SiPM choice discussion

My perspectives on 3×3 mm^2 vs. 6×6 mm^2 choice. For discussion FWIW.

	3×3 mm^2	6×6 mm^2
Capacitance **per unit area**	64.2 pF/mm2	64.1 pF/mm2
irradiated DCR per unit area	same (details TBD)	
cost	(stated elsewhere)	(stated elsewhere)
PDE	same	
chip to PCB thermal impedance *	"standard"	**new and improved**
package self-alignment in soldering	probably worse	probably better
array to be used	4 × 4 or 4 × 5	2 × 2
readout ch to be used per crystal **	1, 2, 4, … , 16 or 20	1, 2, or 4

* This factor may turn out to be important after radiation damage, to avoid over-warm SiPM's having yet higher DCR, or warming the crystals too much.

** I do not believe we will benefit from multiple readout channels per crystal, particularly for the discrete/COTS readout option. But it is conceivable and certainly worth contemplating, especially in a low cost ASIC-based readout. Nevertheless, I don't believe we will use >4 readout channels per crystal… So this added flexibility in 3×3 mm^2 case, I do not believe it is really useful.