MPGD FEB – RDO connectivity

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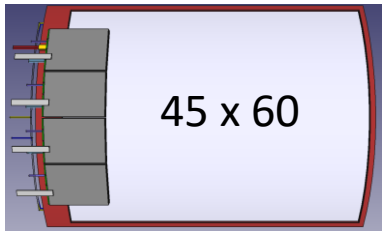
Outlook

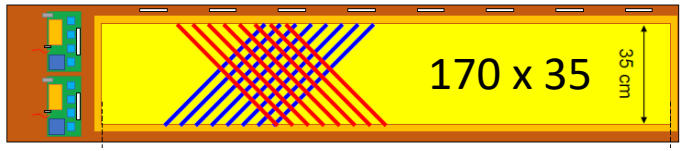
- Options for placing RDOs
- Reminders
  - → Salsa Interface
  - → FEB powering schemes
  - → FEB-RDO connectivity options
- Number of MPGD FEBs and RDOs
- Envisaged studies of FEB-RDO connectivity
- Summary

Reminder on MPGD sub-systems and channel counts

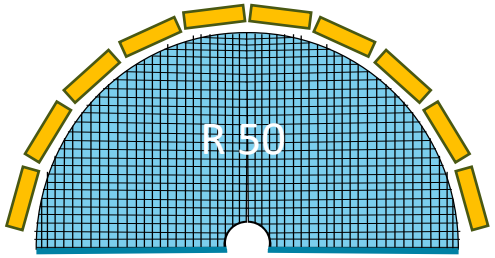
- Cylindrical Micromegas Barrel Layer : CyMBaL : ~30k channels
  → 32 tiles of 1024 channels each



- µRWELL Barrel Outer Tracker : µRWell-BOT : ~100k channels
  → 24 modules of 4 096 U-V strips each

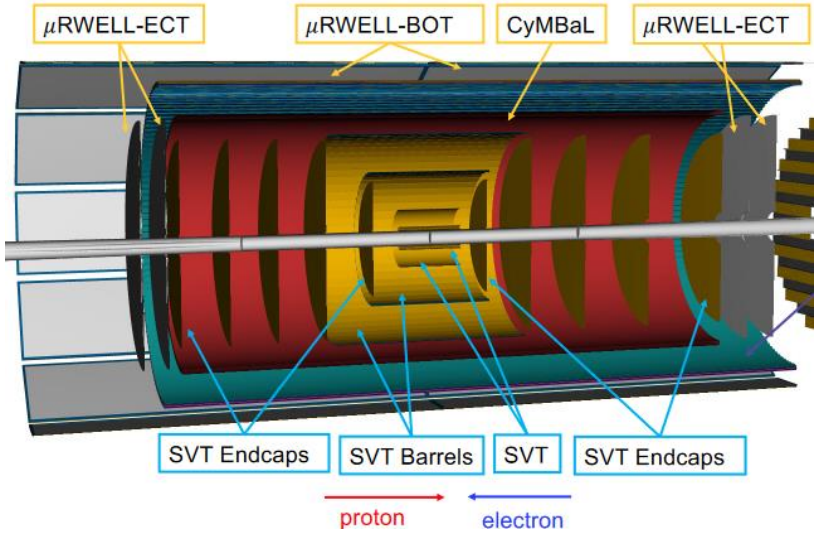


- µRWell End Cap Tracker : µRWell-ECT : ~30k channels
  → 8 half-disks of 4 000 X-Y strips each



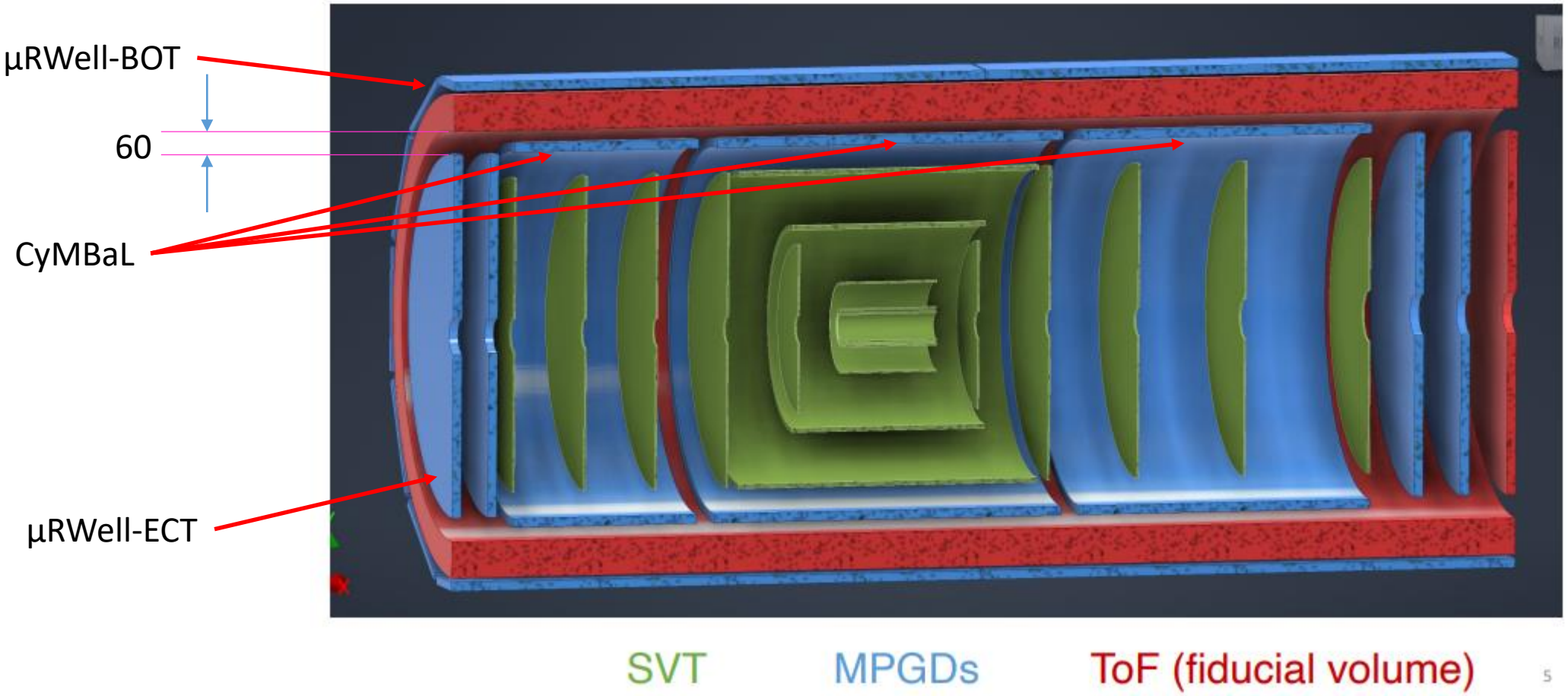
- ~160k-channel heterogeneous system
  → Micromegas, µRWell, barrel, endcap, curved, planar, circular

- Common approach to acquire data from different types of ePIC MPGDs
  → Use same frontend ASIC
  → Share frontend design between groups
    - Adapt form factor if needed



Spatial constraints for inner barrel cylindrical tracker

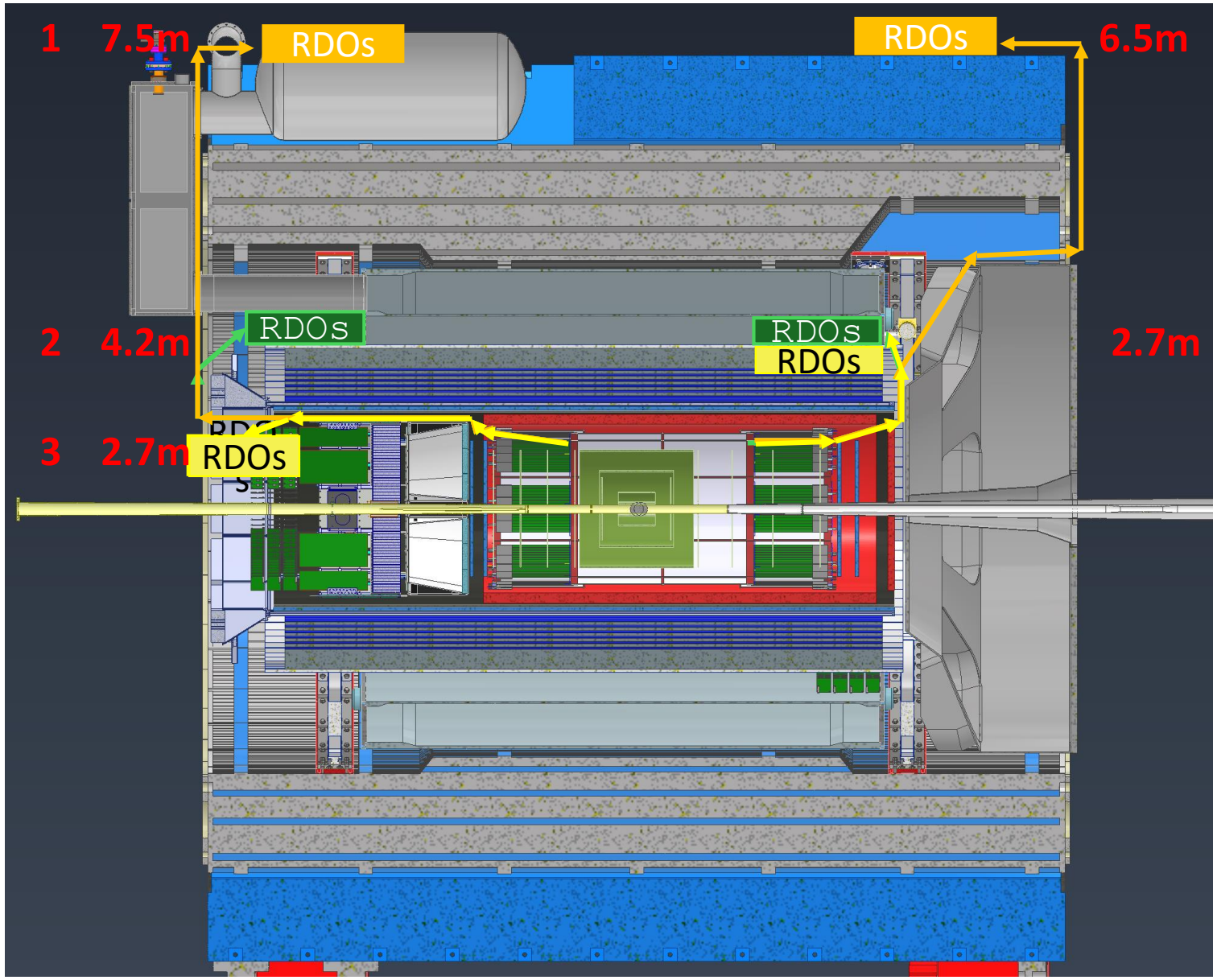
- Space is stringent: 6 cm
  → Detectors, gas pipes, HV cables



- On detector frontend electronics
  → FEBs + LV distribution + RDO interface cabling + cooling

Options for placing the RDOs

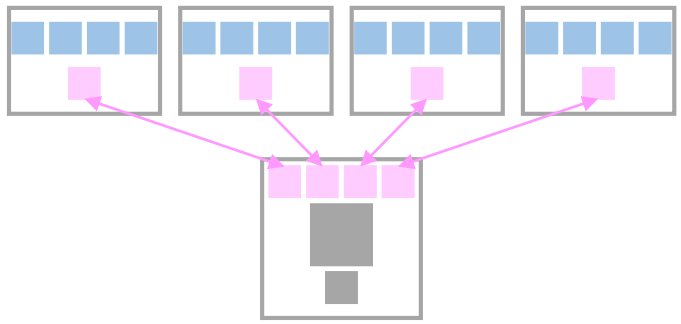
- 3 options
- Option 1 :
  - → Better for installation and maintenance
  - → Better for powering
- Options 1-2-3
  - → Difficult for bulky data cables
    - In addition to services
- Impact on FEB – RDO interface
  - → Optical versus electrical
  - → ASICs per FEB
- Impact on power consumption and cooling

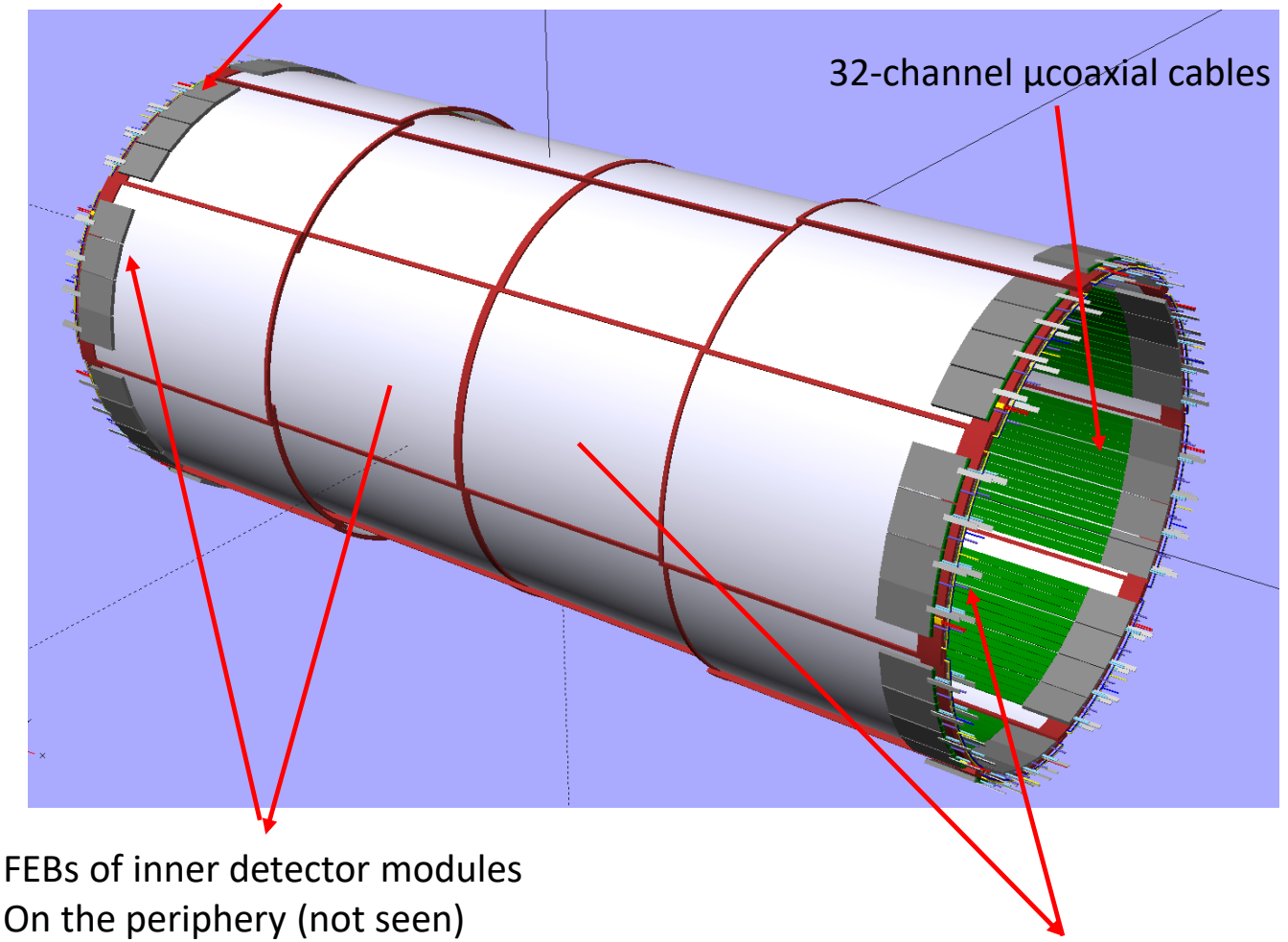


Example of CyMBaL configuration under study

- 32K channels
- 128 256-channel FEBs
  → 4 Salsa ASICs per FEB
- 32 1024-channel RDOs
  → 4 FEBs per RDO

16 Salsa-s, 4 FEBs, 1 RD0 = 1024 channels



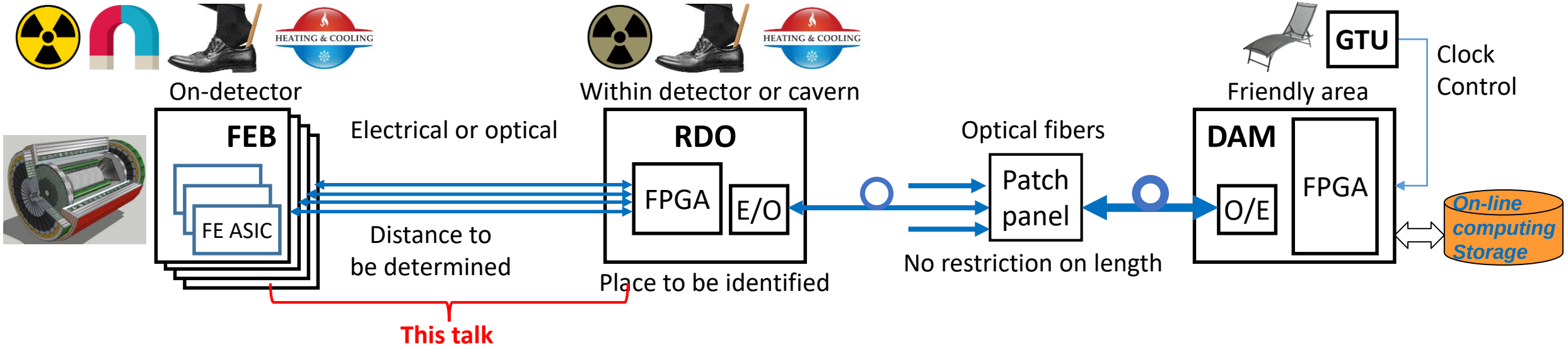


Is there an extra length accounted for cables ?

- Looks like FEB-RDO cable length for inner detector modules is estimated from the module edge
  → Probably there is some extra 0.5 m, but does not change an overall picture

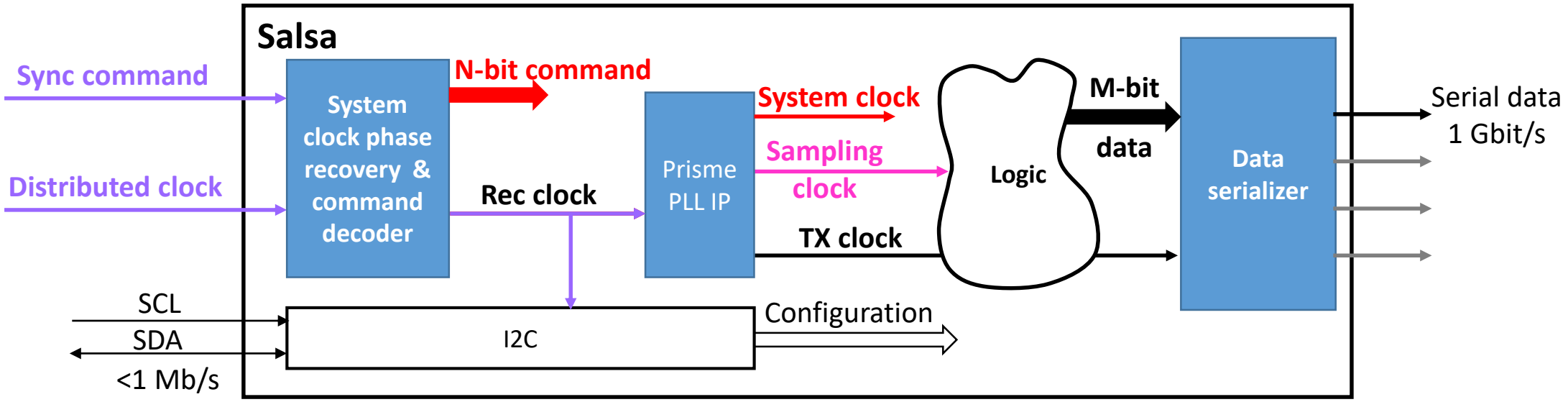
Salsa interface options

Readout organization of ePIC detector

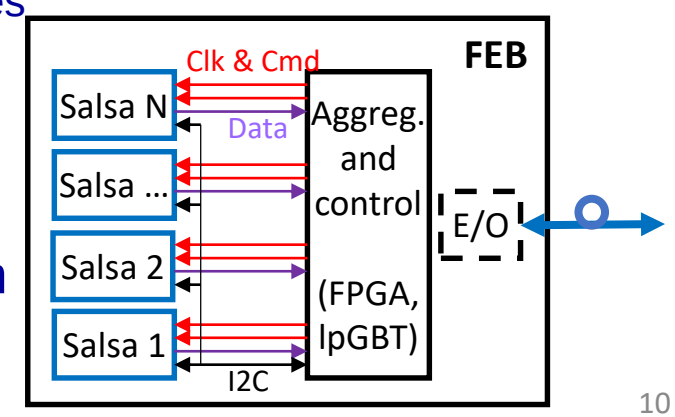


- FEB – frontend board with readout ASICs
  → MPGD : common design based on Salsa, form factor adapted to detector module geometry
- RDO – readout module – first stage of FEB data aggregation, last stage to dispatch clock & control
  → Mostly common design framework between sub-detectors, different form factor
- DAM – data aggregation module – interface with computing and global timing and control unit (GTU)
  → Common design for all sub-detectors
- Downstream towards detector : clock, control, monitoring
- Upstream towards storage : physics, calibration, monitoring data

Support of “traditional” prevalent interface

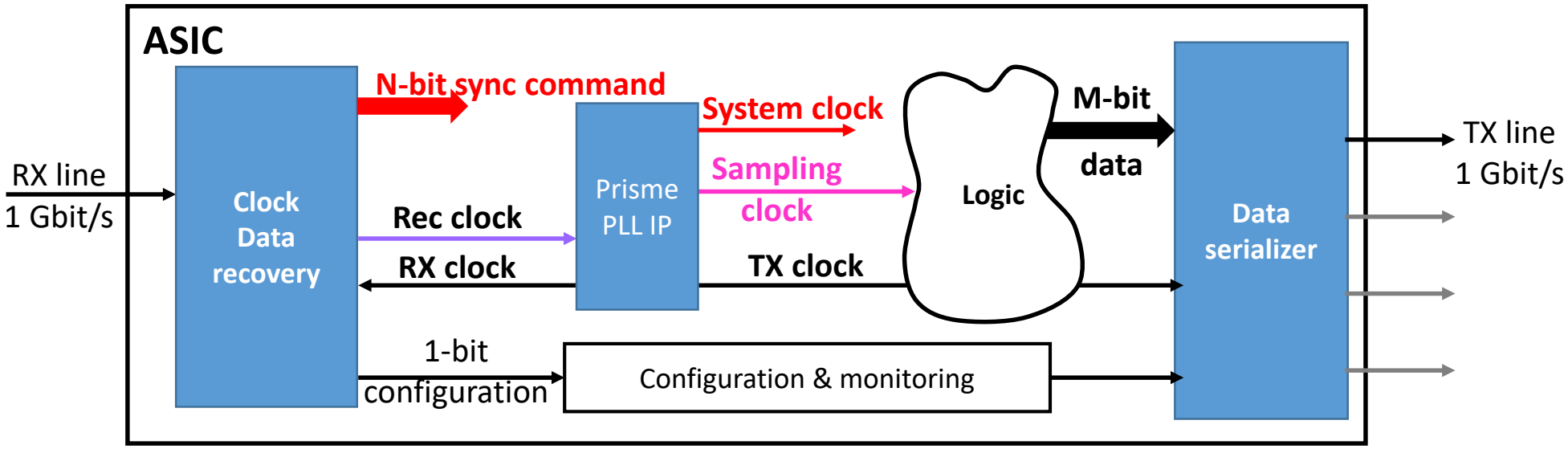


- Important number of heterogeneous external interface signals proper for each functionality
  - → Clock_diff_in, SynCmd_diff_in
    - Synchronous commands decoding options in backup
  - → SCL_in, SDA_io
    - Configuration of ASICs on a FE board in series : longer startup and recovery times
  - → Up to 4 Data_diff_out serial links
  - → Additional IOs like Trigger_diff_in, TrigPrim_diff_out



- May require an on-board companion intelligence for control & aggregation

Alternative “unified” interface



- Single encoded RX line for Clock, SynCmd, Trigger, configuration and monitoring
  - → Minimal external interface: a single diff RX line + at least one diff TX line
    - Simplest case: only 4 pins (Rx_p / Rx_n + Tx_p / Tx_n) to communicate with the chip
    - Parallel configuration of ASICs possible : fast startup and recovery time
- Relatively complex initialization phase requiring collaboration from the remote partner
  - → Clock recovery phase followed by
  - → Data reception and transmission phase

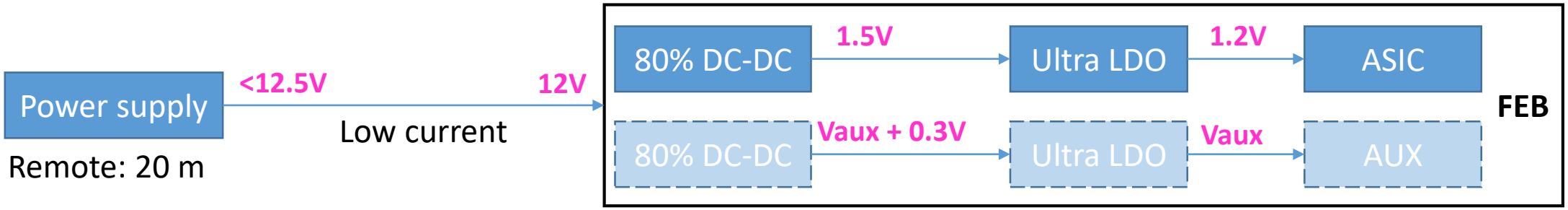
FEB powering options

FEB power distribution options : DC-DC

- DC/DC-based LV distribution: to be magnetic field tolerant

→ Remote power supply distributes 12V with a low voltage drop over 20 m cables

- Say less than 0.5V
  - The lower the drop the lower the power dissipation in cables but the large is their cross-section



→ Higher efficiency

→ Low cross-section power cables

→ Less overall* mW/ch

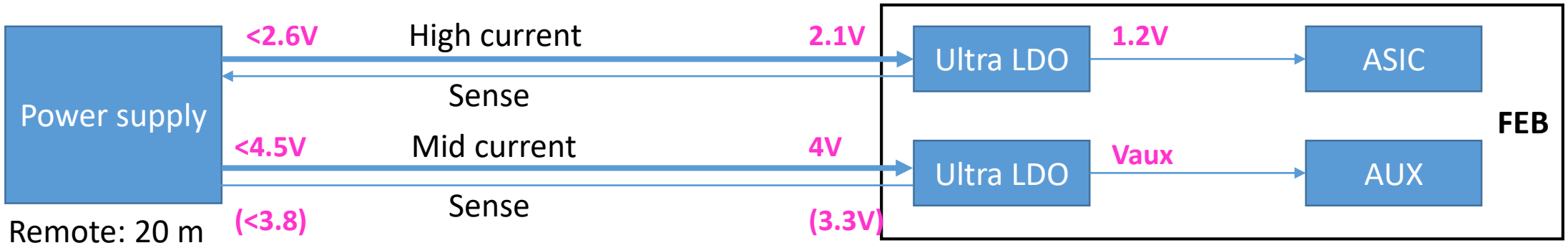
*Overall : Power supply W / nb of channels
includes loses in cables, regulator inefficiencies

→ DC/DC regulators might be bulky and a source of EMI

- Space + extra material for shielding
- Not clear if 80% efficiency can be really achieved

FEB power distribution options : LDO

- LDO-based LV distribution
  - → Remote power supply distributes 2.1V and any auxiliary voltages with a low voltage drop over 20 m cables
    - Say voltage drop is < 0.5V
      - The lower the drop the lower the power dissipation in cables but the large is their cross-section
  - → Low cross-section sense wires for remote power regulation



- → Lower efficiency
- → High cross-section power cables
  - Space due to thick cables
- → High overall* mW/ch

*Overall : Power supply W / nb of channels
includes loses in cables, regulator inefficiencies

About powering and cooling

- Count on the ePIC community effort to devise compact DC-DC regulators
  → ~2 T magnetic field and mild radiation tolerant

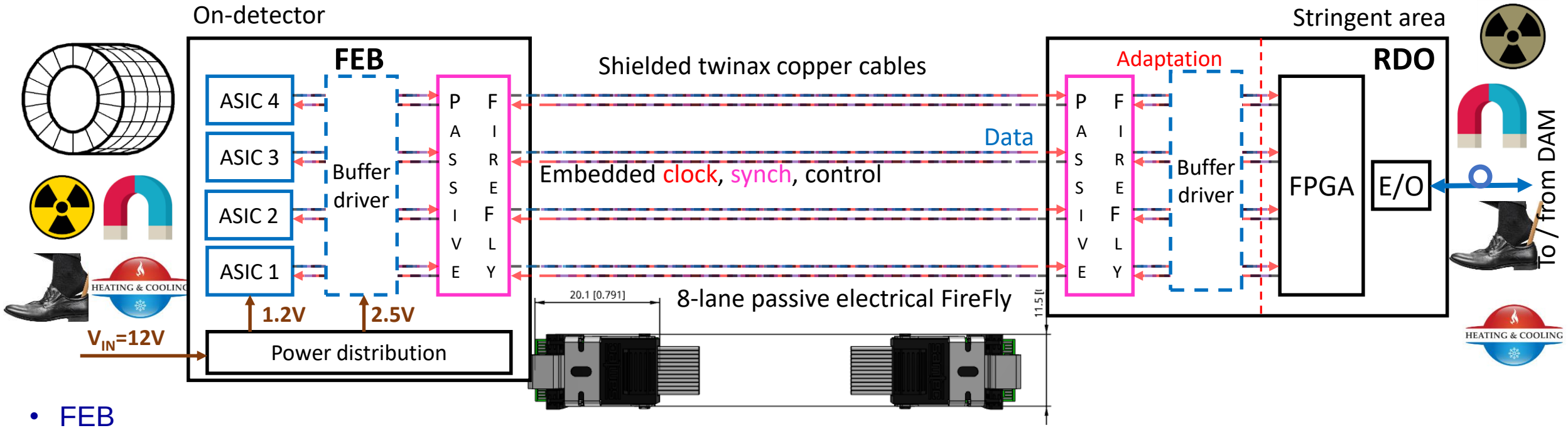
  → Crucial for FEBs

- Need an input / advise from RDO colleagues on RDO powering scheme
  → Can be problematic if RDOs are on-detector or within the magnetic field area
  → Understand RDO power consumption

- Cooling not yet addressed
  → To be started for FEBs
  → To be understood for RDOs if within the detector

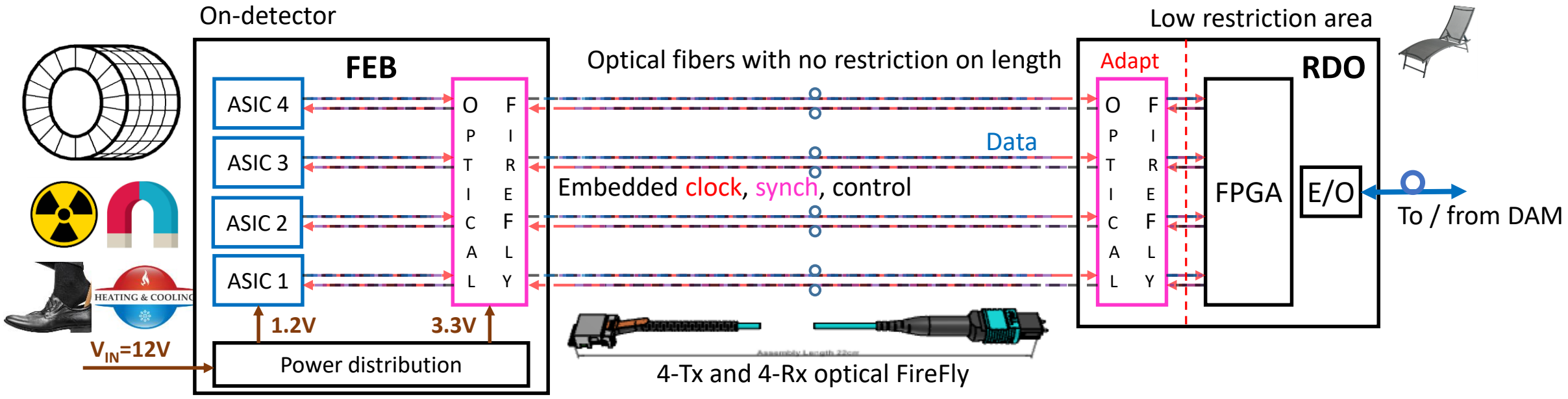
FEB-RDO connectivity

256-channel FEB with electrical “unified” interface



- FEB
  - → Low active component count: minimal power consumption
    - ~30-35 mW / channel
    - 1 mm^2 (DC/DC + LDO) or 5.6 mm^2 (LDO only) wires to power a FEB
- RDO
  - → Study is needed to evaluate the distance
    - ALICE MFT : up to 7m with ~1 Gbit/s links and some number of intermediate connectors
    - Our experience with CLPS drivers : 2-3 m with pre-emphasis techniques @ ~500 Mbit/s
    - The need of active drivers – buffers to be evaluated and their impact on power consumption
  - → May suite µRWell-BOT and partially µRWel-ECT for option 2 RDO placement
- Attention must be payed to ground loops and to noise pickup over long distance

256-channel FEB with optical “unified” interface



- FEB
  - → Low active component count
    - Samtec FireFly : reported to stand TID of 50-100 krad and neutron fluence of at least $5x10^{11}$ n_{eq} / cm^2
    - ~35-37 mW / channel - 15% increase compared to pure electrical interface
    - 1 mm^2 (DC/DC + LDO) or 6 mm^2 (LDO only) wires to power FEB
- RDO
  - → Can be placed anywhere in experimental hall with no particular environmental restrictions
- Optimal tradeoff between complexity of the on-detector electronics and its power consumption

Connectivity volume

FEBs and RDOs for MPGDs

- Estimates of operational quantities for MPGDs assuming 256-channel FEBs

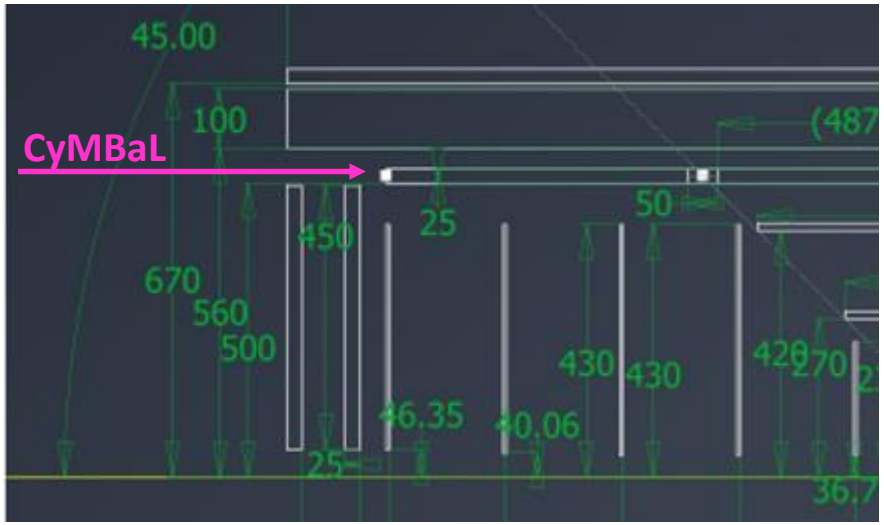
	CyMBaL		µRWell-BOT		µRWell-ECT		Total
	Tile	Sub-detector	Module	Sub-detector	½ disk	Sub-detector	MPGDs
FEB	4	**128**	16	**384**	16	**128**	**640**
RDO	1	**32**	4	**96**	4	**32**	**160**

- As many cable assemblies as FEBs

- CyMBaL
  - → Assume ±Z symmetry in cable distribution
  - → Assume even distribution in Φ over 500 mm radius
  - → 64 cable assemblies over 3.14 m
  - → 5 cm / cable assembly

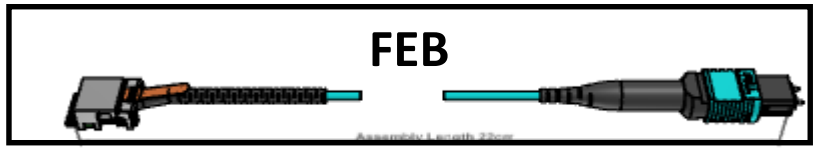
- Estimations for µRWell detectors : need to coordinate ourselves
  - → Probably similar situation for µRWell-ECT
  - → µRWell-BOT : 3 times more cables but also greater perimeter

- Number of RDOs is considerable : place ?!



Cable assembly types

- Parallel optics



Short pigtail / on board

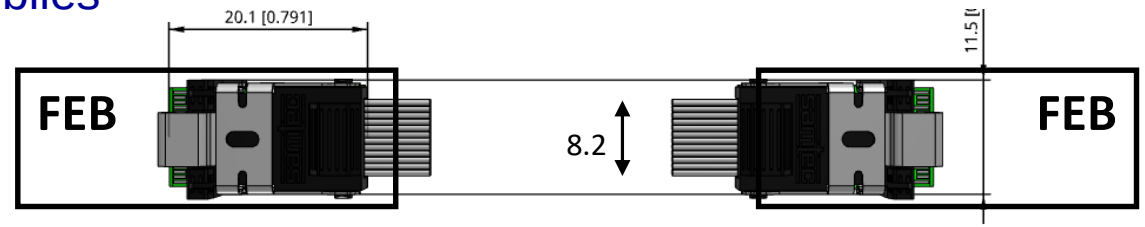
Long, halogen free, low smoke …

Short pigtail / on board

→ Optical power budget to be estimated
  - Usually fine, but long term radiation effect needs to be understood

→ Low cross-section even with protection jacket

- Twinax cable assemblies



Probably in one piece

→ Compact enough to fit FEBs but may be too bulky for cable trays
  - 320 units to bring out at each Z side

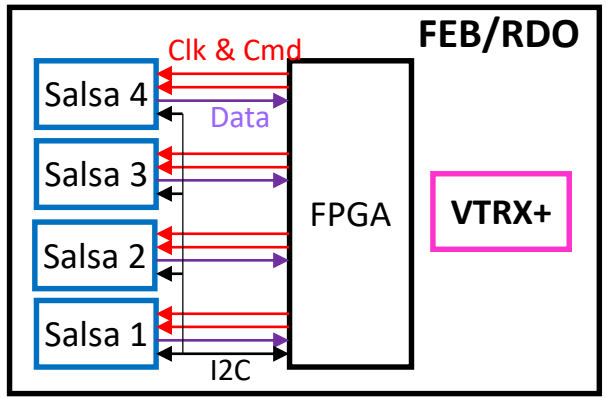
→ Need to understand if low smoke halogen free options exist

→ Rigidity, weight

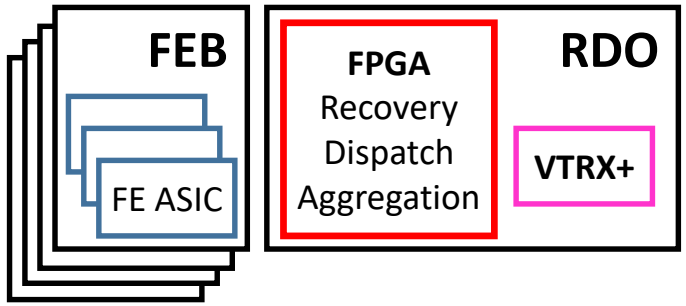
Can we get rid of bulky copper cable assemblies ?

- Closely integrated FEBs and RDOs
  - → Use “traditional” interface if on the same board
  - → Short twinax and flat cables in between if on separated boards

- Merged 256-channel FEB / RDO : worst power consumption scenario
  - → 50% increase compared to a FEB with electrical RDO interface
    - 45-50 mW / channel
    - 1.5 mm^2 (DC/DC + LDO) or 8 mm^2 (LDO only) wires to power FEB



- An RDO per detector module : 4 FEBs / RDO – 1024 channels
  - → ~11% more power compared to a FEB with electrical RDO interface
    - 33 – 37 mW / channel
    - 1 mm^2 (DC/DC + LDO) or 6 mm^2 (LDO only) wires to power FEB

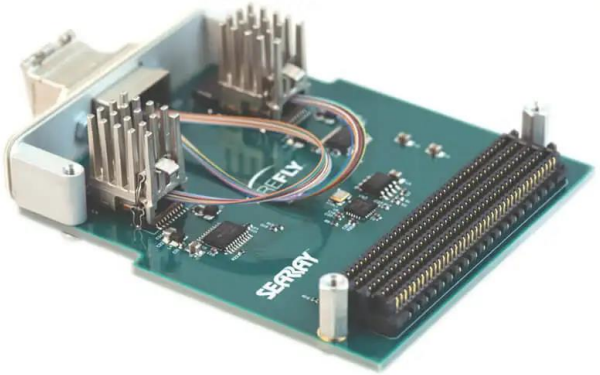


- Estimations for favorable VTRX+ case, should be higher with COTS transceiver
- Cooling and its additional infrastructure !
- SEU effects need to be understood, acceptable failure rates to be agreed on
- Powering FPGA requires “whole lotta” different voltages : (3V3), 2.5V, (1.8V), 1.2V, 1V, (0.9V)
  - → Deriving them from a single auxiliary power source may be inefficient
  - → Avoid mixing analog digital power sources

FEB-RDO connectivity studies

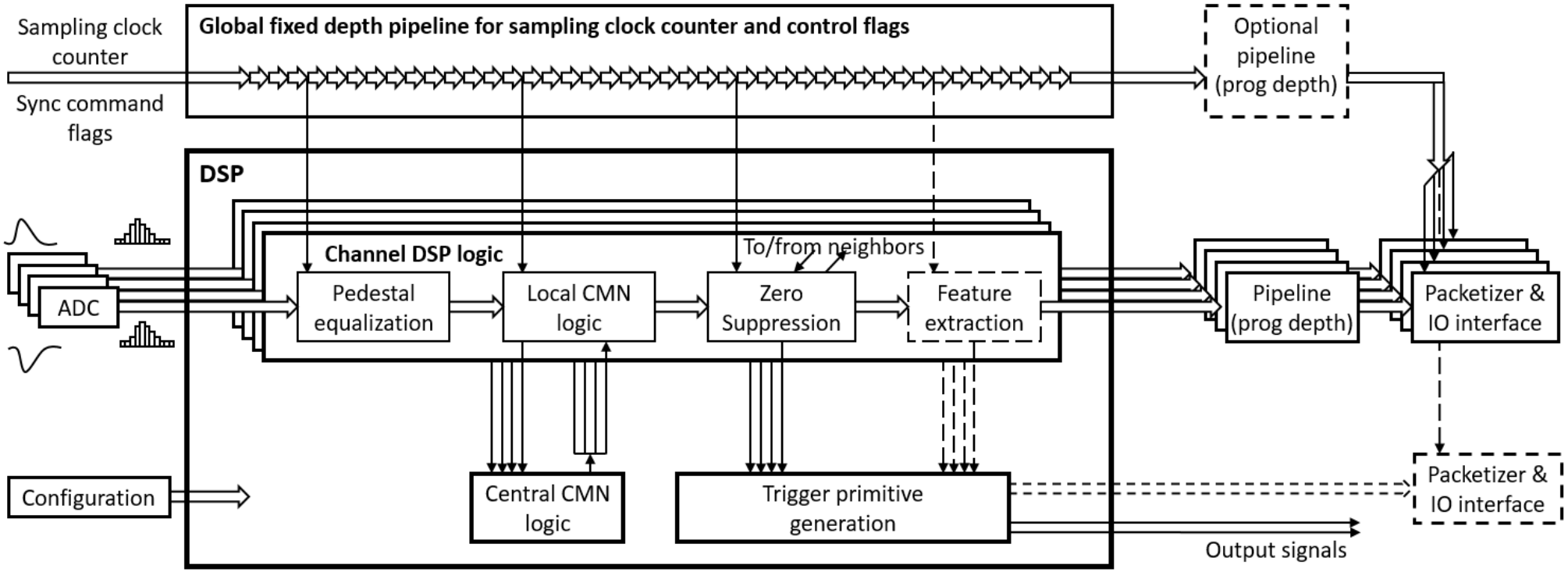
Initial steps

- Use of commercial evaluation kits for FireFly
  - → FMC-based board to use general purpose FPGA IOs
  - → Power consumption of 4-lane bidirectional optical component
  - → Cooling needs



- Radiation tests
  - → PRBS traffic loopback to detect Single Event Transients
  - → FMC extender cables to separate FireFly-s from FPGA development kit

Develop (port) Salsa “Digital” on an FPGA platform



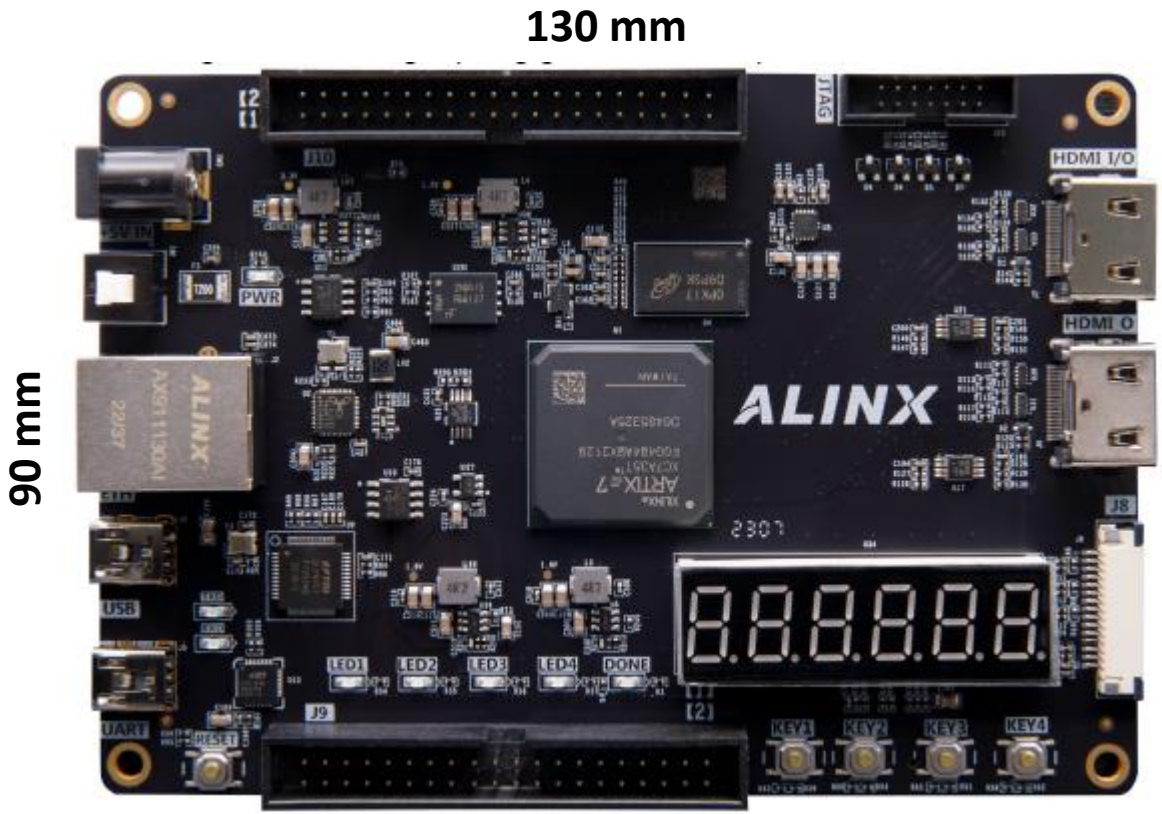
- Accelerate development of the DSP and serial lines
- Progress on Salsa2 test bench development
- Produce a platform to study and validate FEB-RDO interface

FPGA platform

- Preferably cheap to be produced in required quantities if needed
- Sufficiently performant to achieve ~1 Gbit/s speeds over standard IOs with embedded SERDES IPs

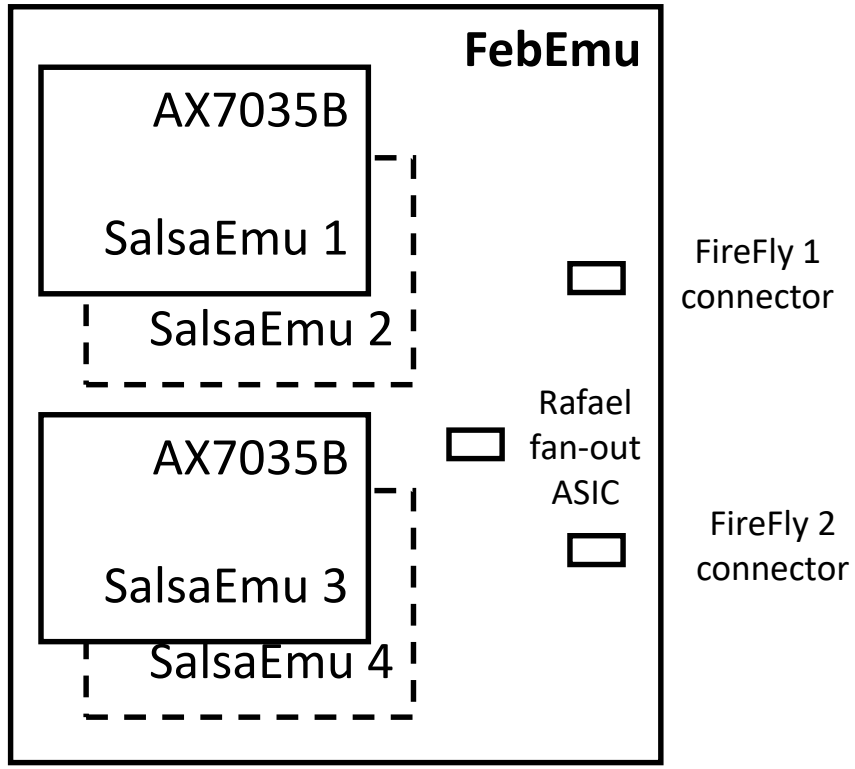
- A possible candidate could be AX7035B evaluation board from ALINX with ARTIX-7 FPGA from Xilinx
  - → XC7A35T-2FGG484I
  - → 256 MB DDR3 SDRAM
  - → 1 GE
  - → 2 HDMI
  - → USB
  - → 2 40-pin expansion ports
  - → $130

- AX7035B = Salsa
  - → Design of central CMN logic exists



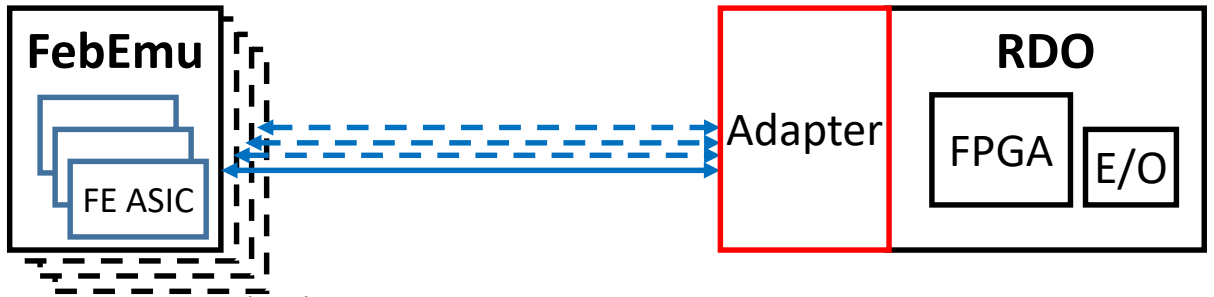
FEB emulation platform

- A relatively simple almost passive PCB
  - → 4 Salsa emulators
    - 2 on each side to fit 6U Eurocard size
  - → 2 FireFly connectors either for optical or electrical components
    - FireFly 1 : 8-lane for “Unified” interface
    - FireFly 2 : 8-lane for “Traditional” interface
      - Clock_in, SyncCmd_in, 4 TX_out, 2 I2C
  - → Rafael ran-out ASIC for Clock and Sync command distribution
    - Radiation hard
    - To be used for “Traditional’ Salsa interface
  - → LVDS driver / buffers, I2C ?
    - For long distance tests



- Radiation qualification tests
  - → Salsa emulators separated from FireFly

- FEB-RDO connectivity / protocol development and validation
  - → RDO-side firmware plug-ins
  - → RDO-side hardware interface



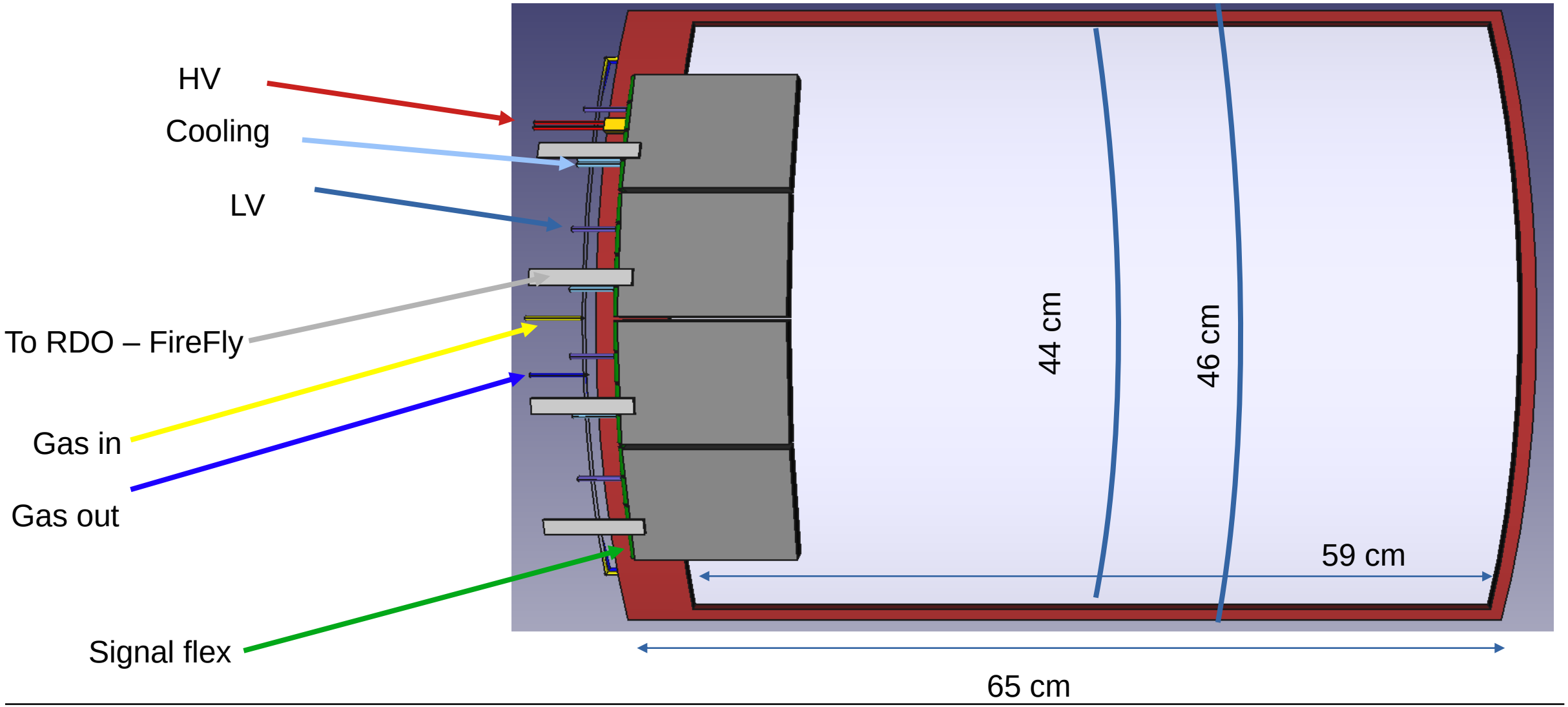
Summary

- Optical FEB-RDO link is considered as preferable
  - → No restriction on RDOs
  - → Easier to maintain
- FireFly optical components to be evaluated
  - → Power consumption @ 1 Gbit/s rate
  - → Radiation tolerance to be confirmed
- Powering of FEBs with DC-DC regulators to be followed
  - → Where to place them if bulky
    - e.g. place them in the option 1 or 2 locations instead of RDOs
- Cooling options need to be studied
- Follow developments on integrated FEB – RDO solution
  - → Power consumption, optical interface
    - Any gain in power and cost with Spartan US+ versus Artix US+ ?
  - → If feasible for MPGDs – try to adapt
- Need a close collaboration between the MPGD teams and the ePIC integration team

Backup

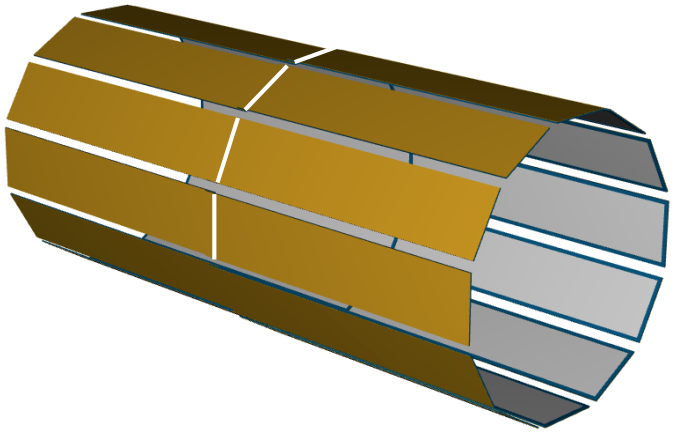
CyMBaL – Module

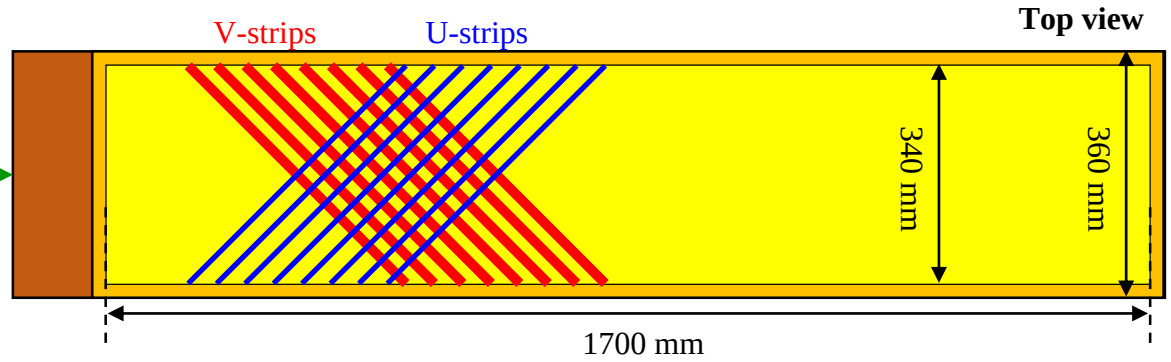
Charge 3

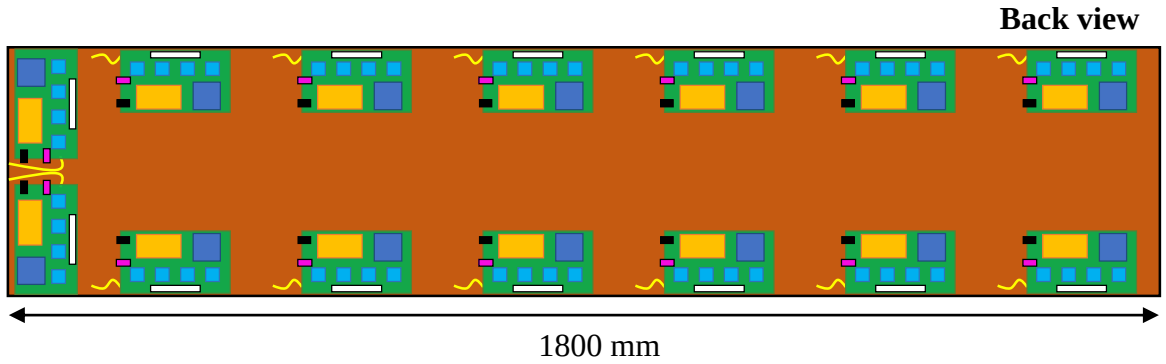


µRWELL-BOT Module:

Charge 2,3





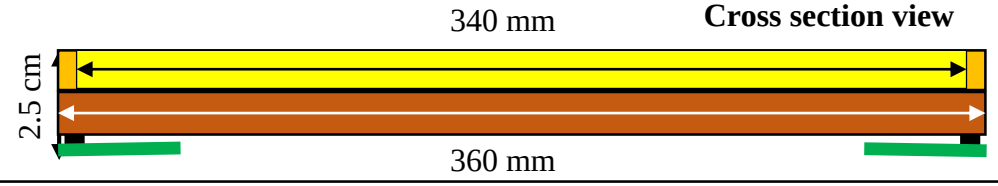


µRWELL-BOT module

- Thin-gap (1-mm drift) hybrid amplification GEM-µRWELL detector
- Capacitive-sharing U-V strips readout layers(45^{O} stereo angle)
- Pitch: 1.14 mm (1790 U-strips and 1790 V-strips per modules)

On-detector Front End Boards (FEBs) based on SALSA chips

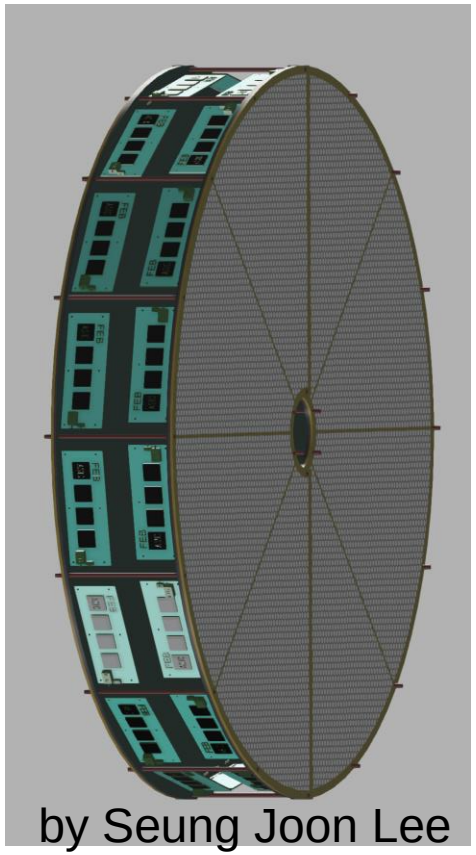
- 14 FEB / modules (assuming 4 SALSA chips i.e 256 e-ch / FEB)
- Direct connection on the back of the modules (no need for flex cables)



Detector, Electronics Readout, and Services

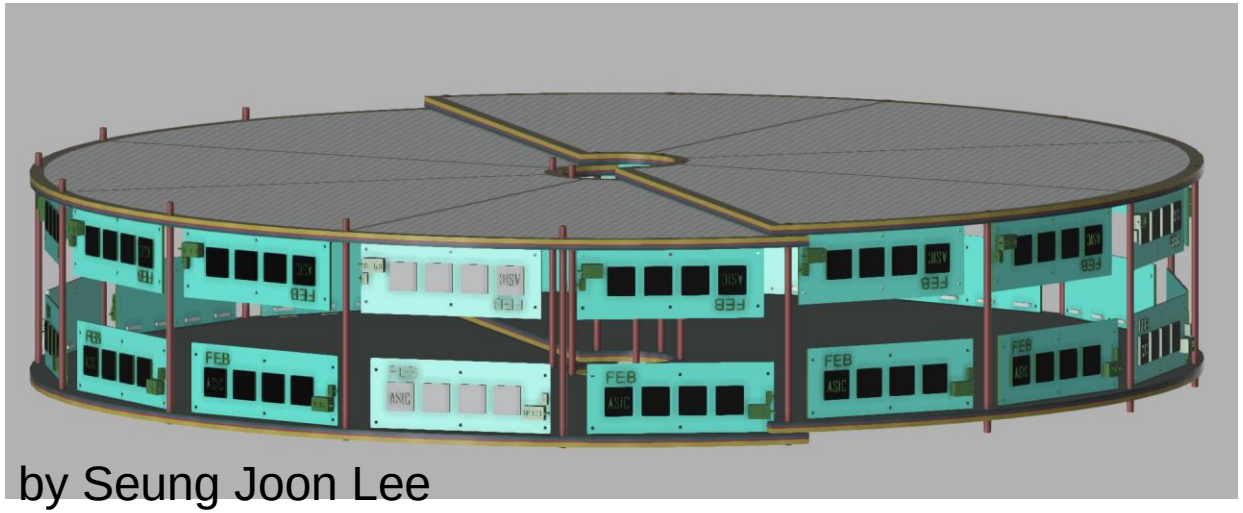
Charge 3

Are the current designs and plans for detector, electronics readout, and services sufficiently developed to achieve the performance requirements?



by Seung Joon Lee

MPGD Endcaps configuration



by Seung Joon Lee

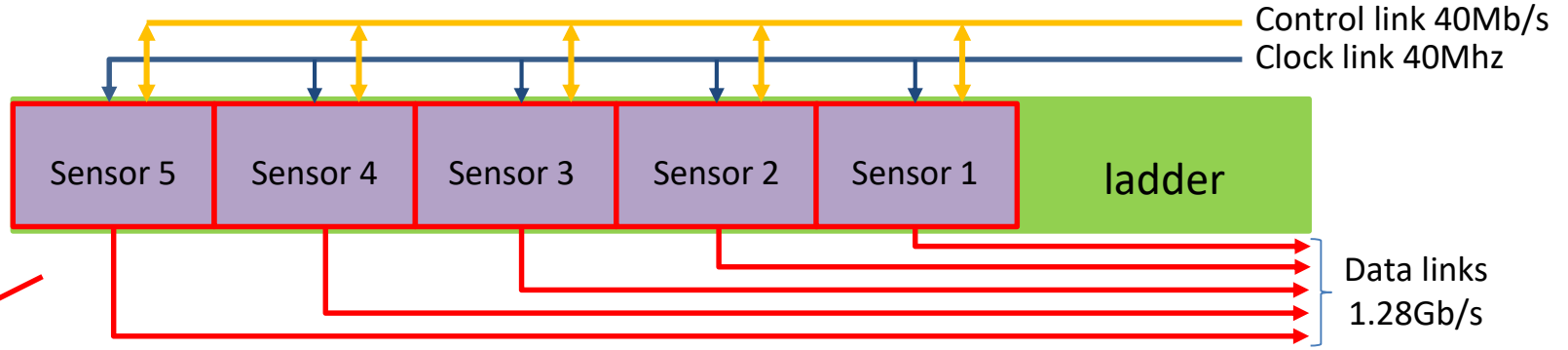
- The two disks are mounted facing each another
- The FEBs are connected perpendicularly to the disks and will not overlap the active area

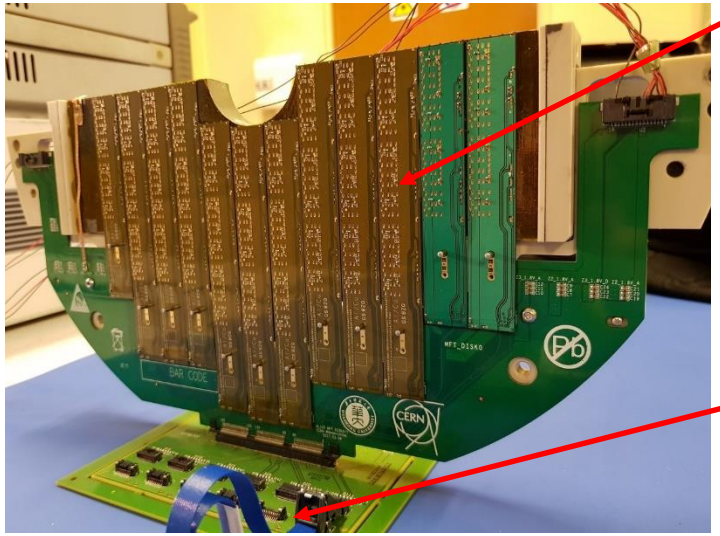
Twinax copper cable performance example: Alice MFT

- Muon Forward Tracker: ladders with a variable number of ALPIDE silicon sensors

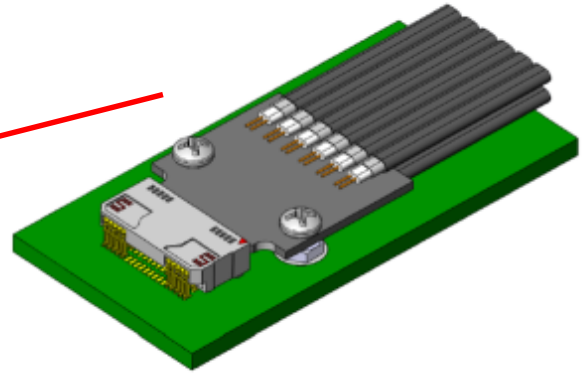
→ ALPIDE sensor: 512K pixels

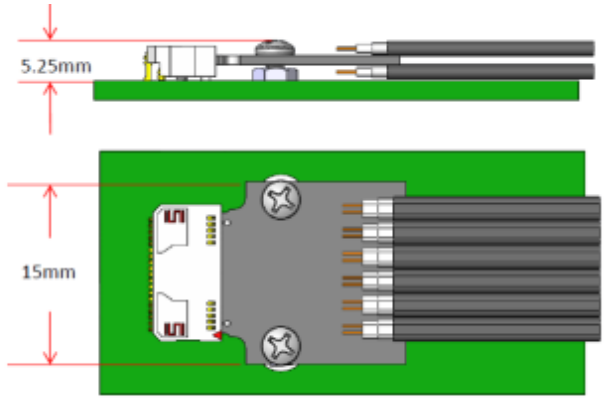
- Pixel = 29 x 27 μm^2
- ZS, triggered or continuous
- 1.28 Gbit/s upstream data link
  - Pre-emphasis capability
- 40 MHz clock
- 40 Mb/s control





Samtec 12-ribbon FireFly twinax cables with low profile connectors





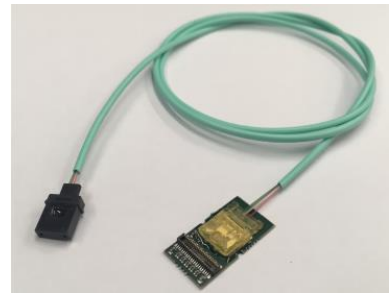
→ Signal integrity studies

- Up to 8m of cable and 9 connectors in the path
- Reliable communication with BER better than 10^{-14}
  - Adjust pre-emphasis

FEB with optical interface: VTRX+

- FE ASICs are directly interfaced to VTRX+
  - → Downlink with embedded clock / sync / async data distributed with high fidelity fan-out
  - → Requires an “innovative” ASIC interface
    - Working on CDR circuitry for Salsa

CERN VTRX+

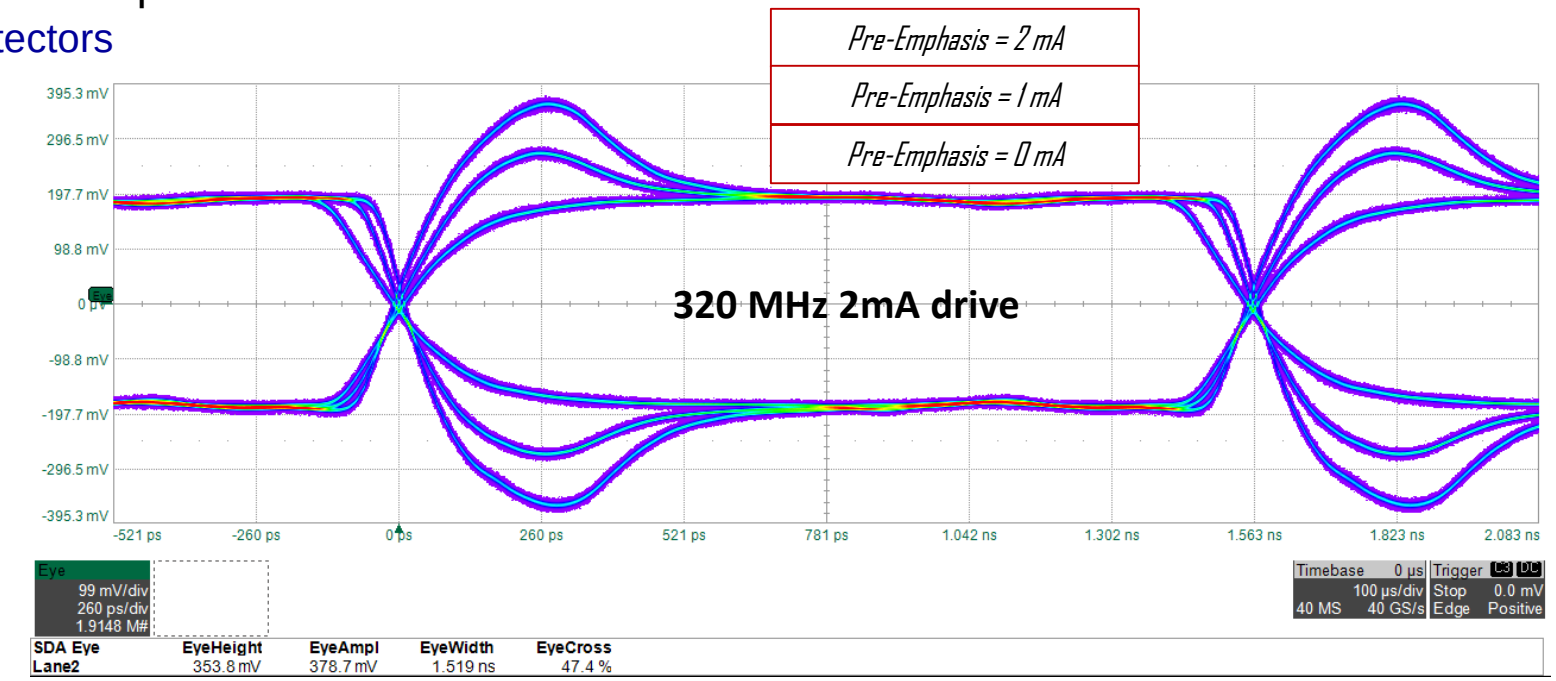


- FEB
  - → Radiation hardened ASICs
  - → Minimal power consumption after electrical interface option: only VTRX+ consumption added
    - ~ 32-35 mW / channel - 8% increase compared to a FEB with electrical RDO interface
    - 0.9 mm^2 (DC/DC + LDO) or 5.8 mm^2 (LDO only) wires to FEB
- RDO : common hardware

Common practices to improve signal integrity on long transmission lines

- Drive strength choice of differential lines:
  - → 1 mA, 2mA, 4mA, 8mA
- Pre-emphasis strength and duration:
  - → 1 mA, 2mA
  - → 150 ps, 300ps
- Rafael clock/command fan-out example (more in backup and
  - → 130 nm 3-to-1-to-13 radiation hard chip
    - Developed for CMS timing detectors
  - → 1.2 V
  - → CLPS differential
    - CERN low power
    - 200 mV, 400 mV diff swing
  - → Measurements over 2 m cable
    - Coaxial SMAs
  - → Additive jitter ~2 ps
    - Specs up to 400 MHz
    - Satisfies 640 MHz
    - Decent at 1.28 GHz
  - → Irradiation tests
    - 6 m SMA cables
    - 200 Mbit/s

Rafael

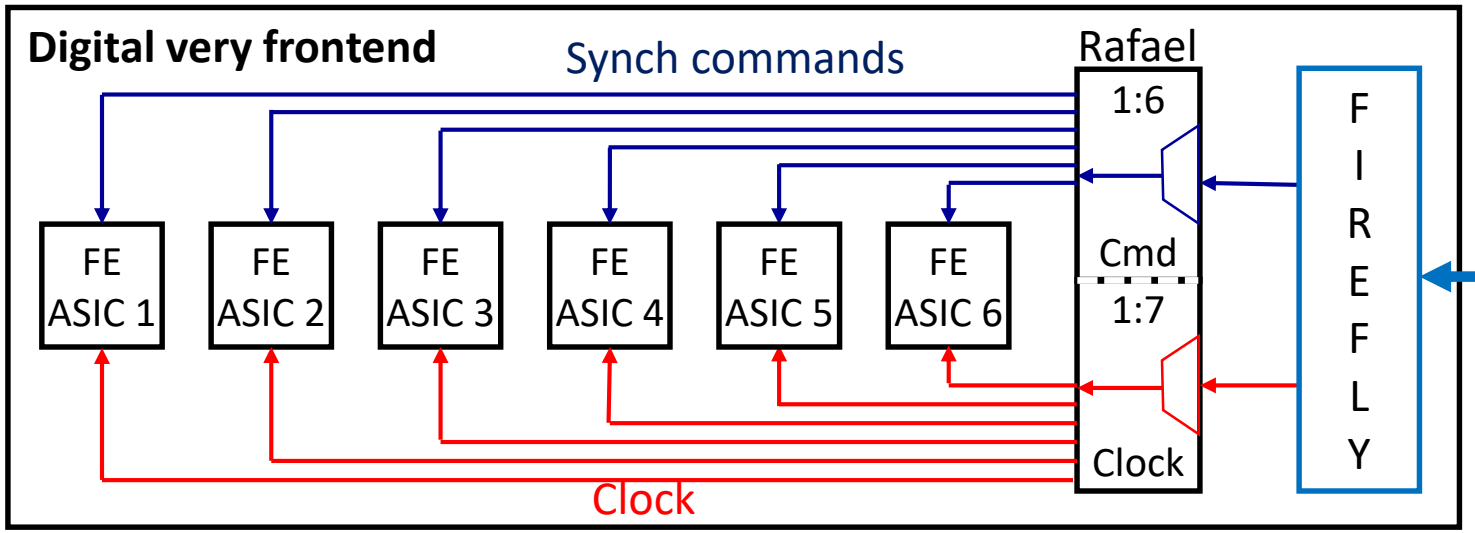


Modern FPGA receivers equipped with circuitry to determine optimal sampling point

Error detection and correction sequences improve further BER figures

Clock and fast command distribution example

- Rafael - Radiation-hArd Fan-out ASIC for Experiments at LHC - developed at Irfu, CEA Saclay
  - → 3 inputs and 13 outputs
  - → CLPS signaling
    - CM voltage: 0.6 V
    - Differential swing: 200-400 mV
    - Programmable drive and emphasis
  - → Single buffer: any input to 13 outputs
  - → Double buffer
    - Input 1 to 6 outputs
    - Input 2 to 7 outputs
  - → Up to 400 MHz and beyond
  - → Low additive jitter of < 2 ps
  - → LHC-level TID, neutron, SEU
  - → 130 nm technology
  - → Possibility to embed a PLL
    - If no jitter cleaner PLL in ASICs



- Commercial counterparts
  - → IDT 8P34S2108: https://www.renesas.com/eu/en/document/dst/8p34s2108-datasheet
  - → TI CDCLVD1216: http://www.ti.com/lit/ds/symlink/cdclvd1216.pdf

Long distance electrical links with Rafael drivers

- Low jitter transmission over 3-4 m coaxial cables
  - → Adjust drive strength between 1 mA and 2 mA
  - → Adjust pre-emphasis strength : 0 mA (none), 1 mA, 2 mA
  - → Adjust pre-emphasis duration : 160 ps, 320 ps, 480 ps

Example: Effect of pre-emphasis @ 320 MHz