



FTOF PB design

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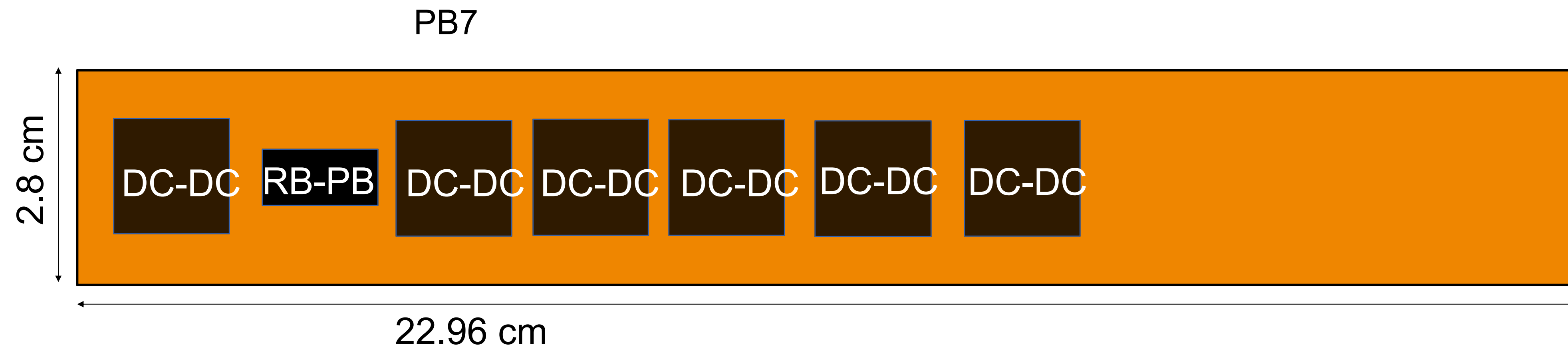
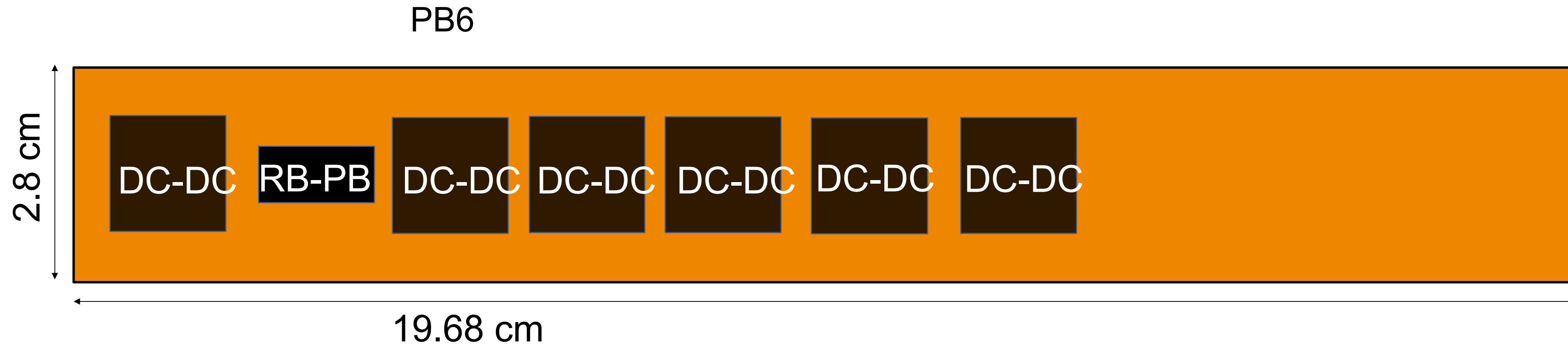
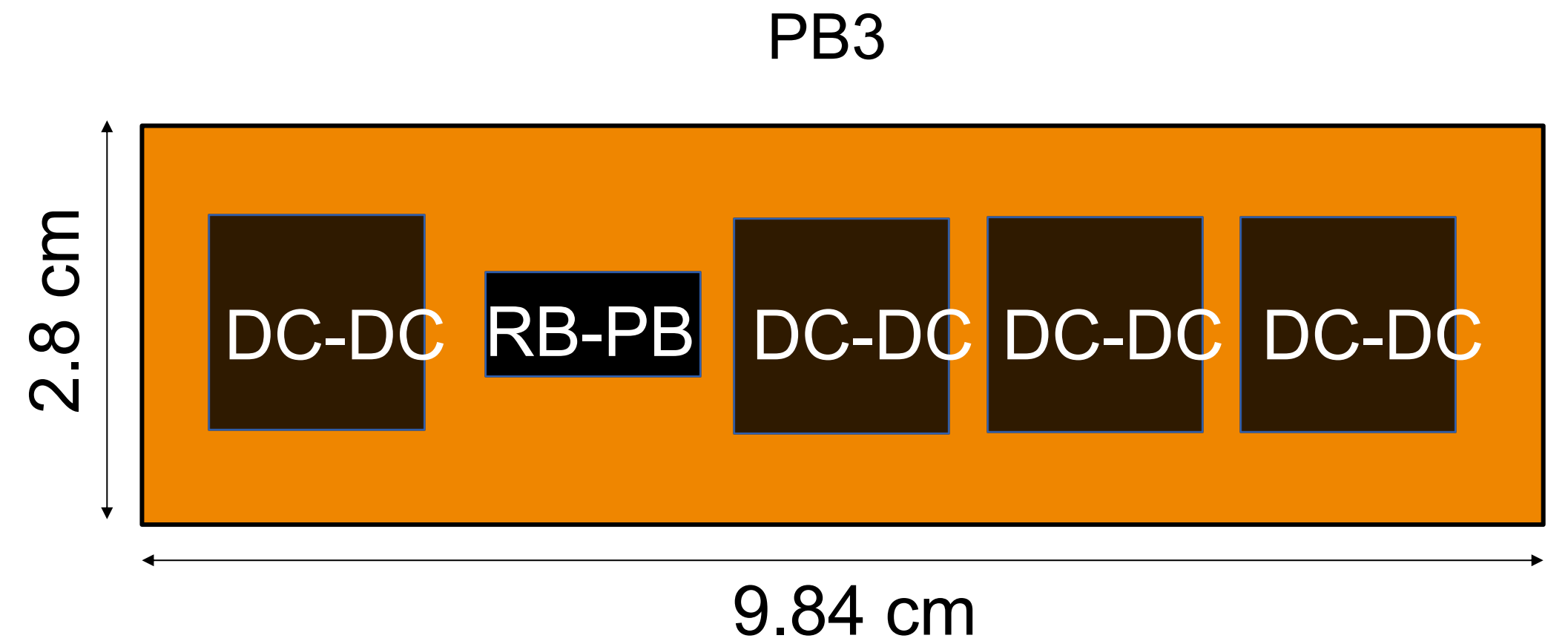
**ePIC TOF WP2 working meeting
June 21, 2024**

Electron-Ion Collider

Power board design

Assuming that we use bPOL48V with $I_{out} (max) = 10A$

Height should be $\leq 1cm$



Power board design

CERN has kindly agreed to provide us 5 bPOL48V chips for evaluation. Shipment to Rice is being arranged.

Ken Wyllie asked how many chips we need and whether we would like to include the order to the IpGPT and VTRx+ contract. This would need to be discussed with the EIC project (Fernando).

- Given that we still need time to evaluate this option, it is premature to decide on a production order, if it has to be made now. Would this be considered LLP?
- Is there any need from other subdetectors? TOF alone needs 2000-3000 chips

FTOF

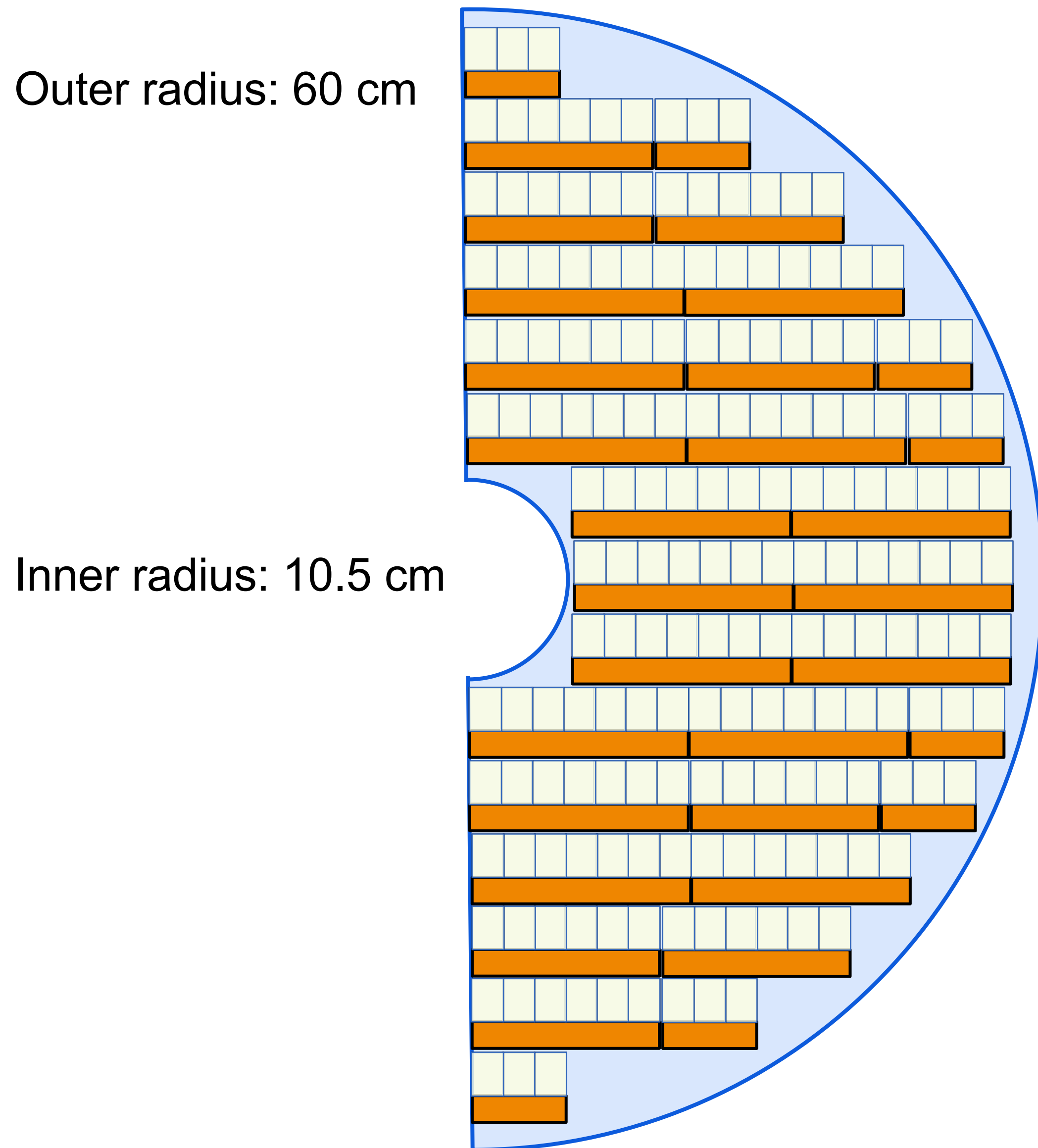
bPOL48V	RB3	RB6	RB7	All
3.3V	1	1	1	
1.8V	1	1	1	
1.2V	2	4	4	
<i>per PB</i>	4	6	6	
<i>FTOF total</i>	128	192	384	704

BTOF

bPOL48V	Stave (64 ASICs)
3.3V	1
1.8V	1
1.2V	8
<i>per PB</i>	10
<i>BTOF total</i>	1440

Backups

FTOF Layout (x-y view): Scenario 2

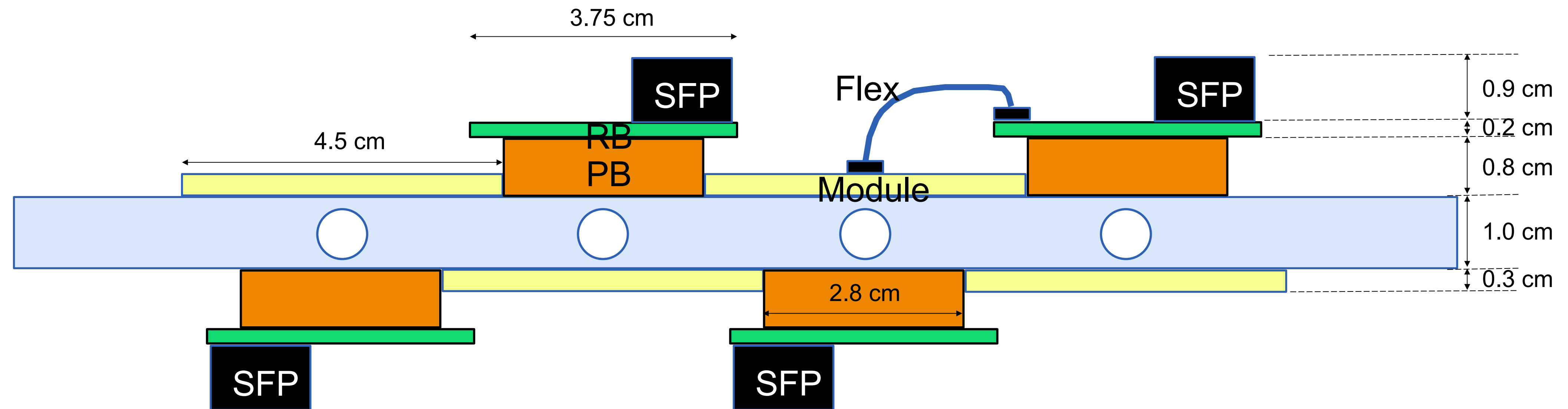


Row	modules	RB3	RB6	RB7	All RBs
1	3	1	0	0	1
2	9	1	1	0	2
3	12	0	2	0	2
4	14	0	0	2	2
5	16	1	1	1	3
6	17	1	0	2	3
7	14	0	0	2	2
8	14	0	0	2	2
9	14	0	0	2	2
10	17	1	0	2	3
11	16	1	1	1	3
12	14	0	0	2	2
13	12	0	2	0	2
14	9	1	1	0	2
15	3	1	0	0	1
Sum	184	8	8	16	32

Total number of modules: $184 \times 4 = 736$

Total number of service hybrids: $32 \times 4 = 128$

FTOF layout (cross section view)



Z thickness requirement:

- At least 7.5 cm
- Can be reduced to 5cm if SFP is replaced by VTRx+