Timing scan data analysis
—Analysis—

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Steps

1. Making a list of runs ✓
2. Processing those runs ✓
    i. Decoding ✓
    ii. Hot channel analysis ✓
    iii. Hot channel removal ✓
3. Run-by-run analysis (InttRawHit without hot channel removal is OK)
    i. Peak finding, plateau finding
    ii. Peak position comparison over all FPHX chips ←
    iii. Peak height estimation
4. Analysis using runs
    i. Comparison of peak position alignment over runs
    ii. Comparison of peak height over runs
5. Repeating steps 3 and 4 with hot channel removal
6. Repeating step 6 with more sophisticated hit selection
    1. ADC cut
    2. MIP selection using INTT tracking
7. and…?

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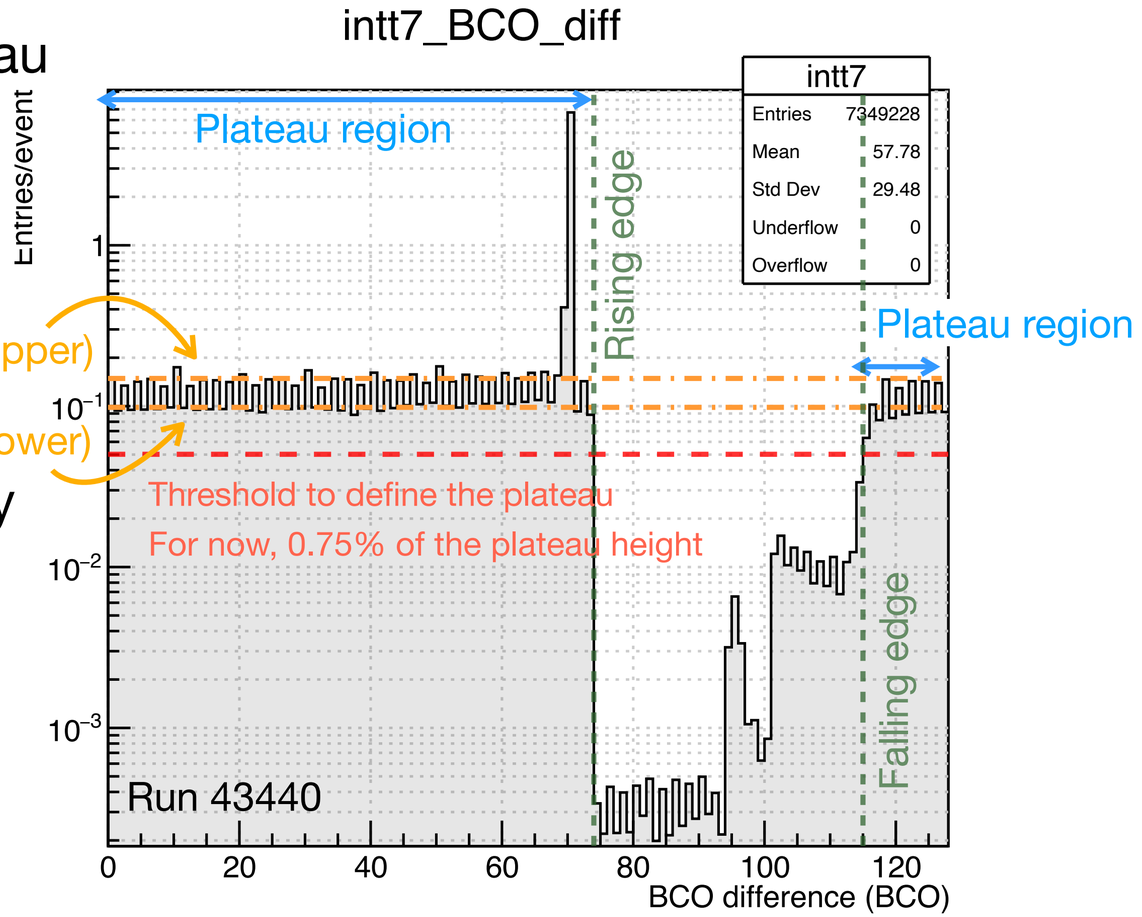
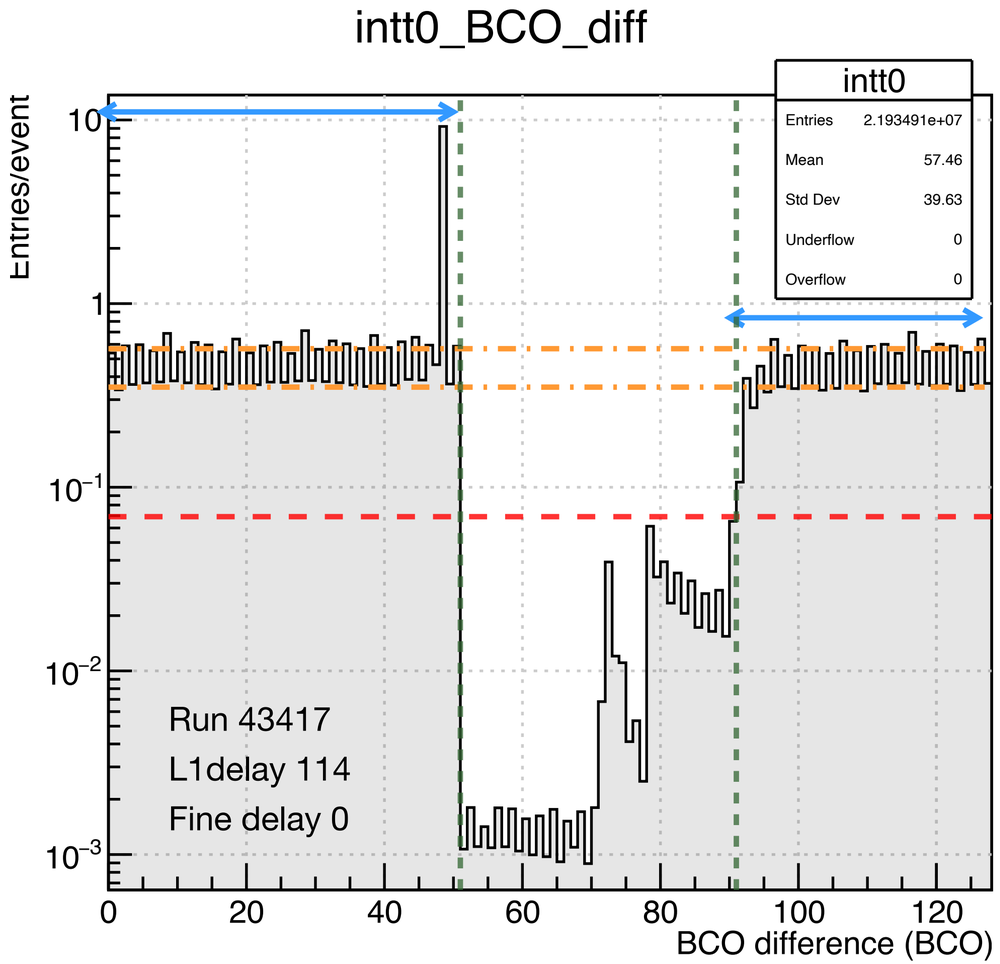
Analysis

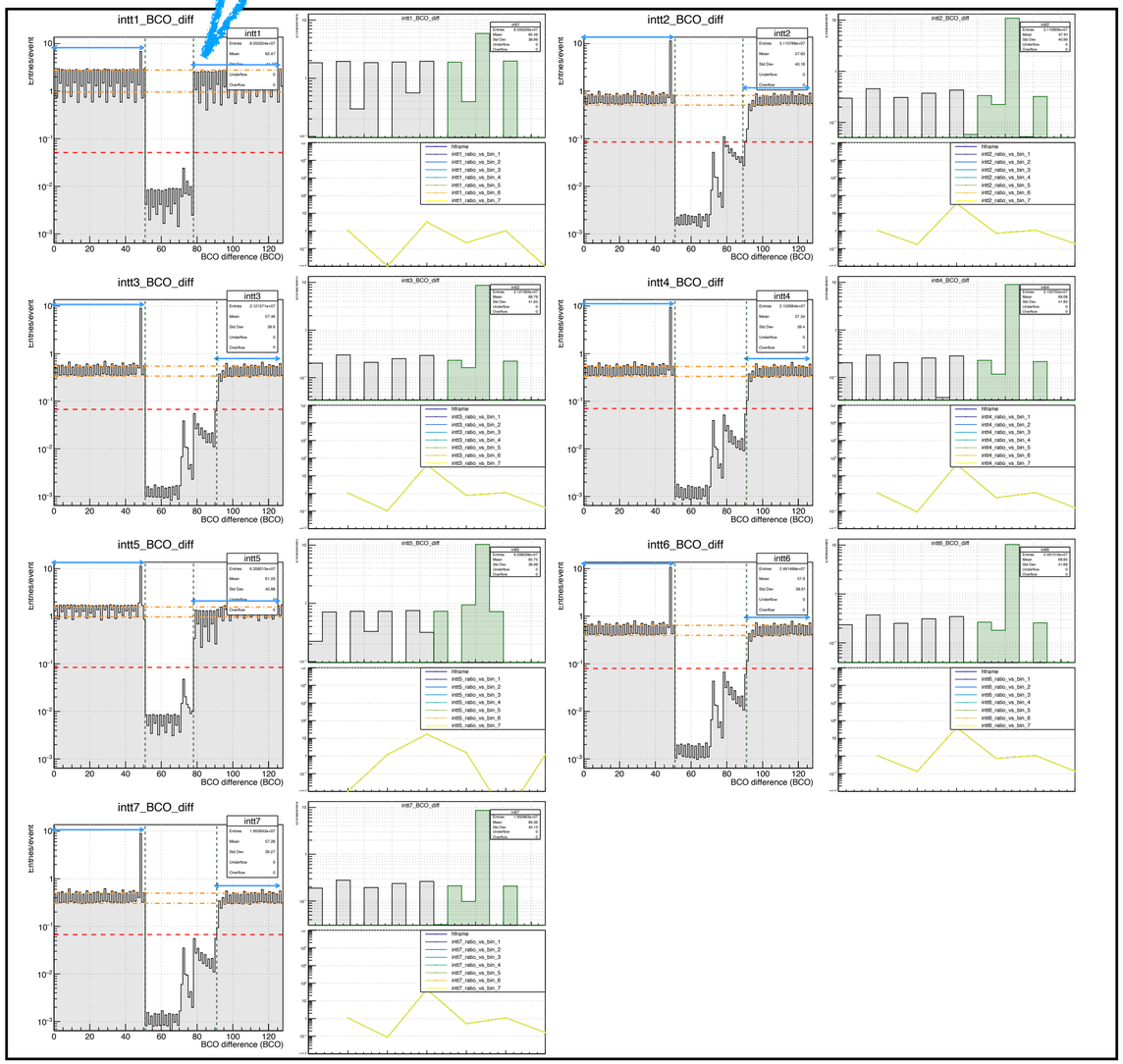
- InttRawHit is used, i.e., no hot channel rejection.
- Checking the alignment of the trigger event timing is good to begin with.

- First of all, the peak of the triggered event and plateau in the BCO diff dist need to be defined.
- The peak definition is simple: the highest bin.
- A threshold was introduced to define the plateau region.
- The height of the plateau was estimated using even or odd bins because the bumpy structure was made by the beam bunch fill pattern.
- The rising and falling edges were also defined.



Analysis: Peak position

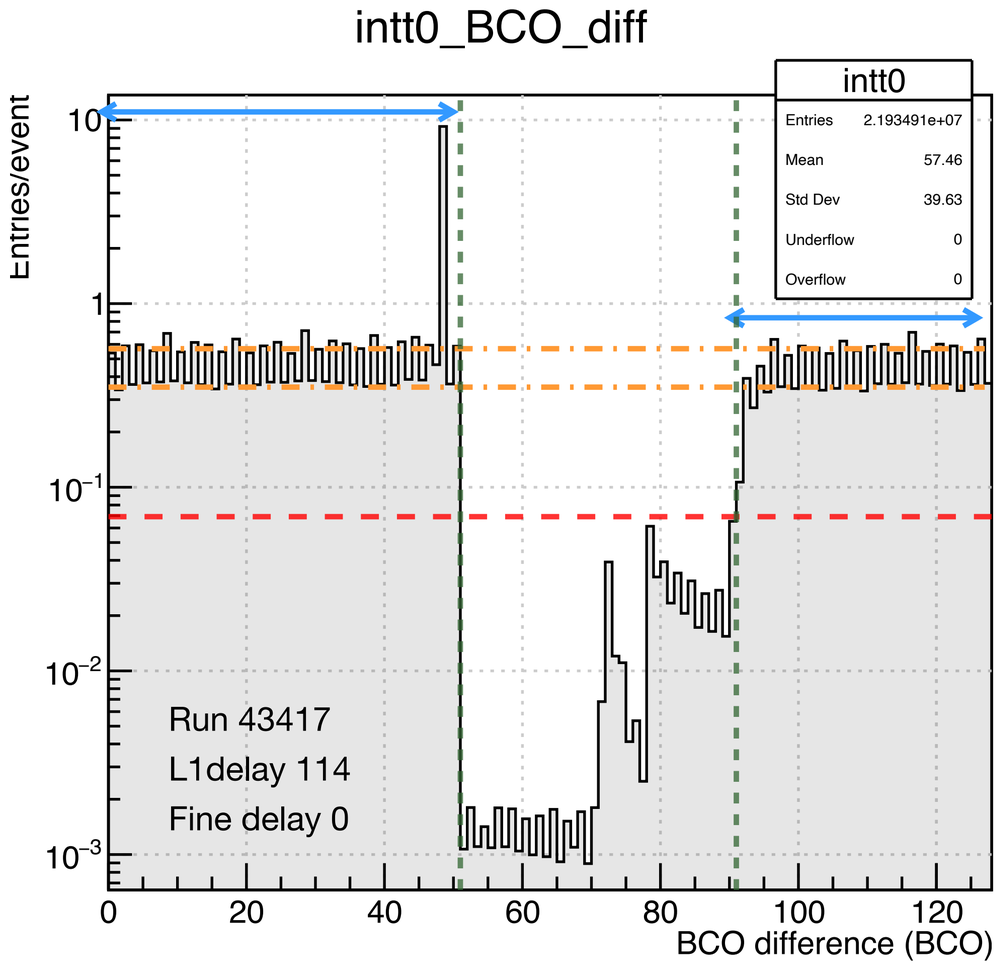


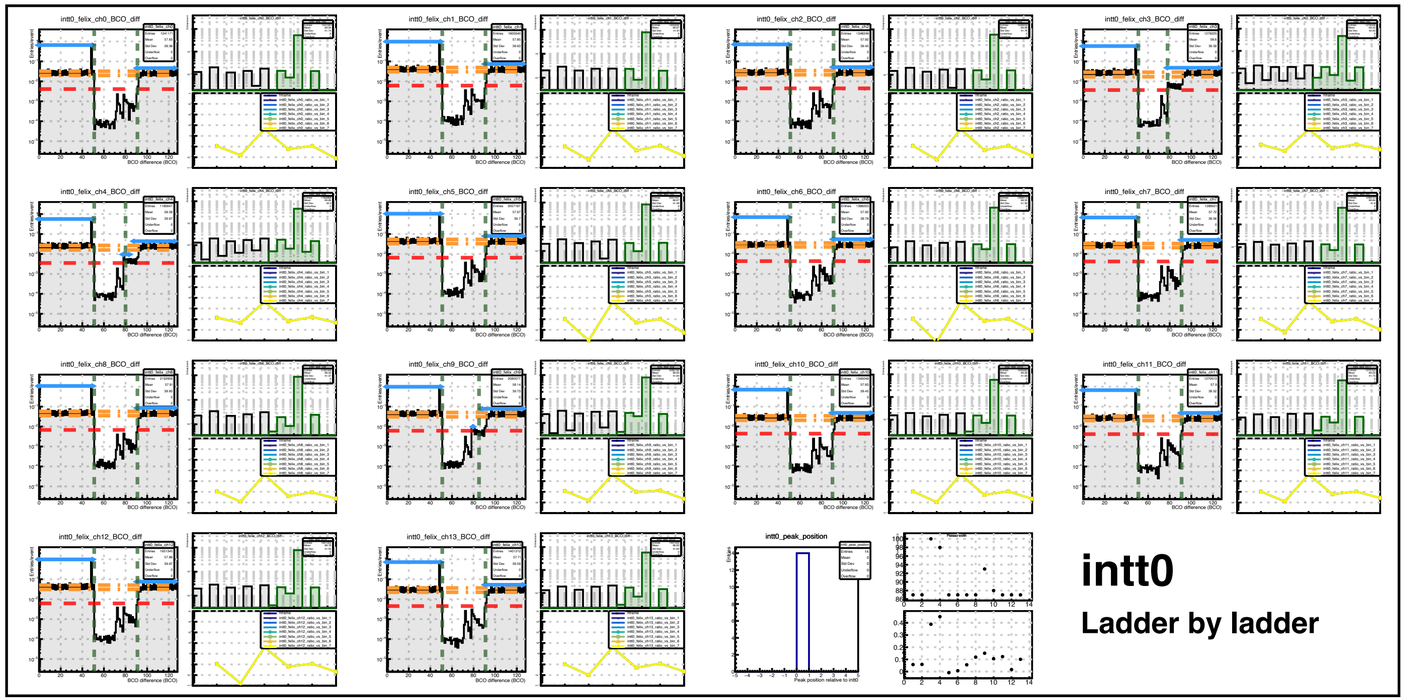


Hot channel makes such a strange structure. I already confirmed that the hot channel rejection solves it.

FELIX by FELIX plots

Analysis: Peak position

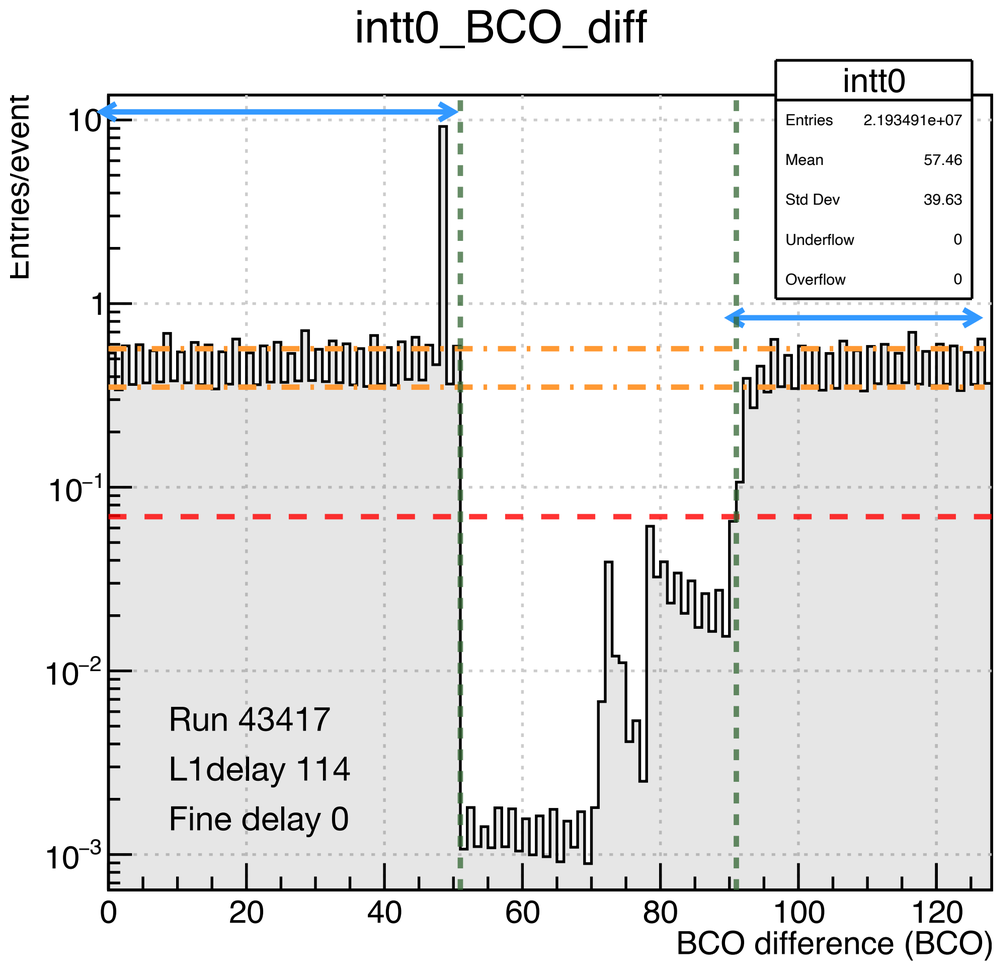


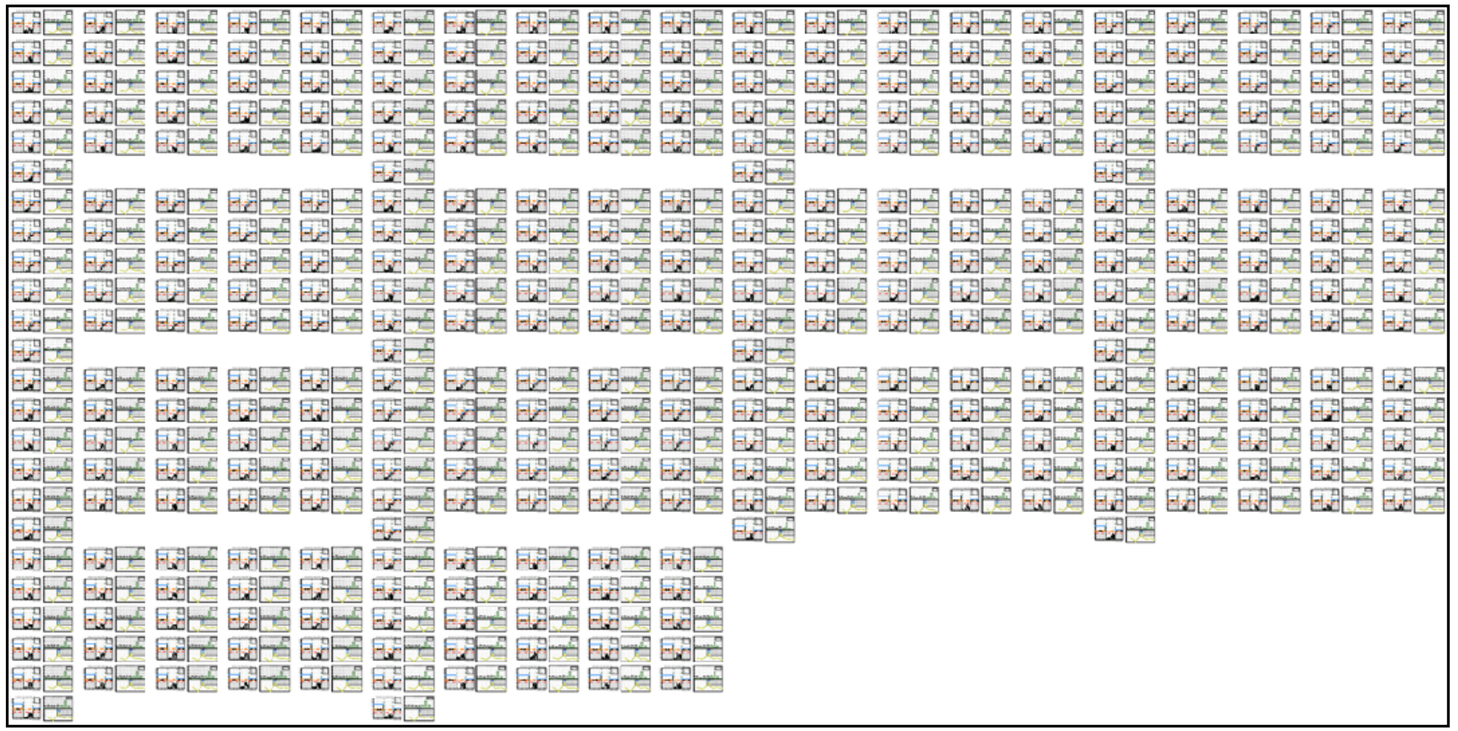


FELIX by FELIX plots

Ladder by ladder plots of intt0

Analysis: Peak position

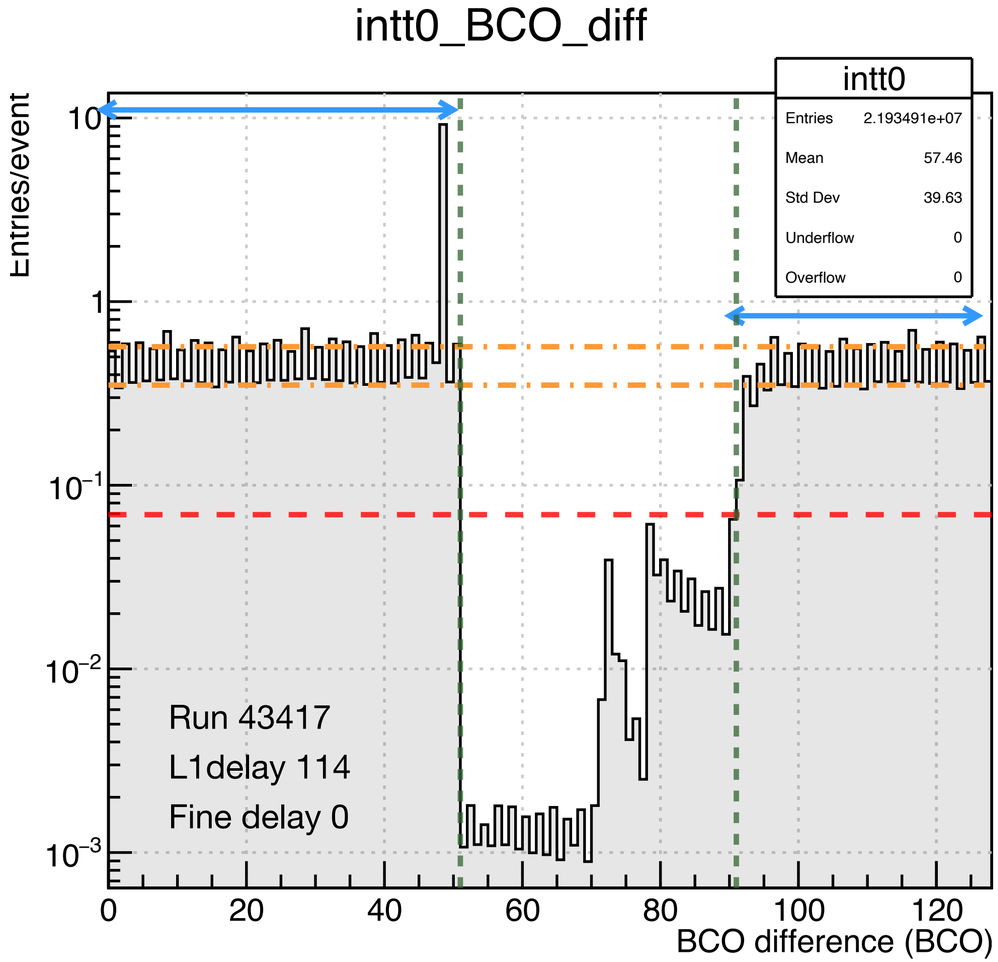


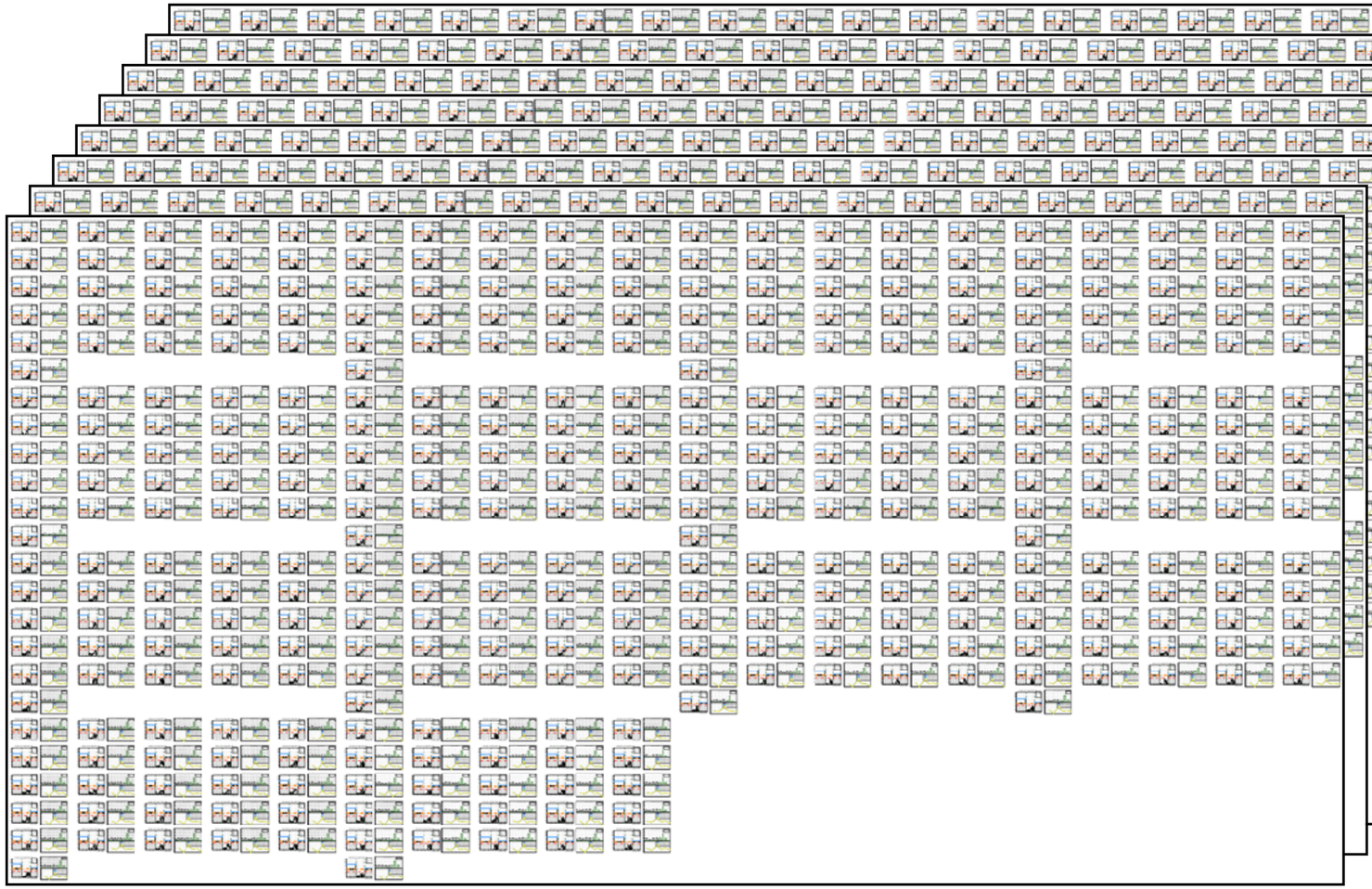


FELIX by FELIX plots

Chip by chip of intt0

Analysis: Peak position

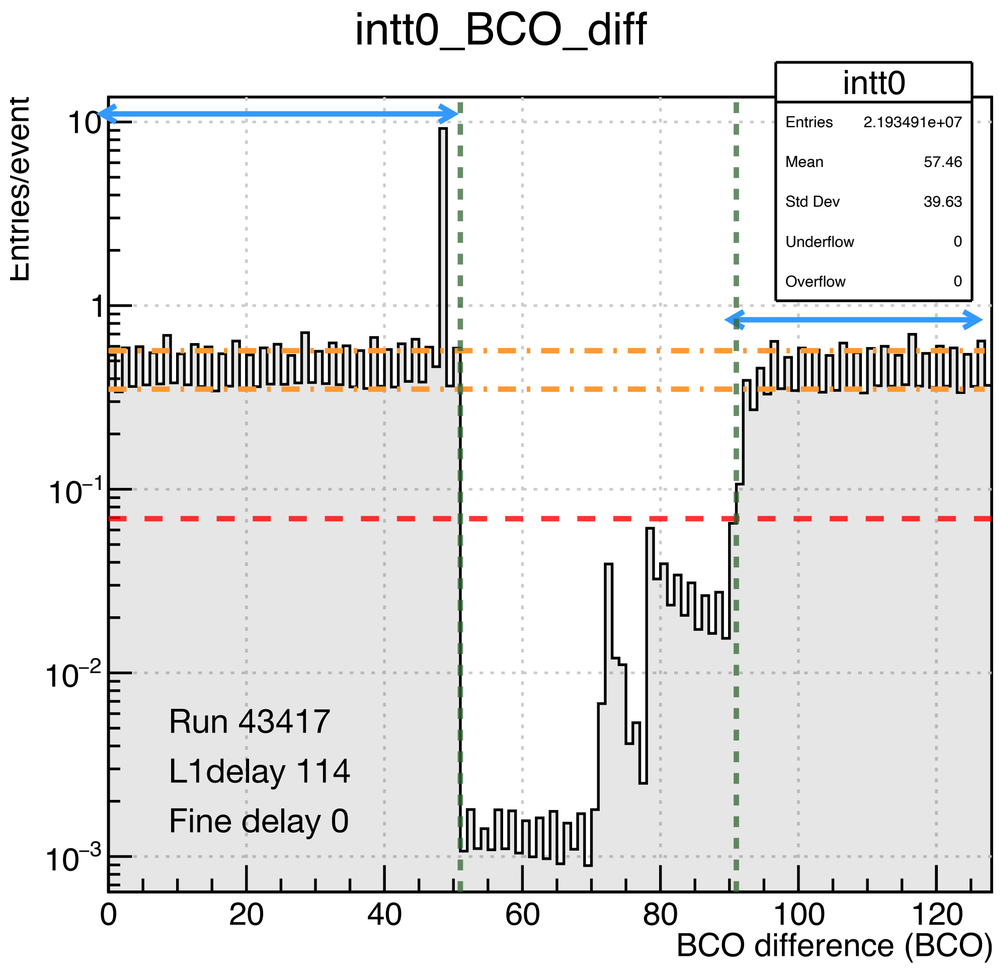


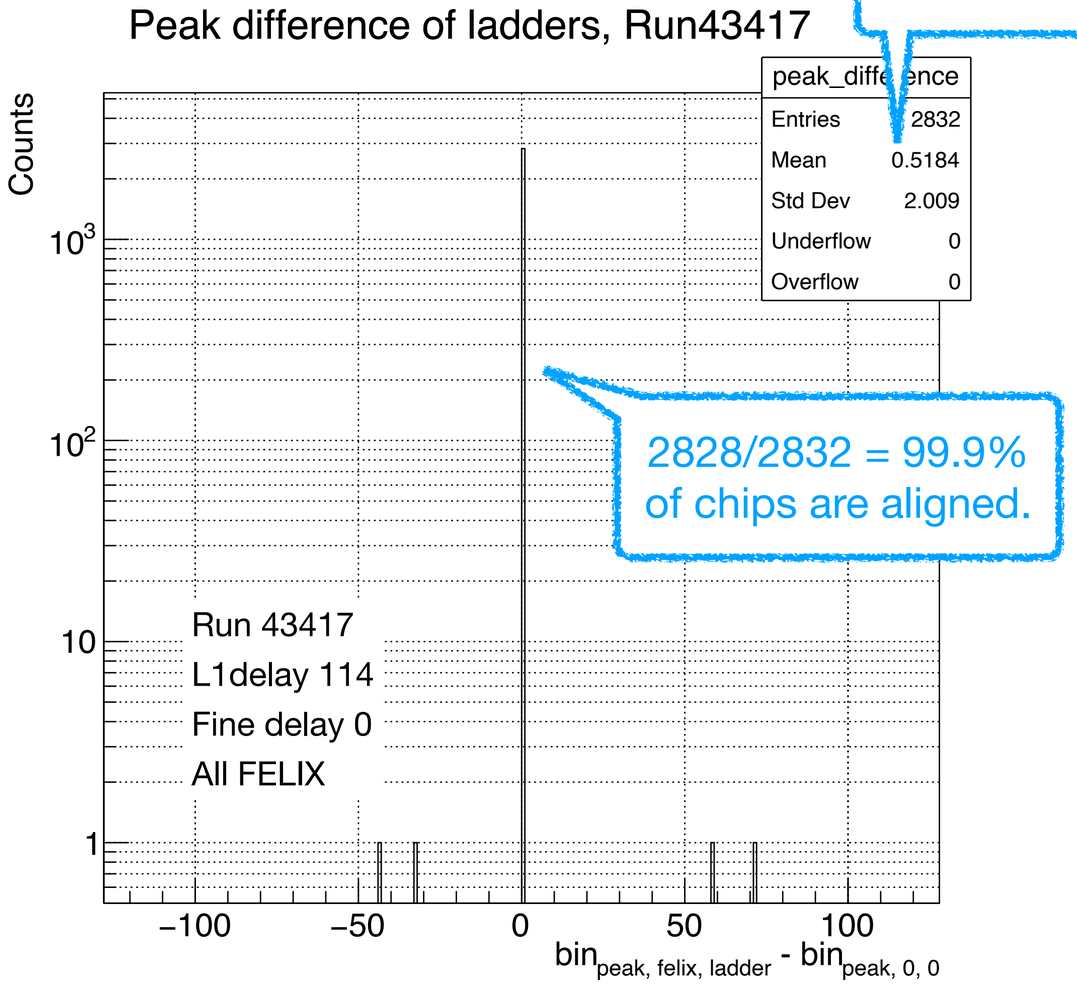


FELIX by FELIX plots

Chip by chip of all

Analysis: Peak position





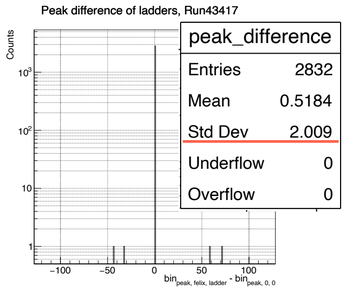
Offset 0.5 exists due to the nature of ROOT histogram

2828/2832 = 99.9% of chips are aligned.

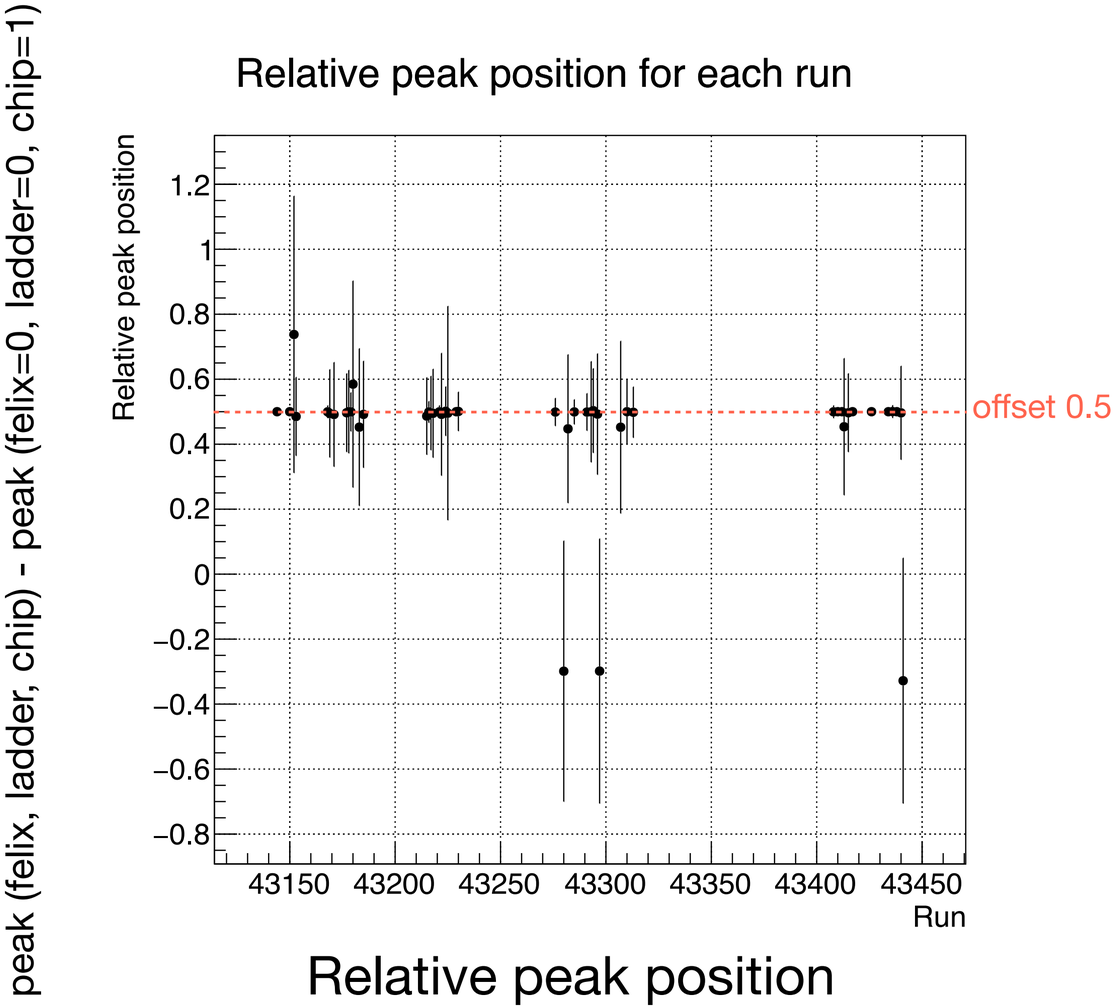
peak (felix, ladder, chip) - peak (felix=0, ladder=0, chip=1)

FELIX by FELIX plots

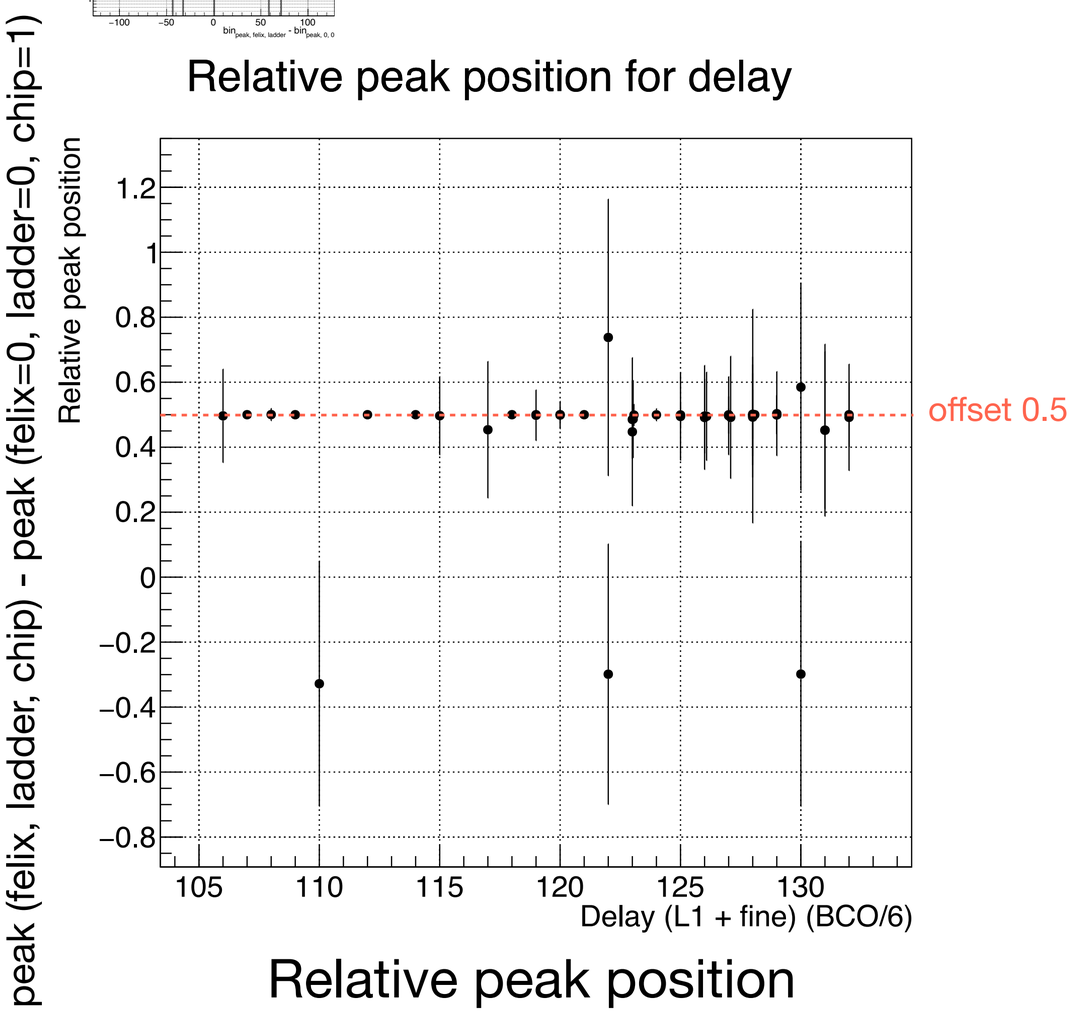
Analysis: Peak position



Error bars in y come from the std. dev. of for the range -5 — +5 of the peak position dists. It's not so good idea, I think.

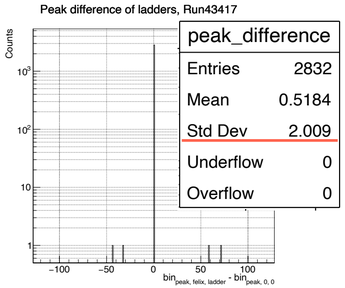


Relative peak position
as a function of run

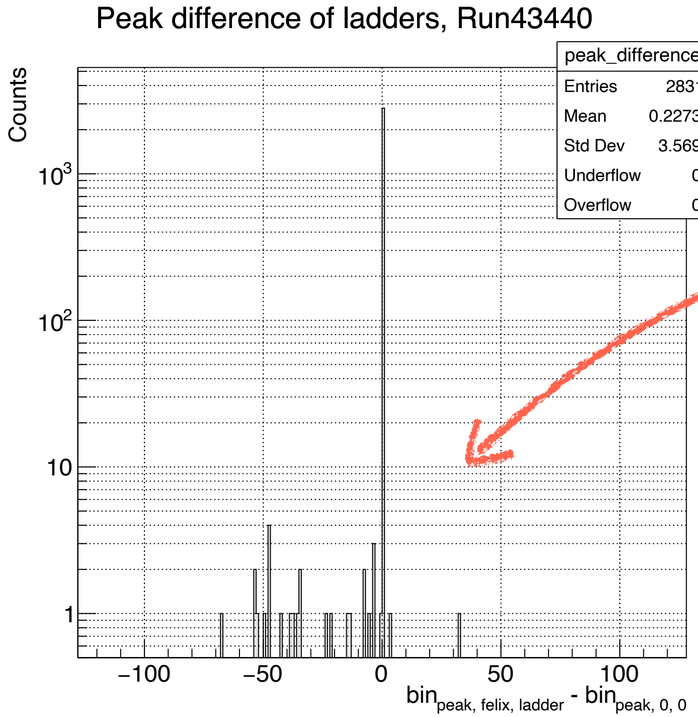


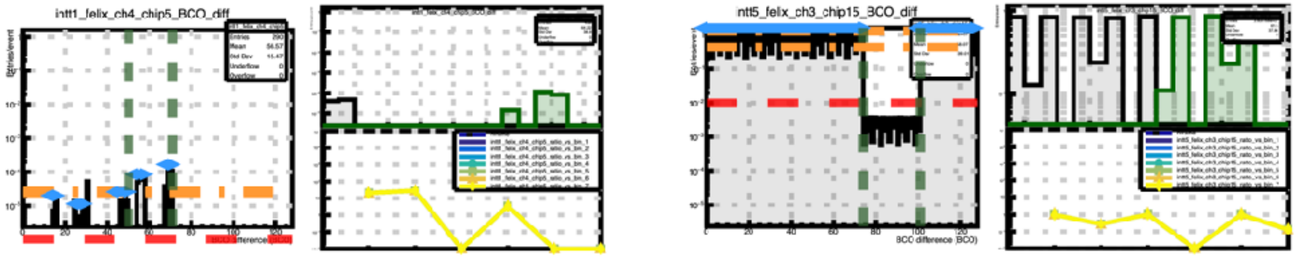
Relative peak position
as a function of delay value

Analysis: Peak position



Error bars in y come from the std. dev. of for the range -5 — +5 of the peak position dists. It's not so good idea, I think.





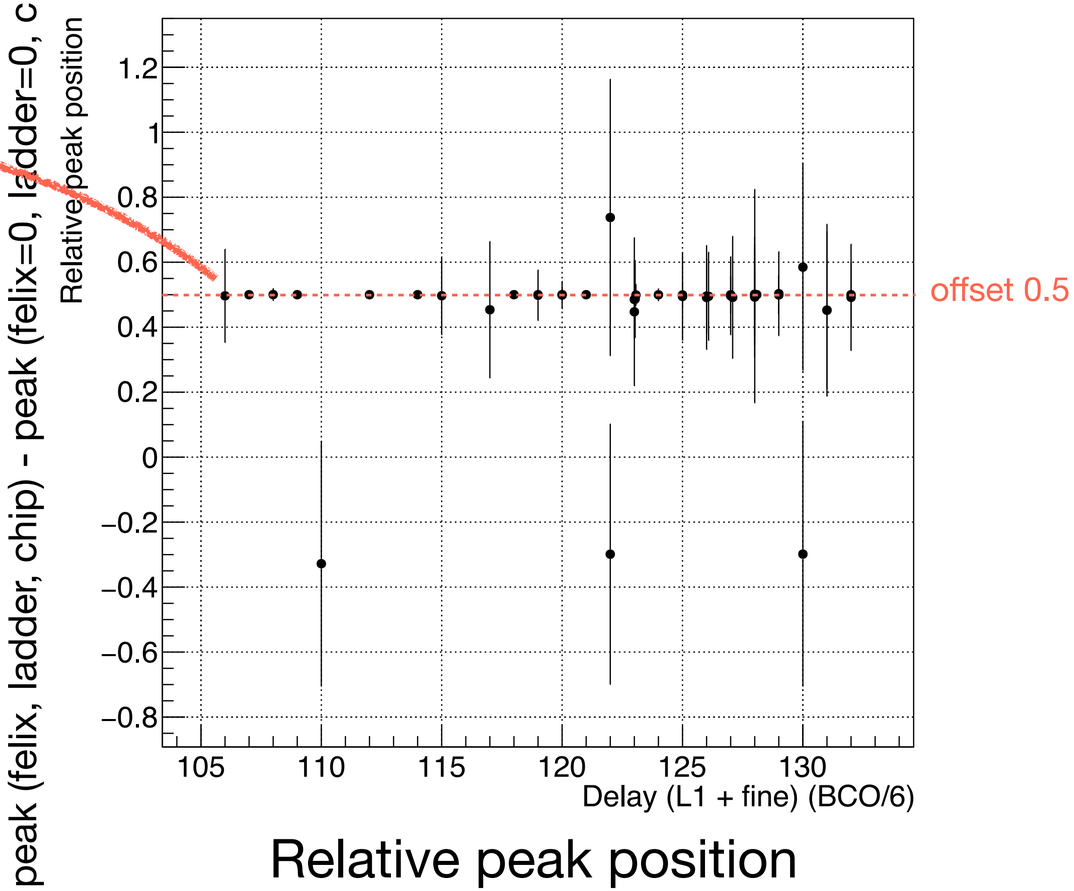
intt1, ladder4, chip5, difference -1

Data of intt1 was generally bad at that time. It's good to remove intt1 from the analysis.

intt5, ladder3, chip15, difference -35

The peak cannot be found. It happens from time to time.

Relative peak position for delay

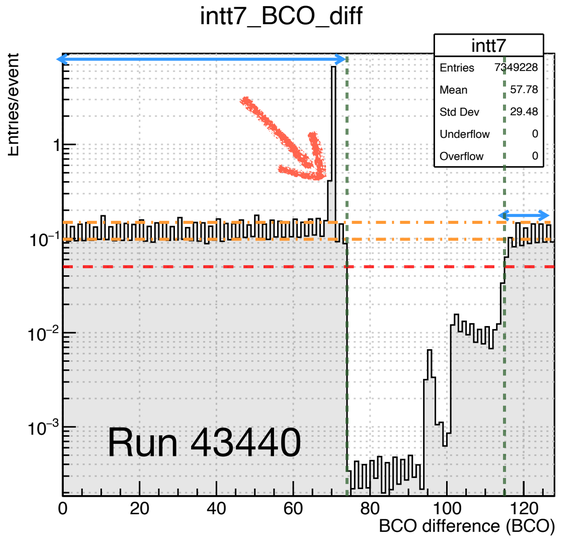


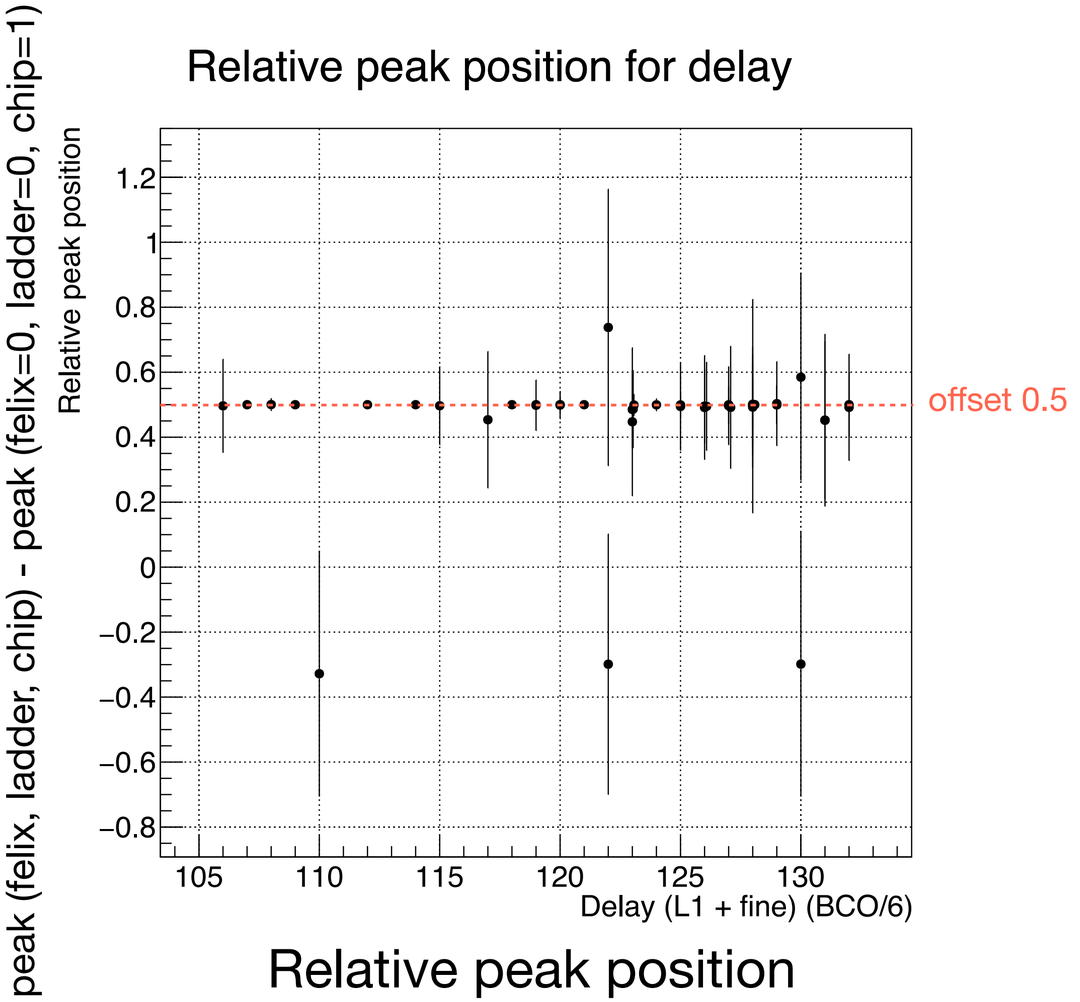
Relative peak position as a function of delay value

Summary

- Alignment of the peak position was checked at the level of FPHX chips.
- They are basically aligned well. Sometimes, the data of some chips is not reliable.
- Data selections are needed to make the situation clearer. Data of intt1 may not be analyzed.
- Peak alignment may not depend on the delay parameter even if INTT was not timed in within a 1 BCO, i.e. when it's bad, all chips are bad.

- The next step is to estimate "how nicely aligned".
  The next bin of the peak will be used.





Relative peak position
as a function of delay value