AC-LGAD TOF

Satoshi Yano (Hiroshima University)

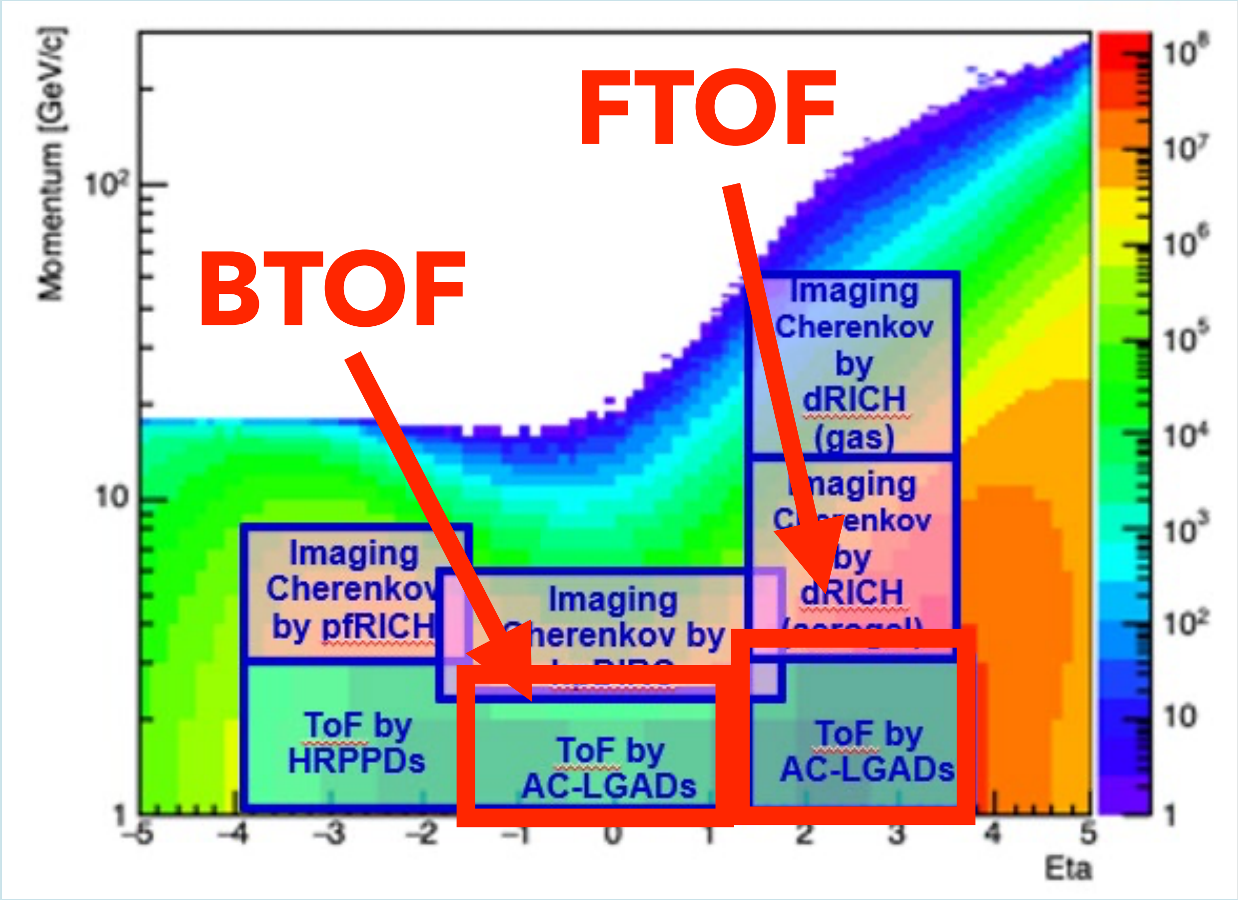
ePIC Collaboration meeting @ Rehigh University

07/25/2024

Role of the TOF in the ePIC project

- BTOF covers midrapidity and FTOF covers forward rapidity
  - BTOF and FTOF cover $-1.42<\eta<1.77$ and $1.86<\eta<3.85$, respectively

Detectors for PID



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  - Tracking with excellent spatial resolution
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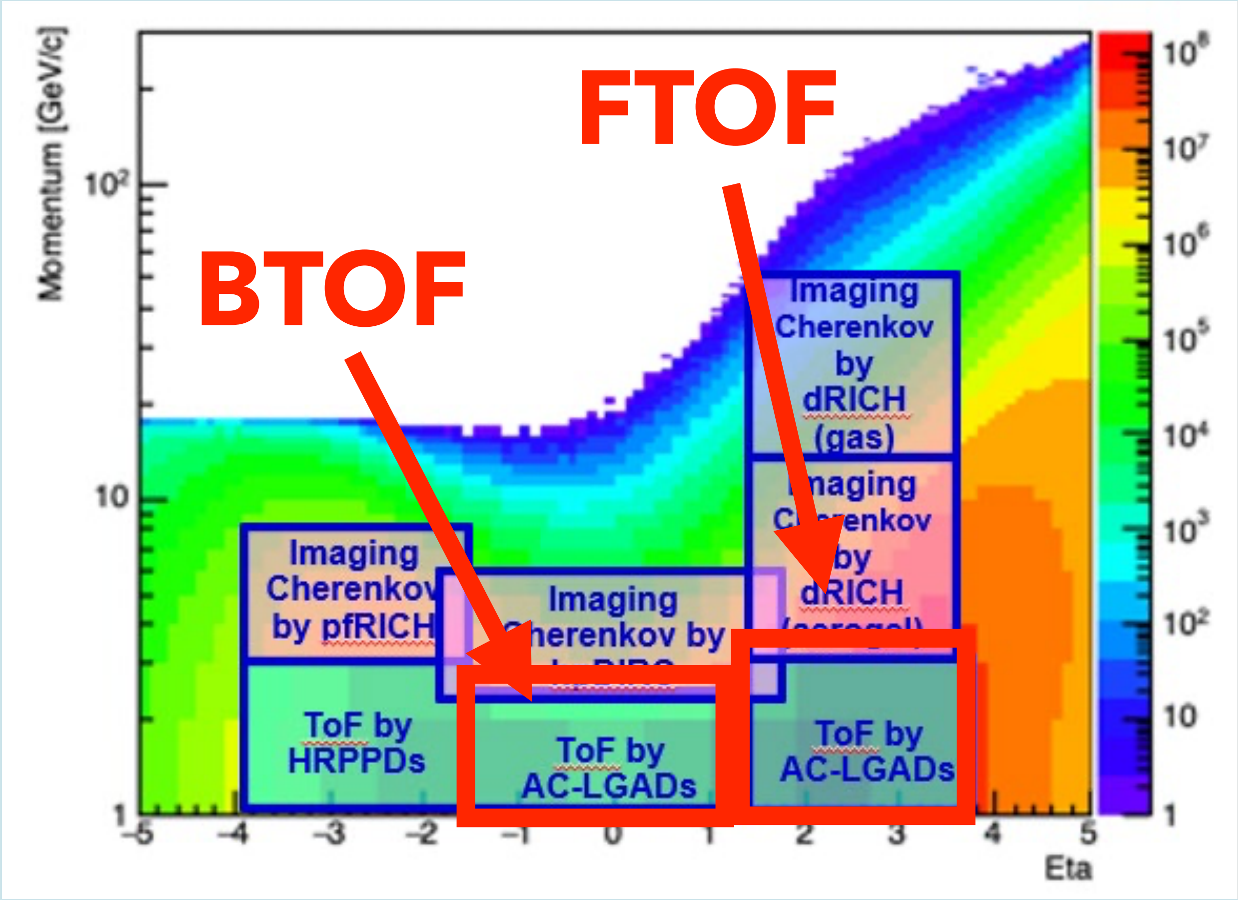
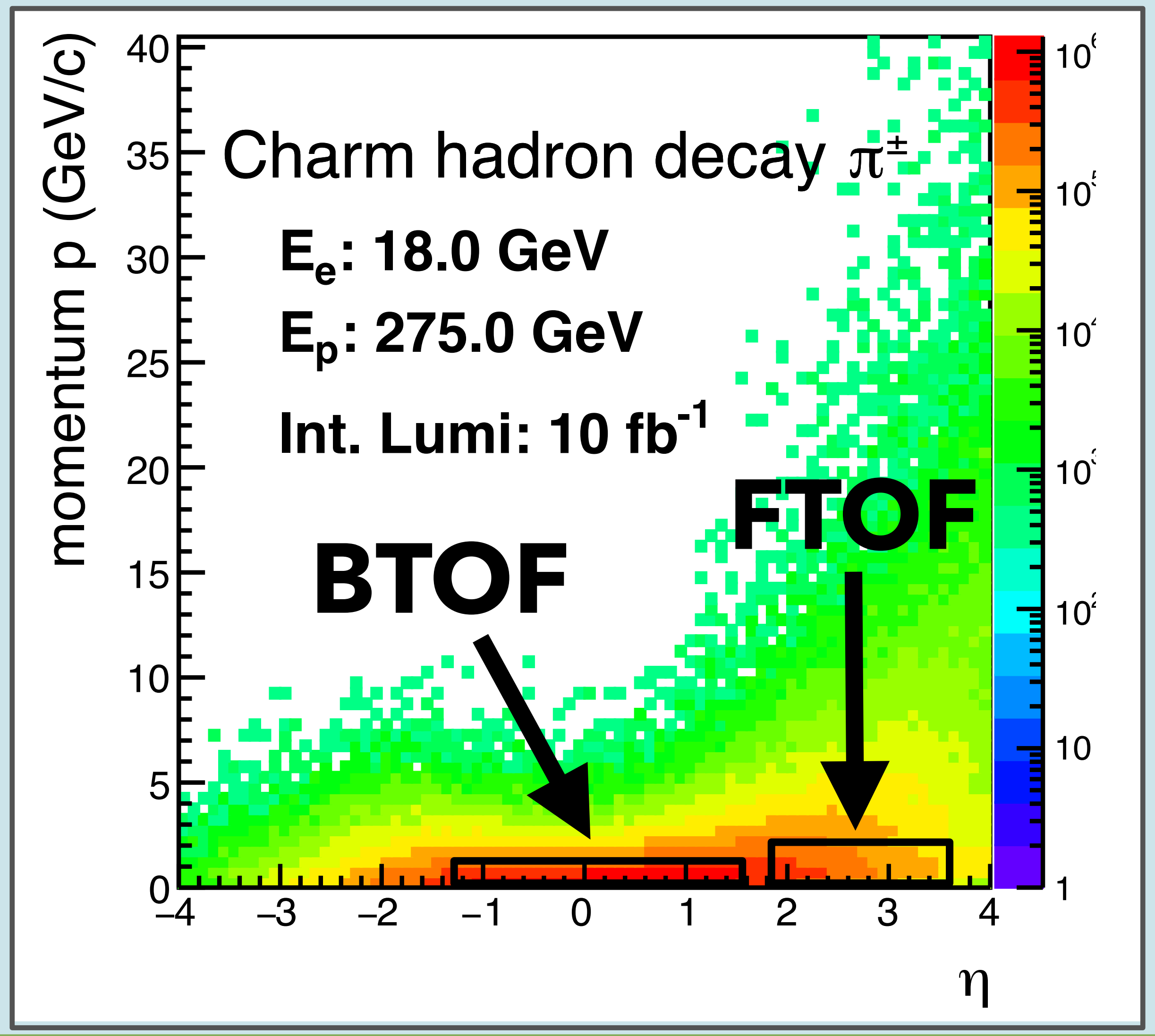


Decay particle kinematics



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- AC-LGAD is the most promising technology for TOF
  - High-timing resolution σ_t = ~30ps
  - High-spatial resolution σ_{xy} = ~30 μm
  - Space-saving design ΔD < 10cm
  - **but… no experiments have been used so far…**

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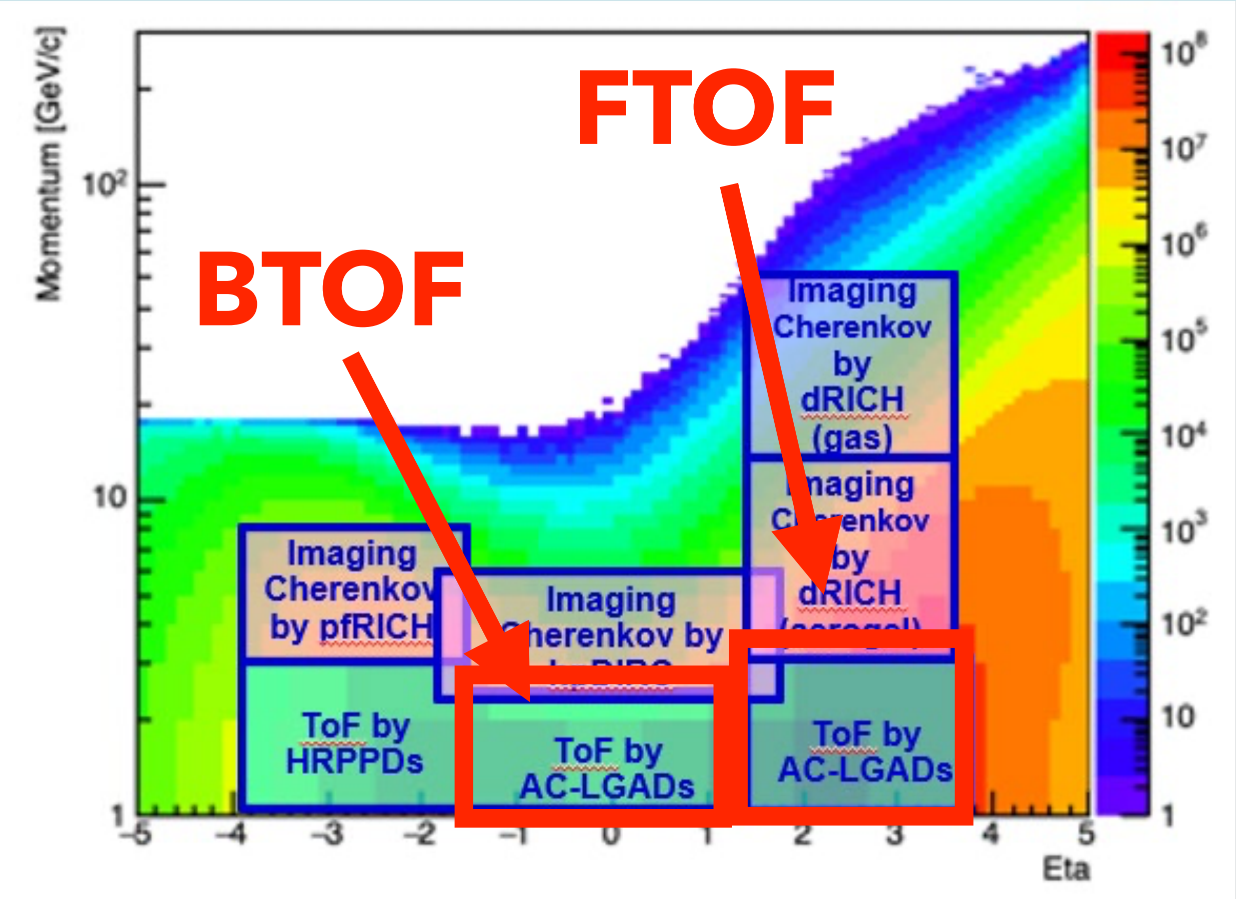

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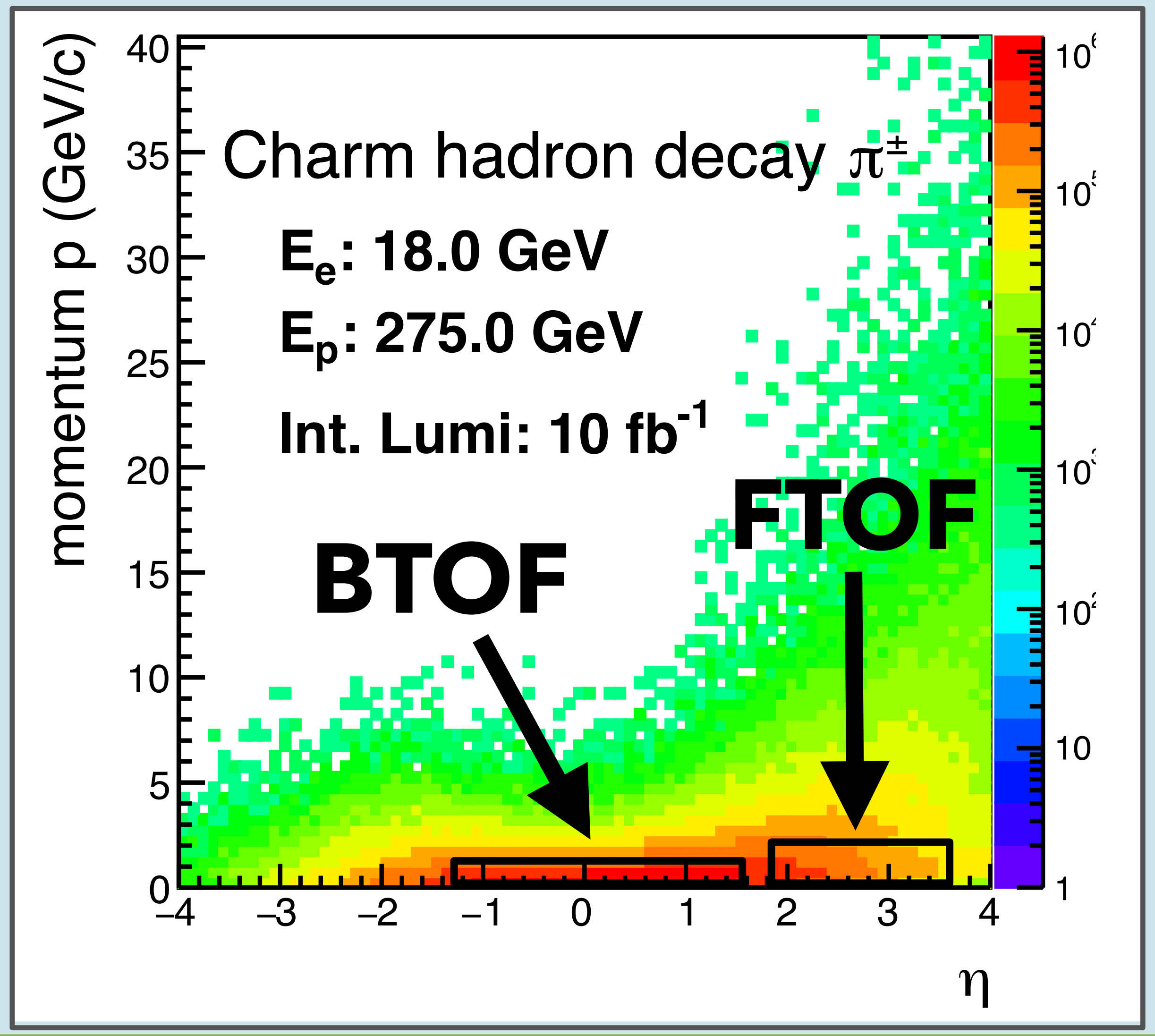

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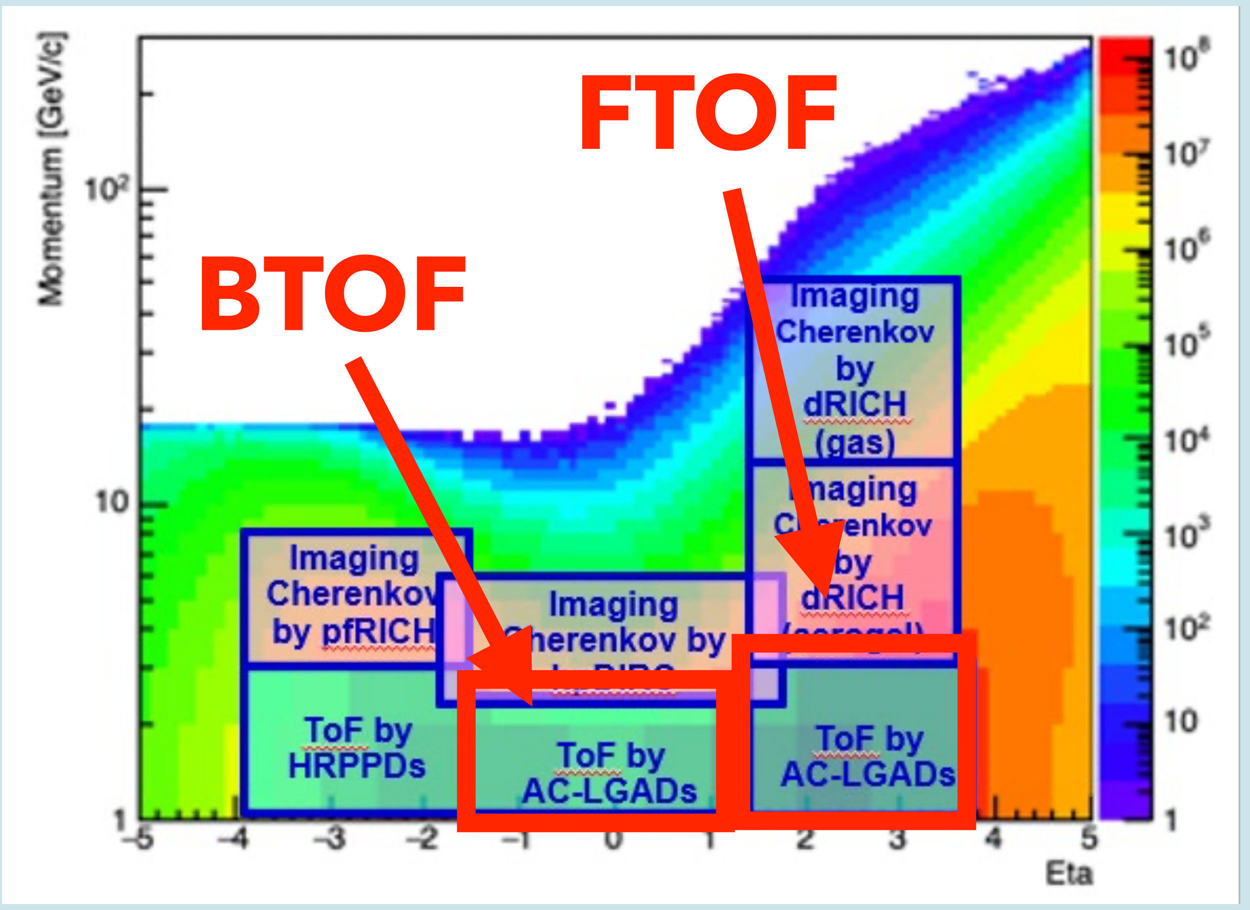
TOF is one of the most important detectors for ePIC and also the most challenging detector

Detectors for PID



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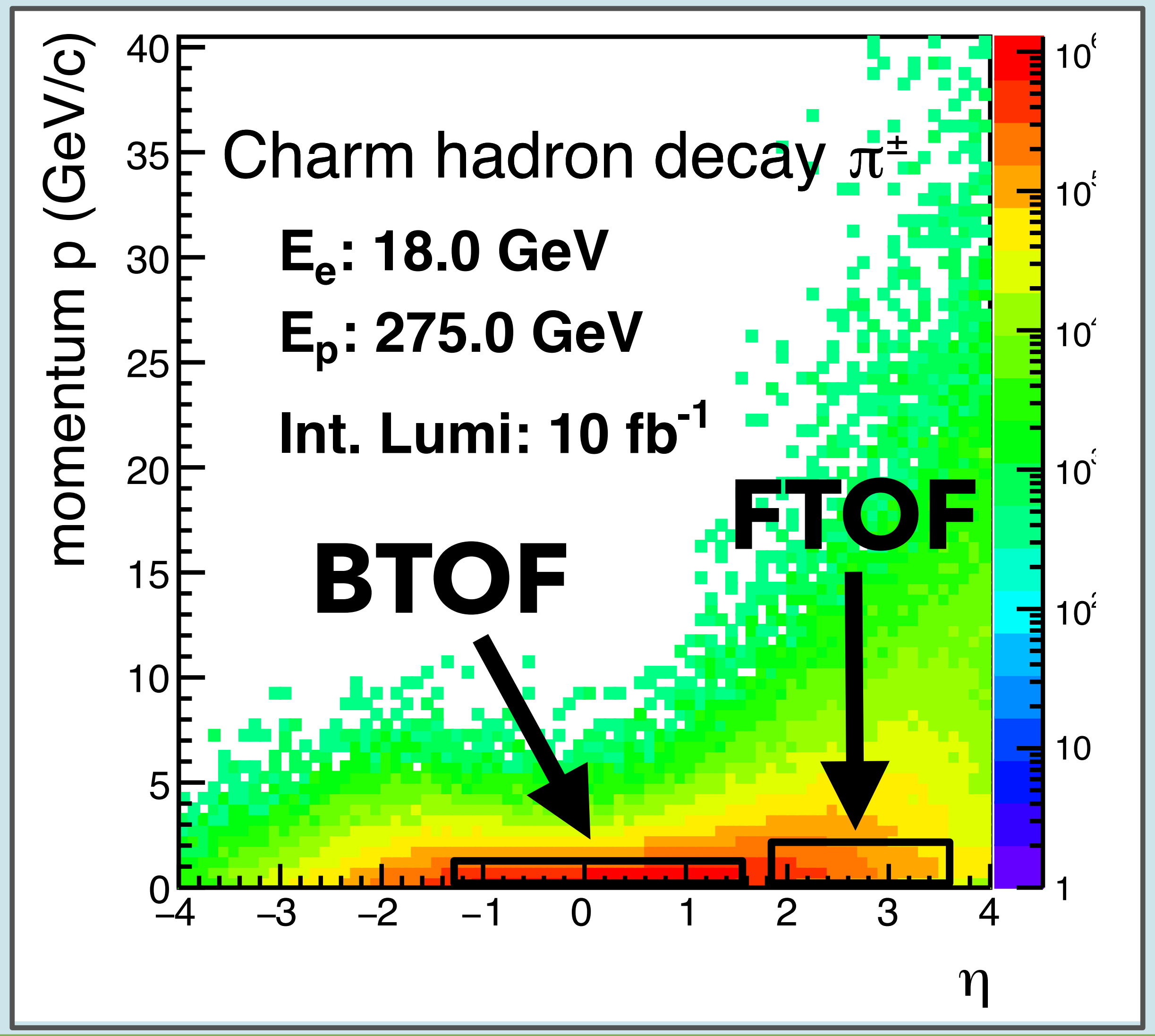
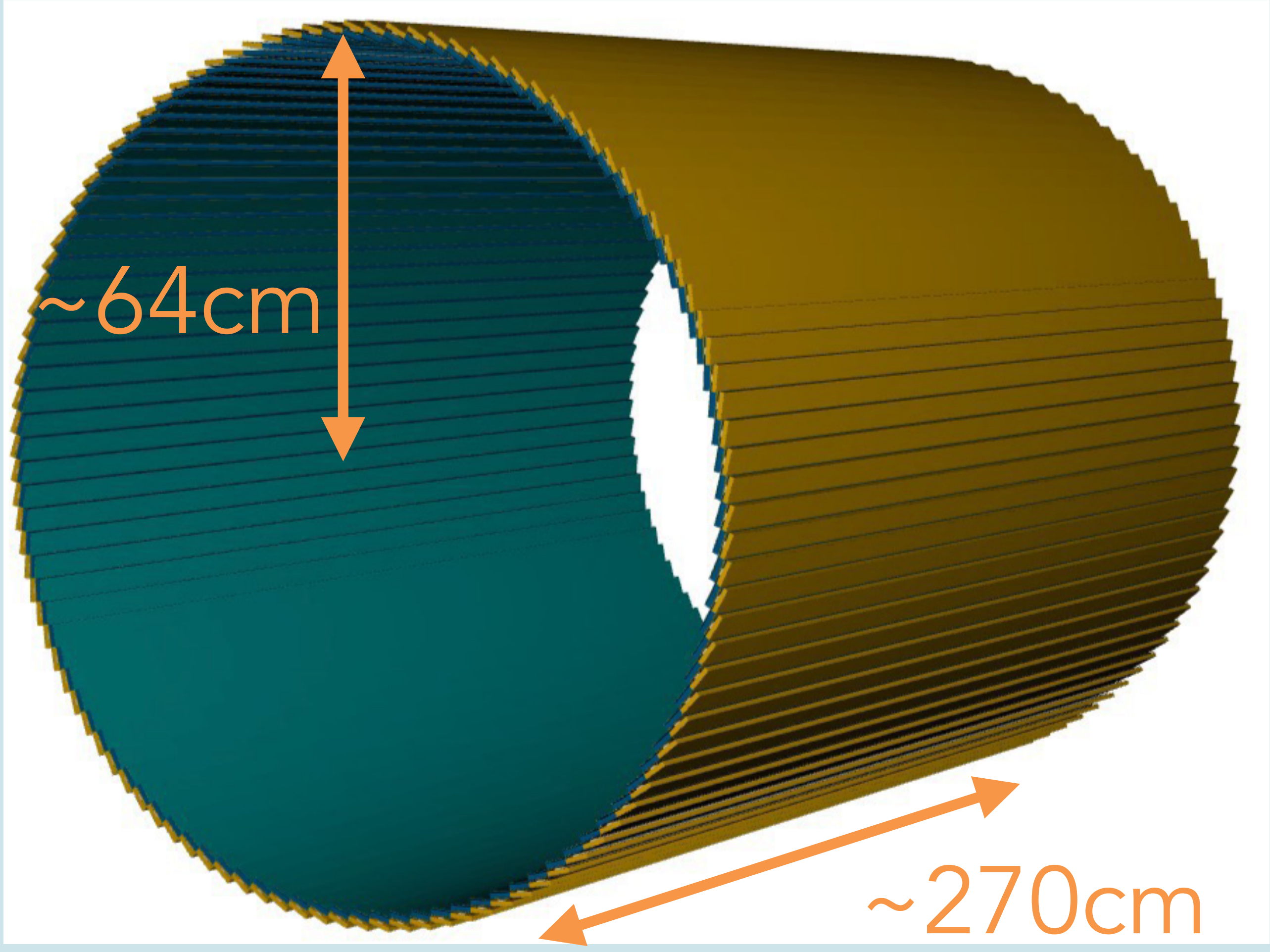


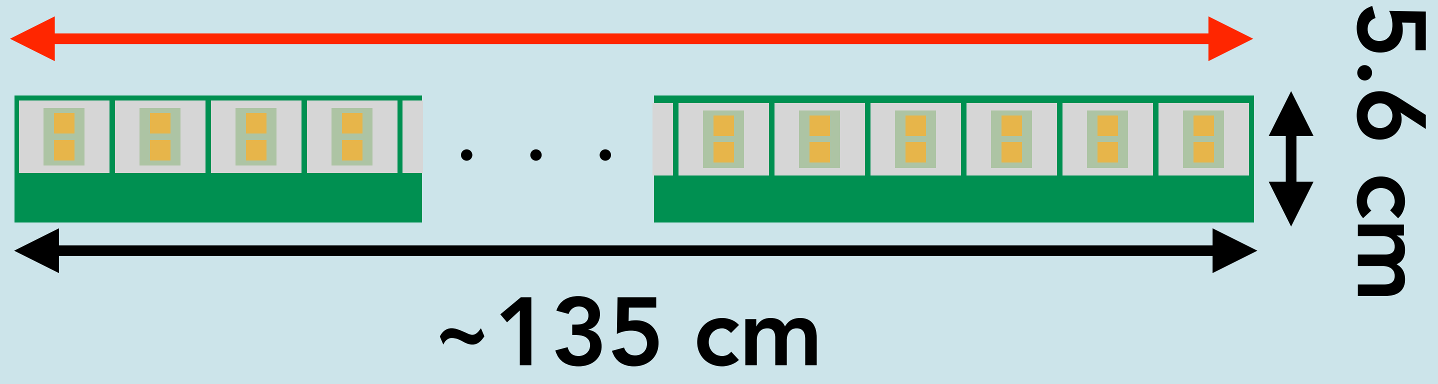
Recap of BTOF and FTOF

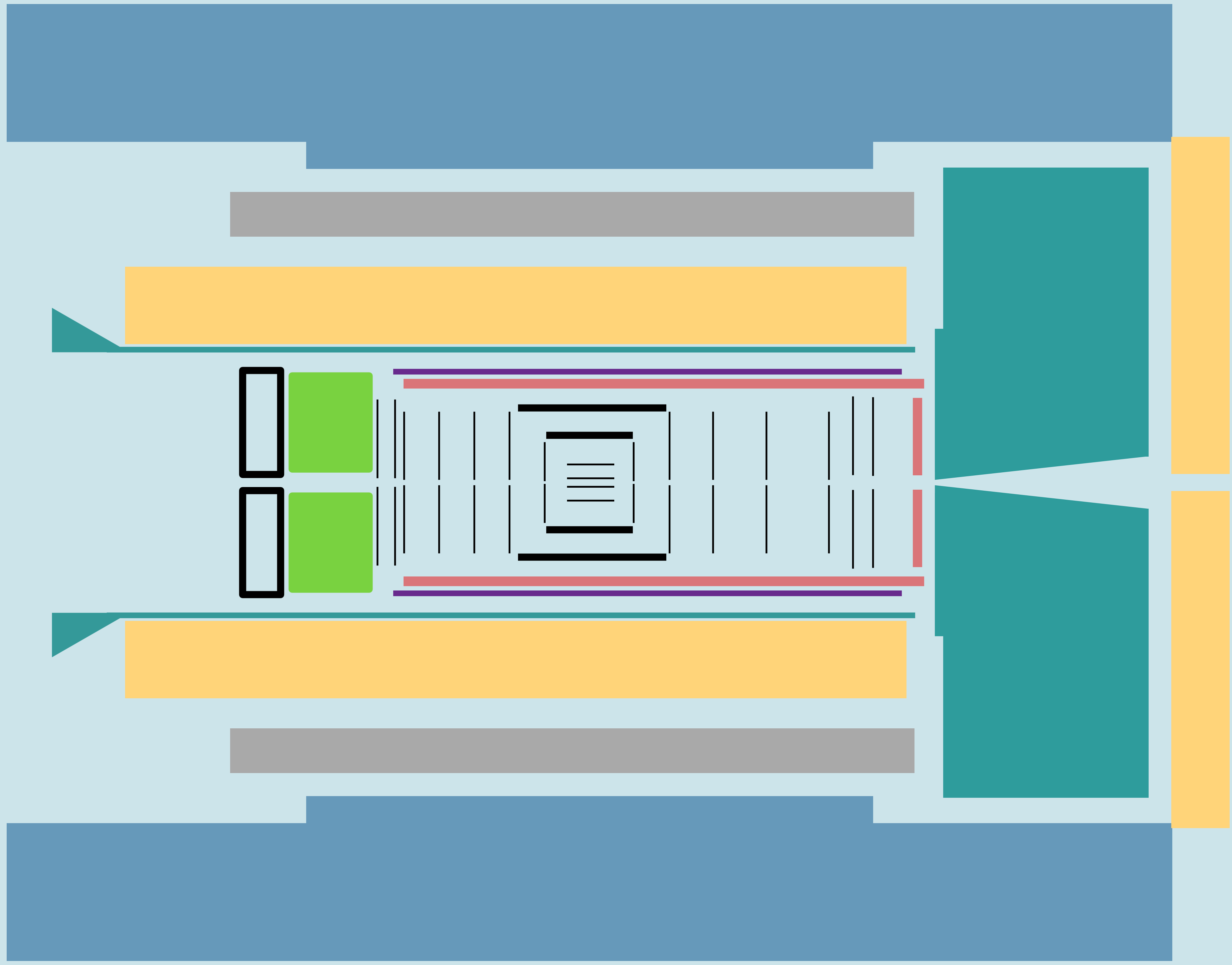
BTOF shape



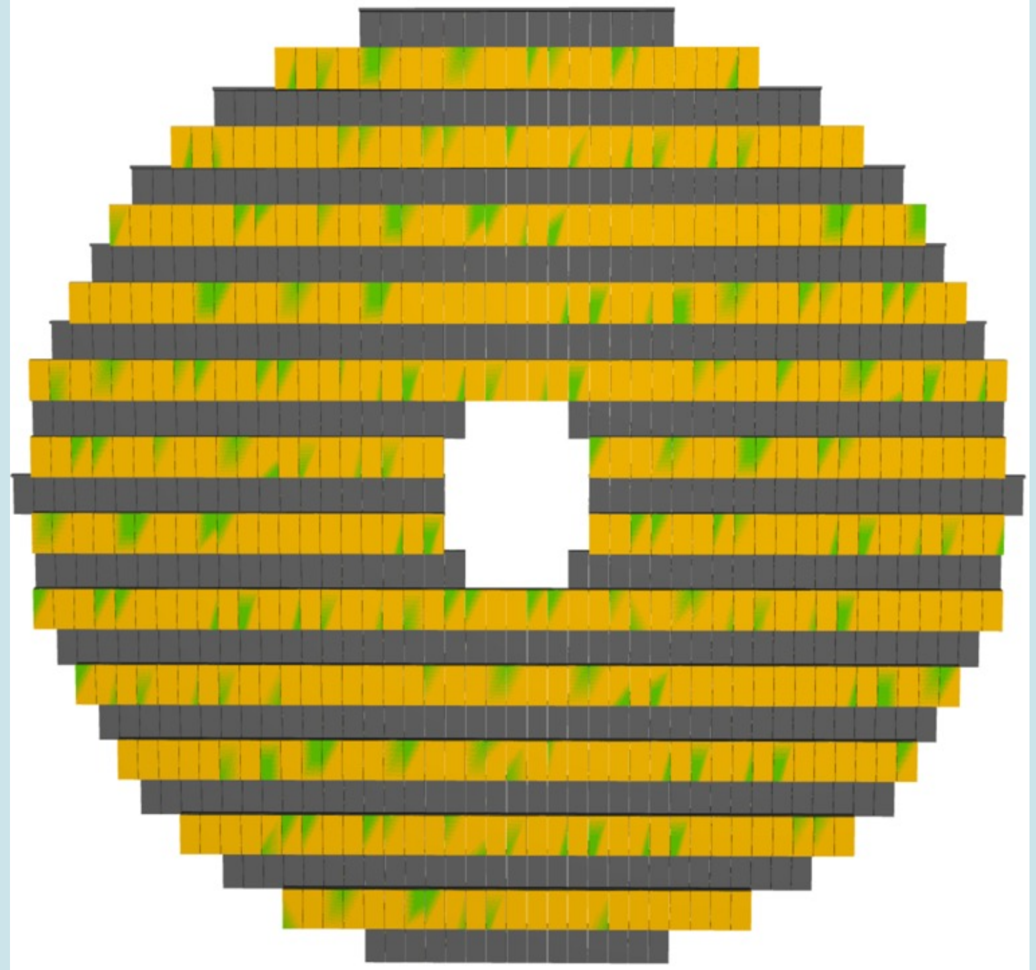
BTOF half Stave

32 AC-LGADs 64 ASICs



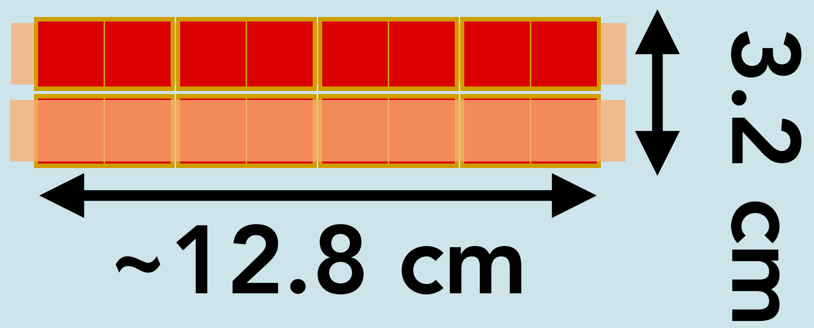


FTOF shape



FTOF Module

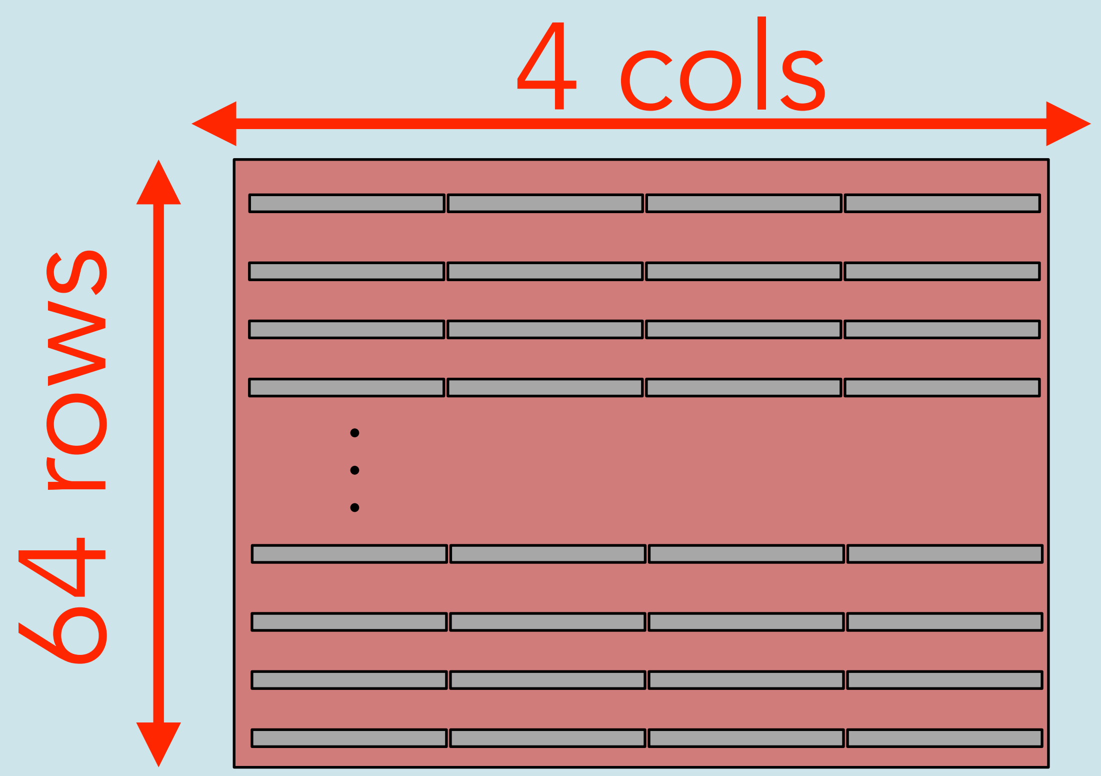
16 AC-LGADs 16 ASICs



- Strip-type and pixel-type AC-LGAD are used for BTOF and FTOF, respectively
- Different ASICs are used for BTOF and FTOF due to different sensor properties

AC-LGAD for BTOF and FTOF

- **Strip-type** sensor, 3.2 x 4 cm^2 sensor size with 0.05 x 1 cm^2 metals, is used in **BTOF**
- The readout metal geometry is 64 x 4 and 256 channels in total each
- 2 ASICs are attached to each sensor with wire bonding



- BTOF strip sensor
  - **9216 sensors**
  - **10 m^2**
  - **2.4 M readout channels**

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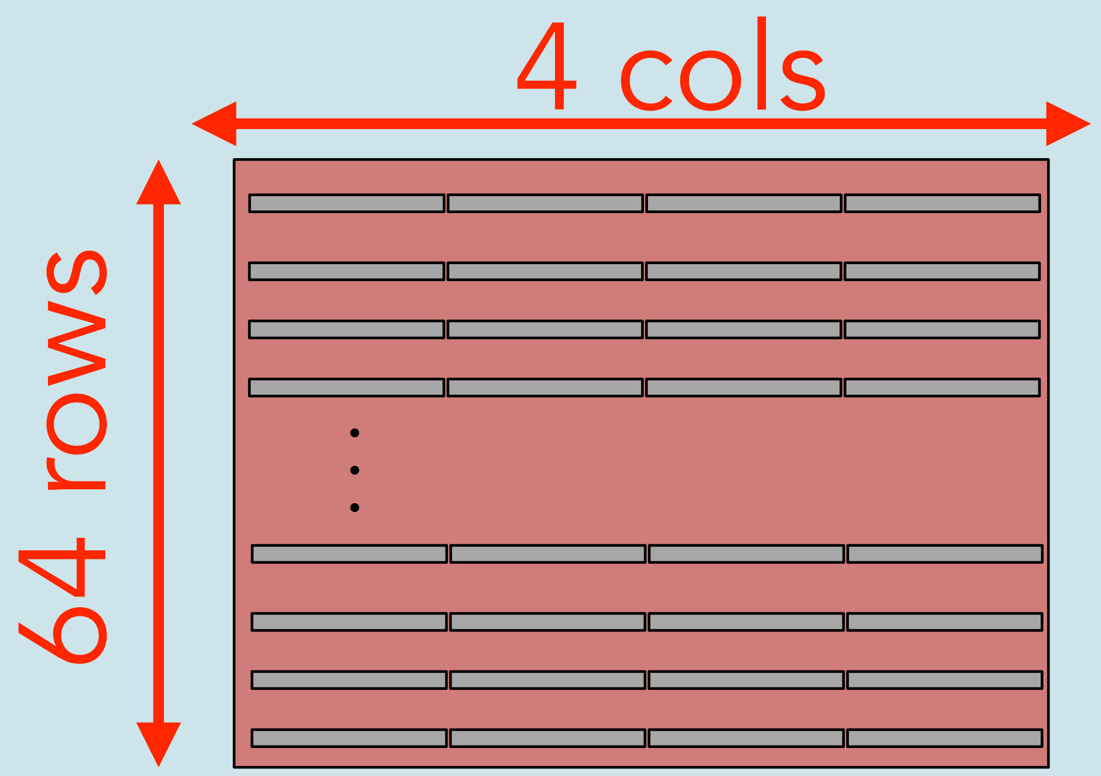
- **Pixel-type** AC-LGAD sensor, 1.6 x 1.6 cm^2 sensor size with 0.05 x 0.05 cm^2 metals, is used in **FTOF**
- The readout metal geometry is 32 x 32 and 1024 channels in total each
- 1 ASIC (2D 32x32) is attached to the one sensor



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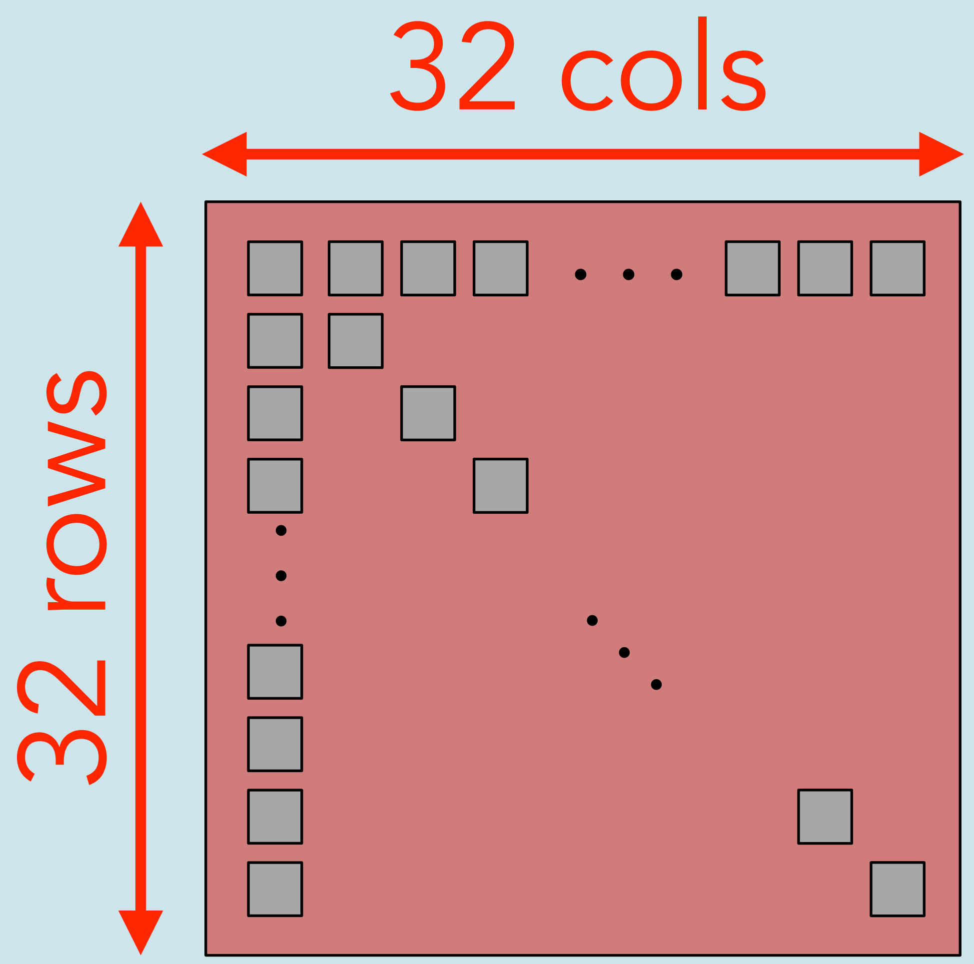
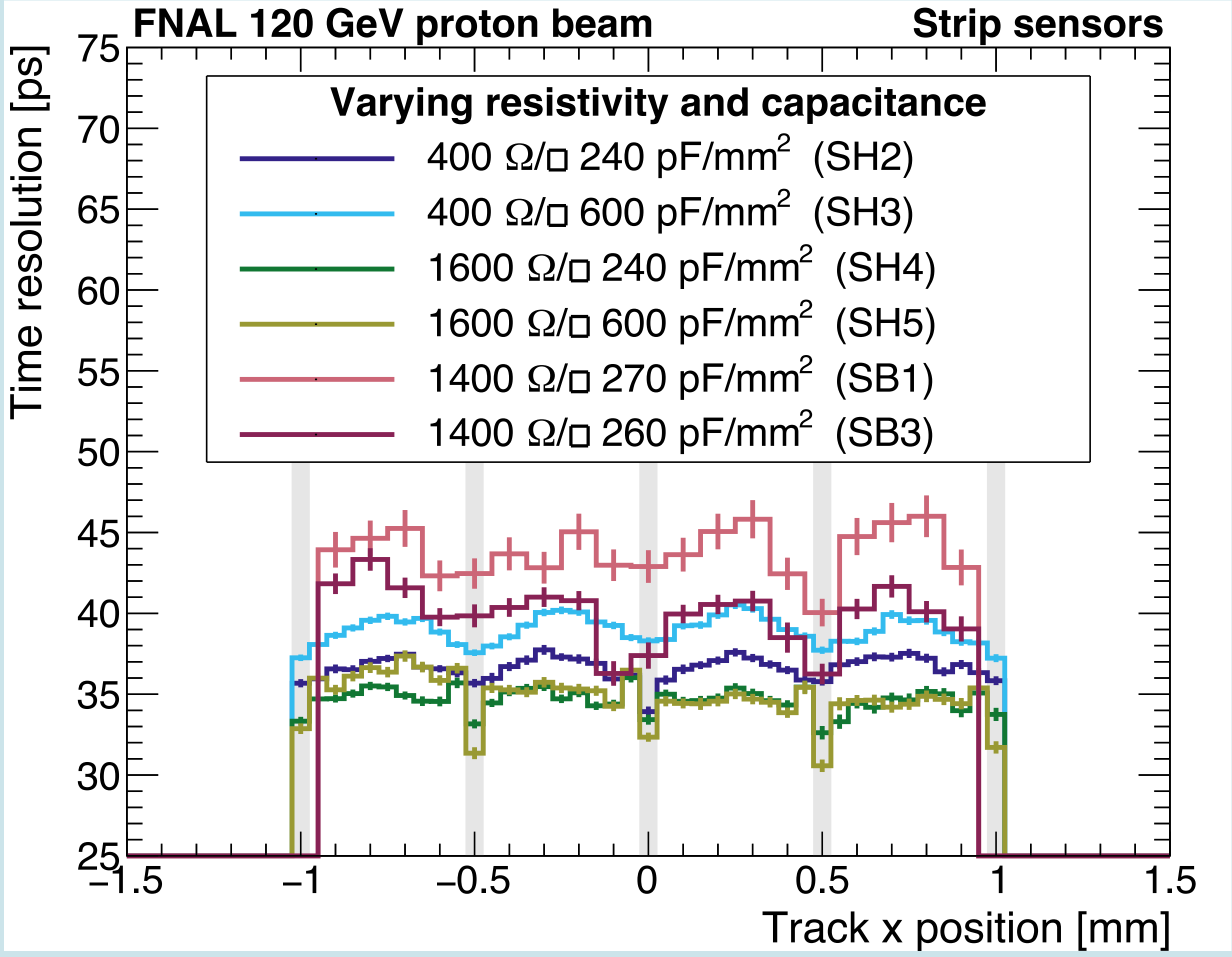
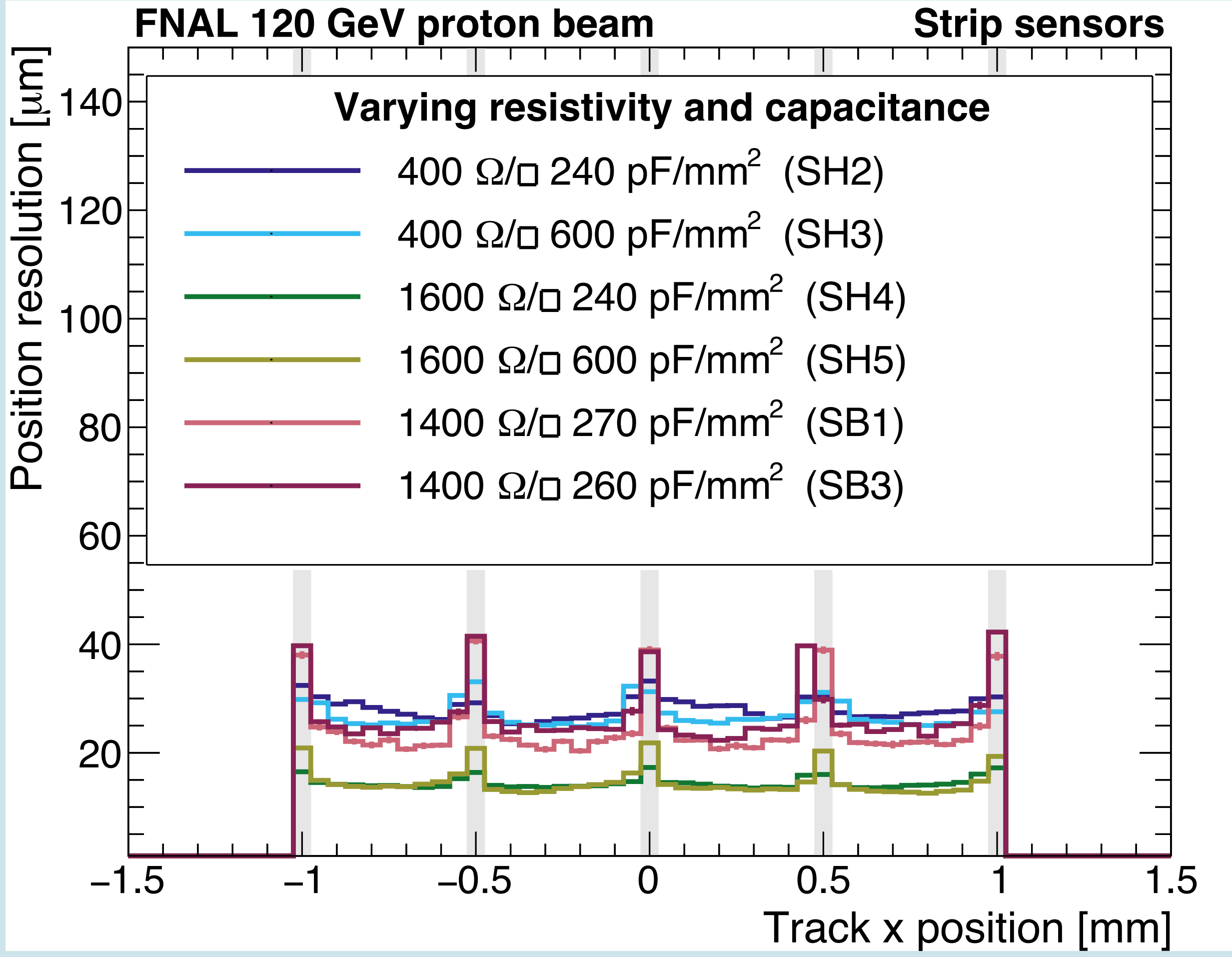


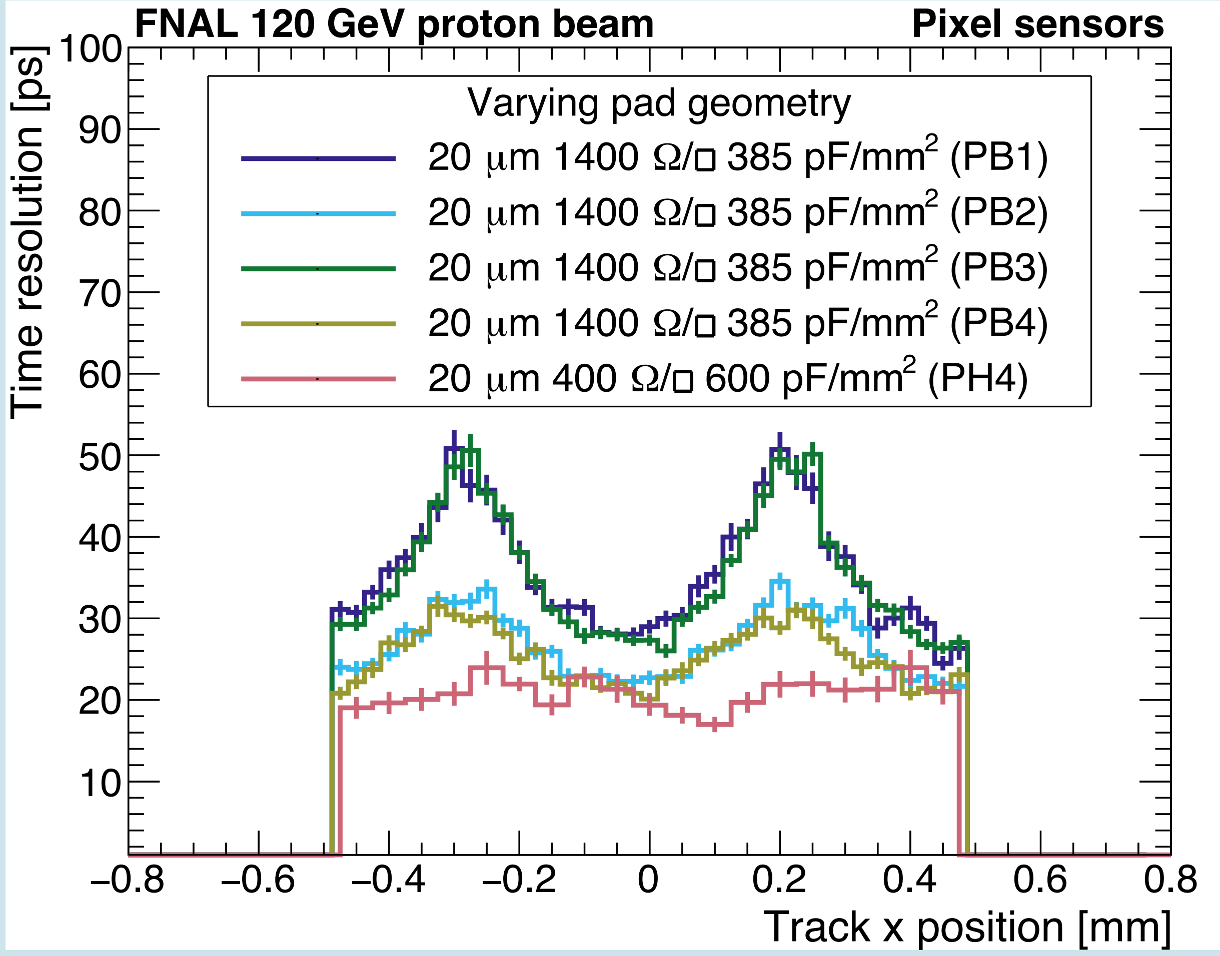
- FTOF pixel sensor
  - **3632 sensors**
  - **1.4 m^2**
  - **3.6 M readout channels**

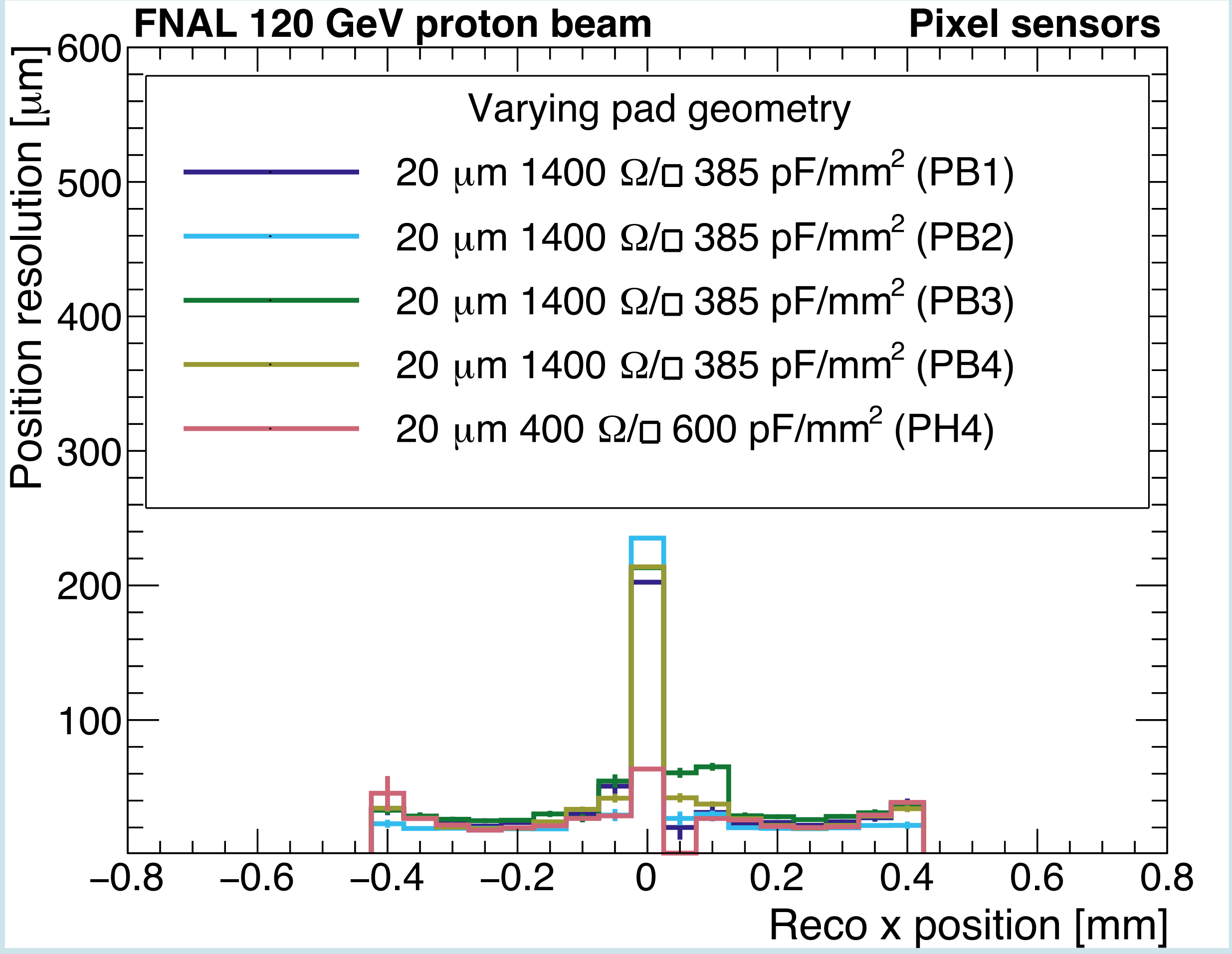
Latest sensor performance

Beam test result at FNAL (from FY24 report by FNAL, LBNL and UIC)









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  - Performance redundancy should be considered
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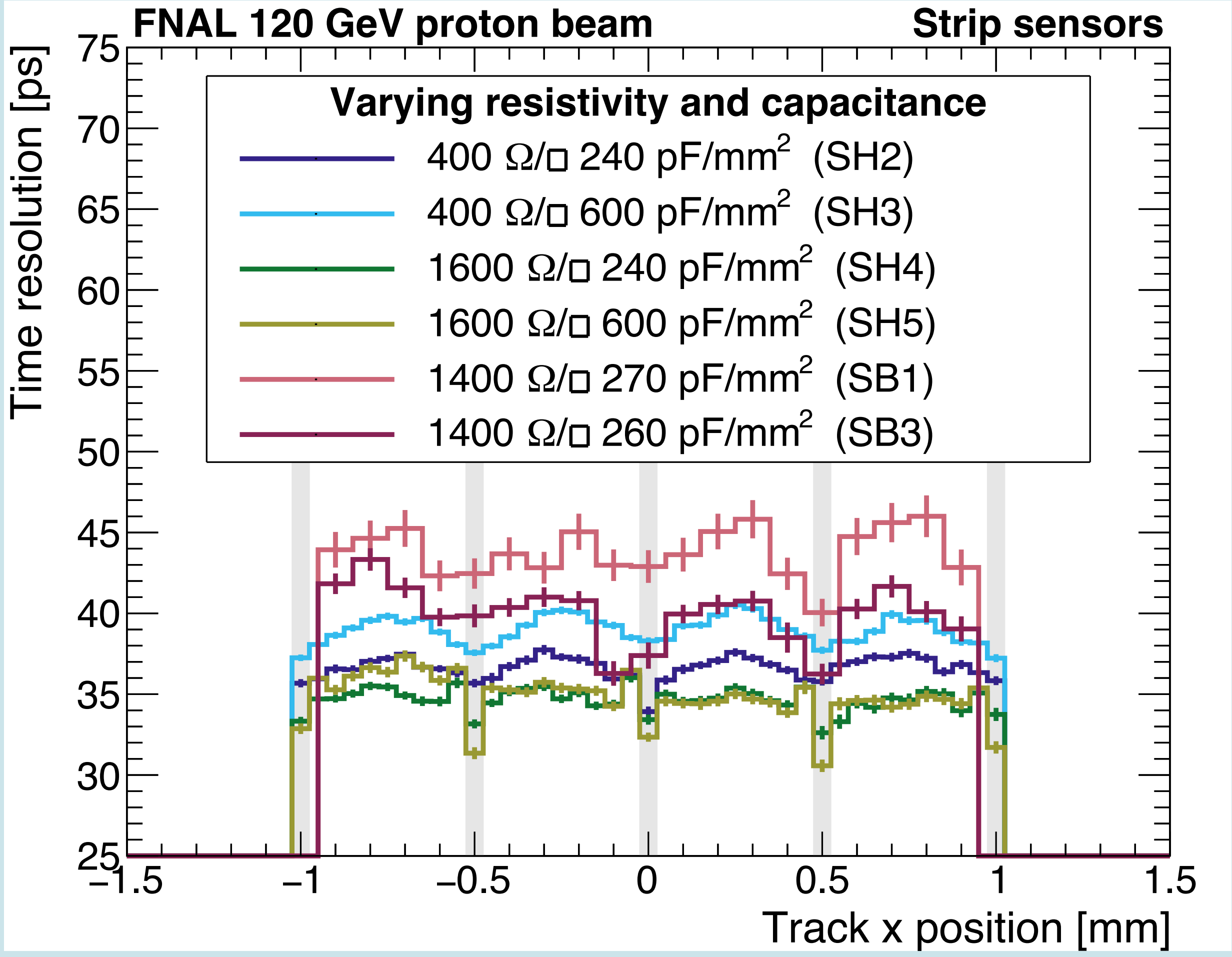

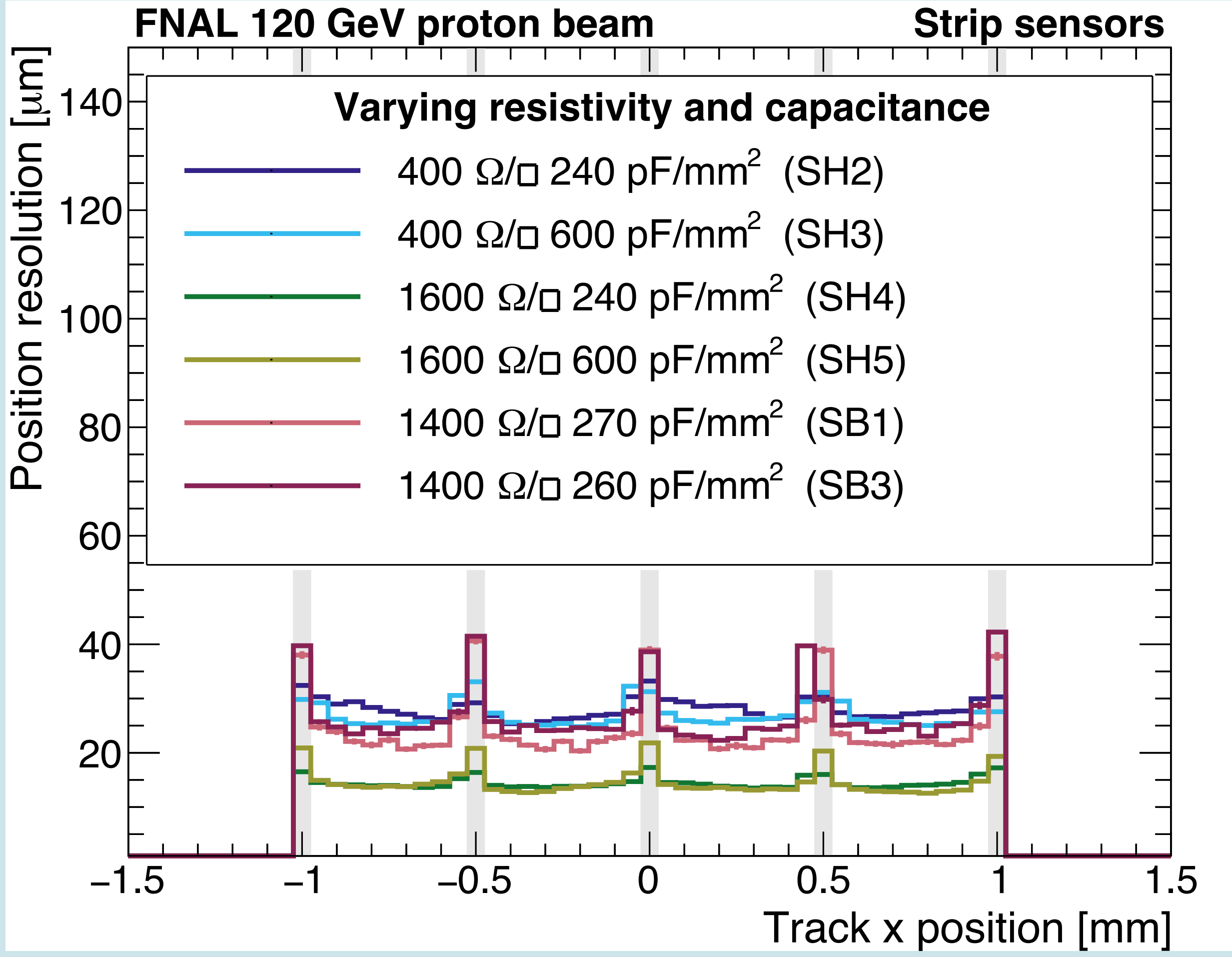

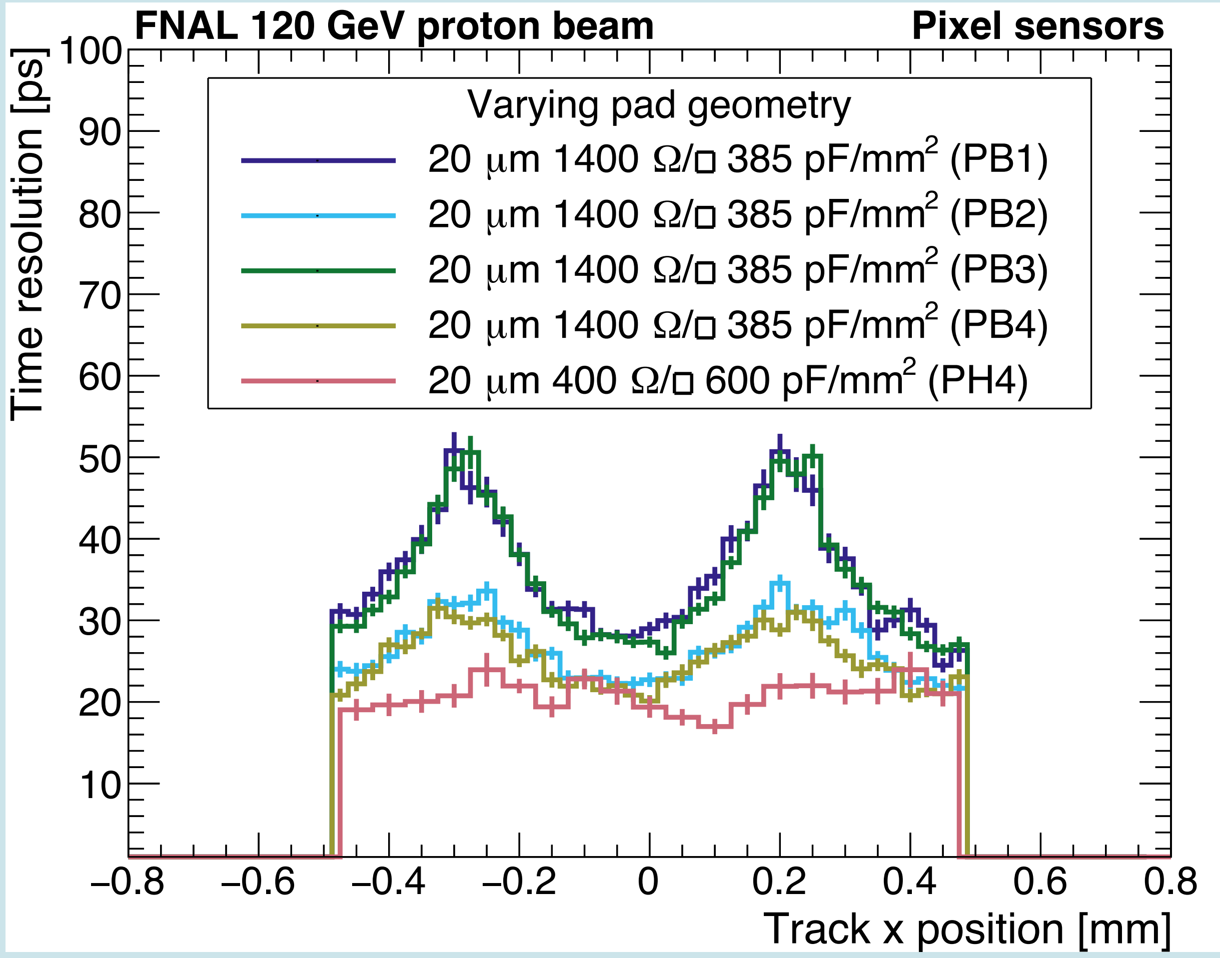

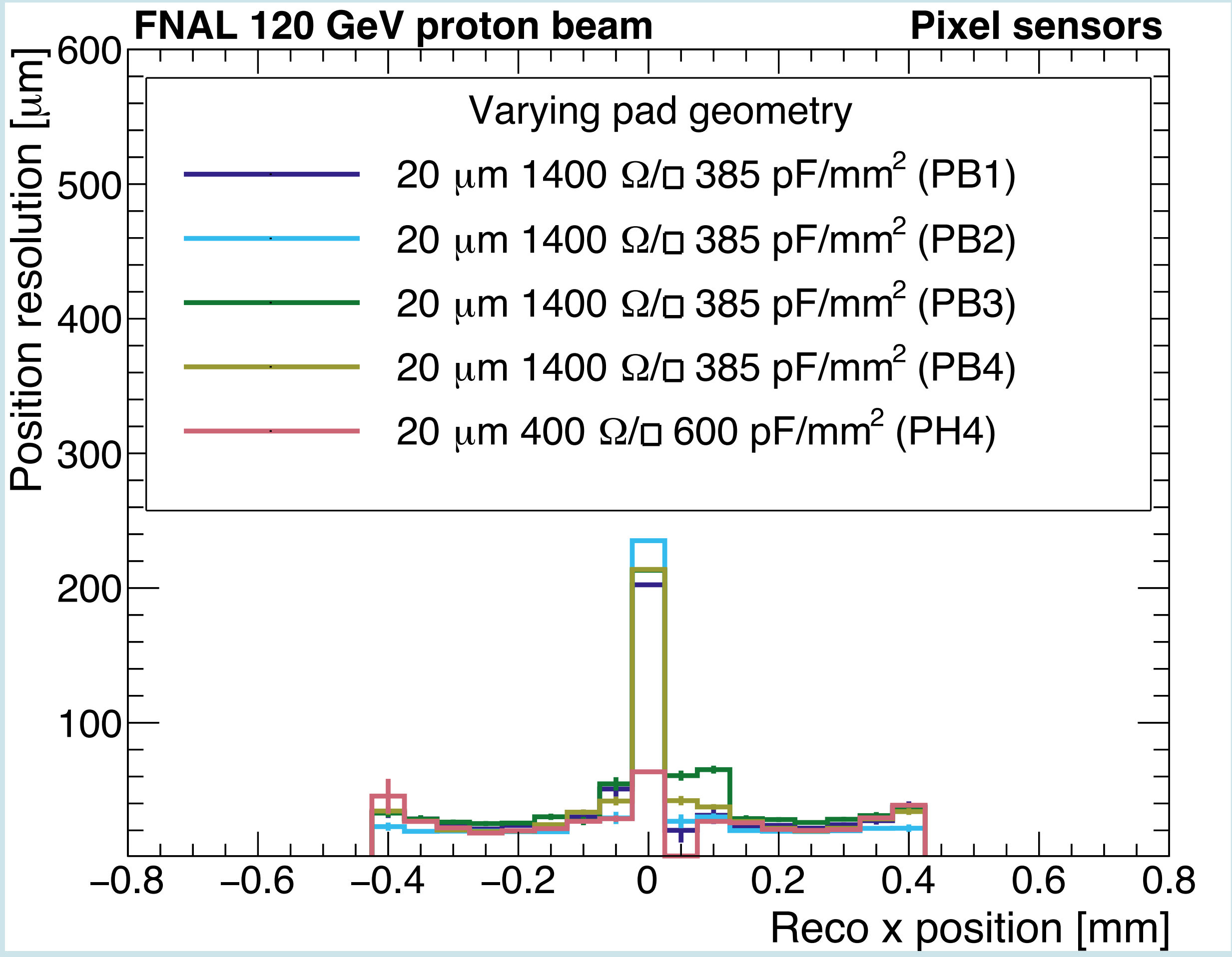

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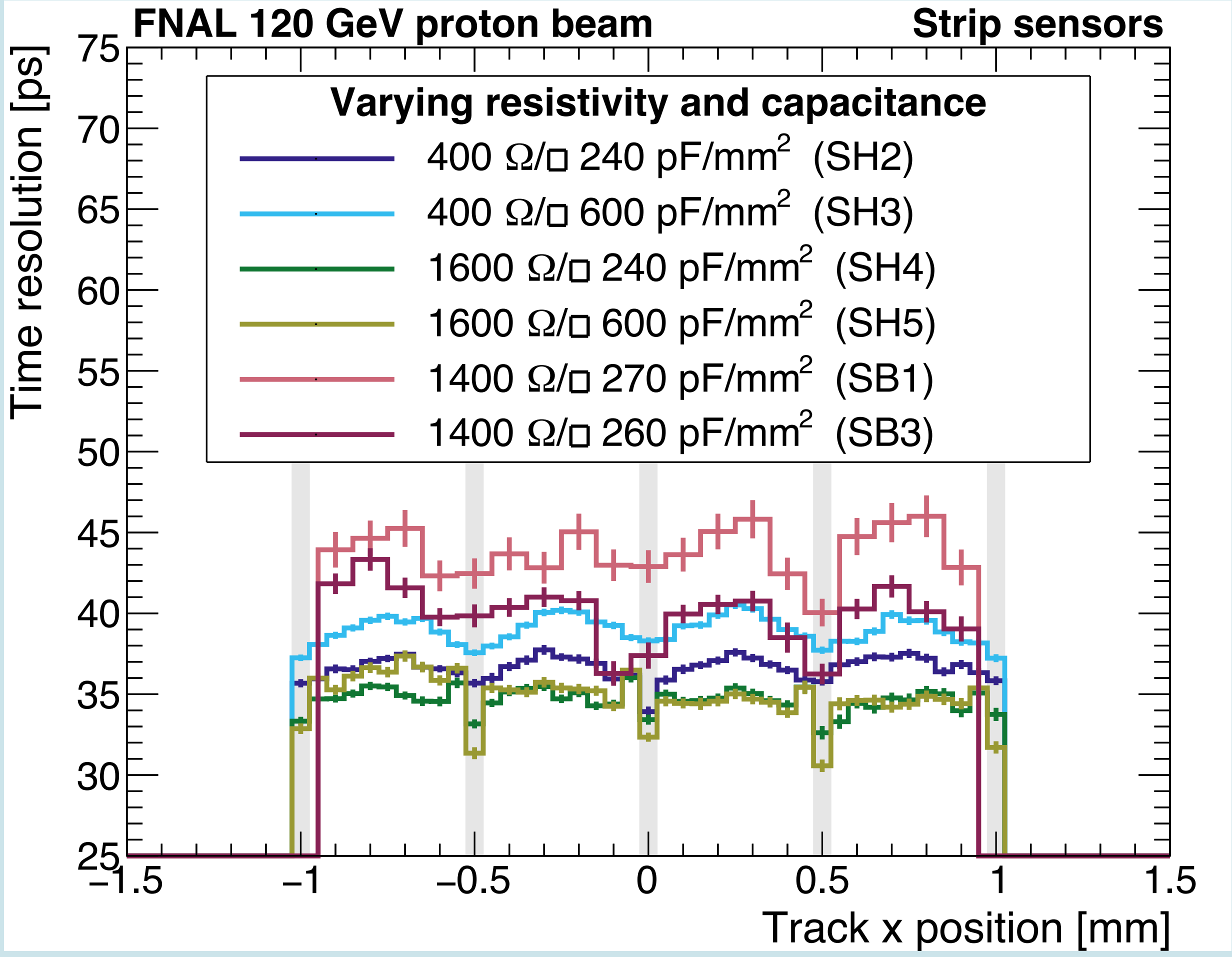

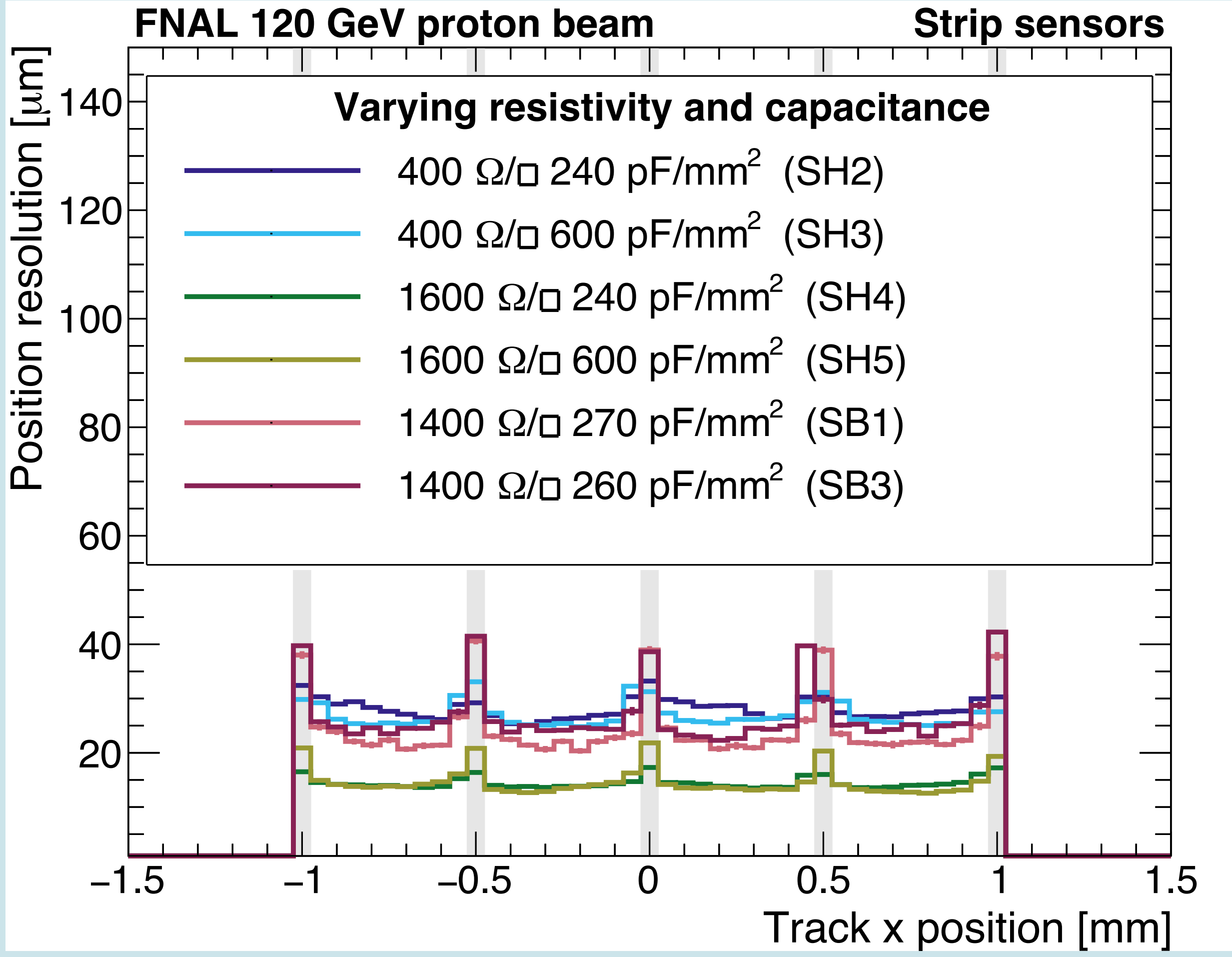

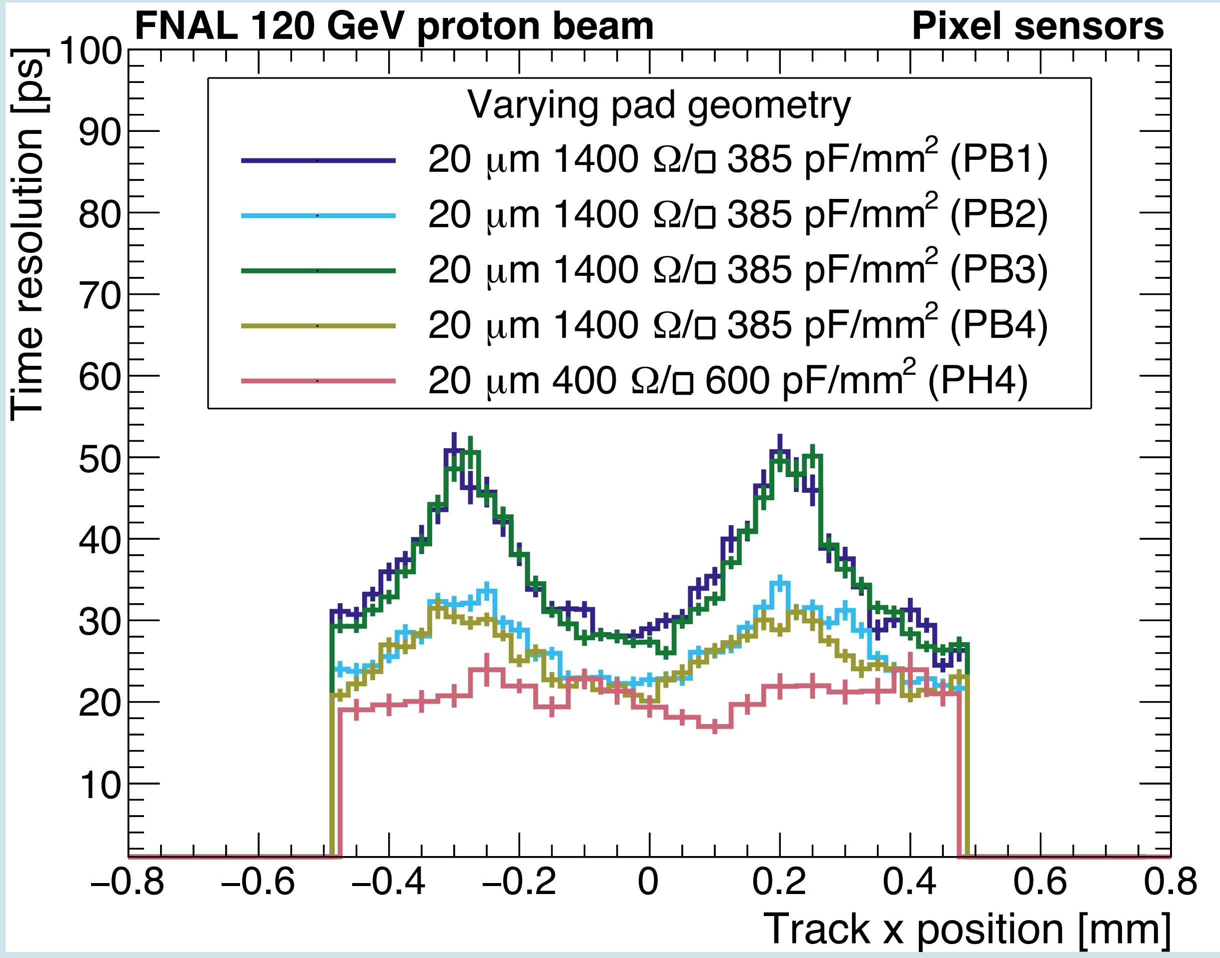

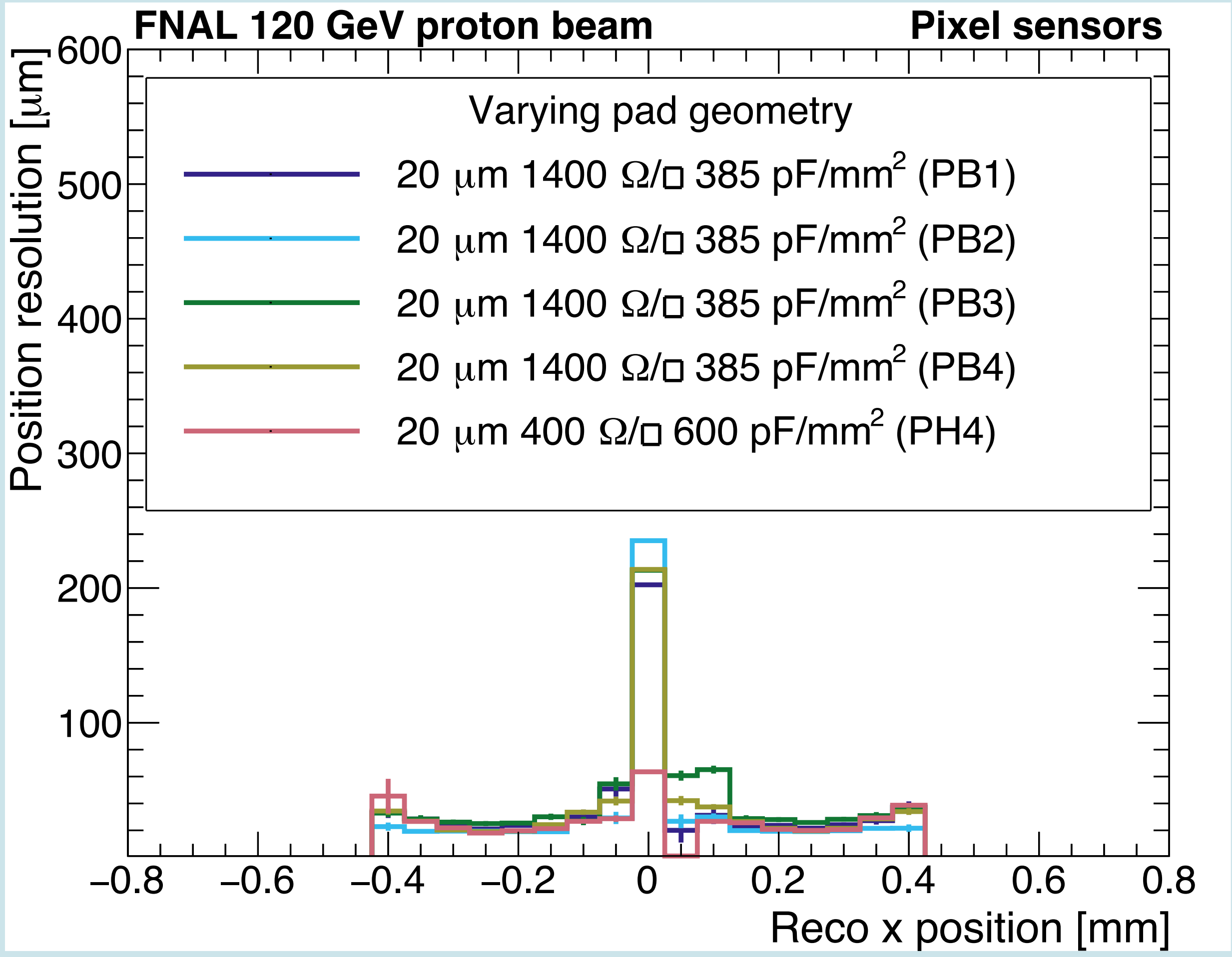

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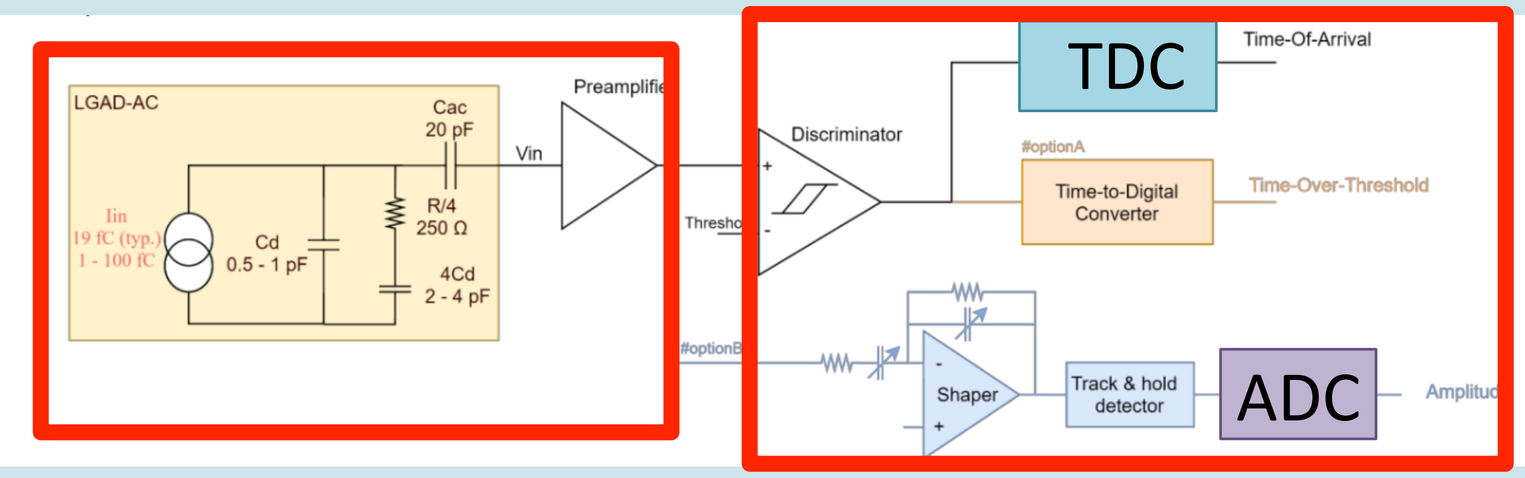
- Sensor temperature dependence study is mandatory and ongoing

TOF ASIC

- EICROC (32x32 = 1024ch) is one of the common ASICs used in ePIC
  - Design suits to pixel-type AC-LGAD readout (for low input capacitance)
  - 10-bit TDC and 8-bit ADC is now available (EICROC0)

Analog block Digital block



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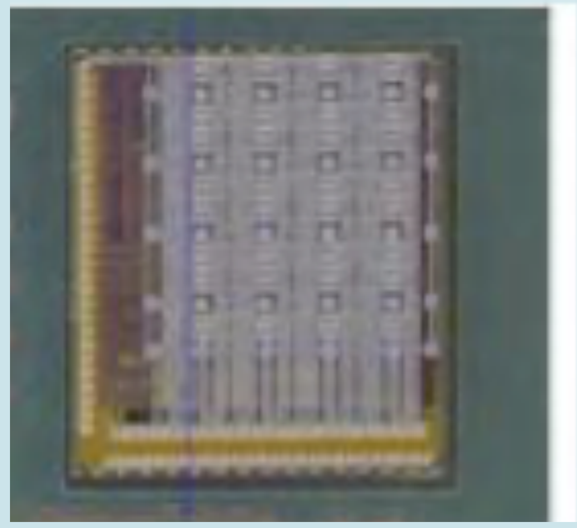

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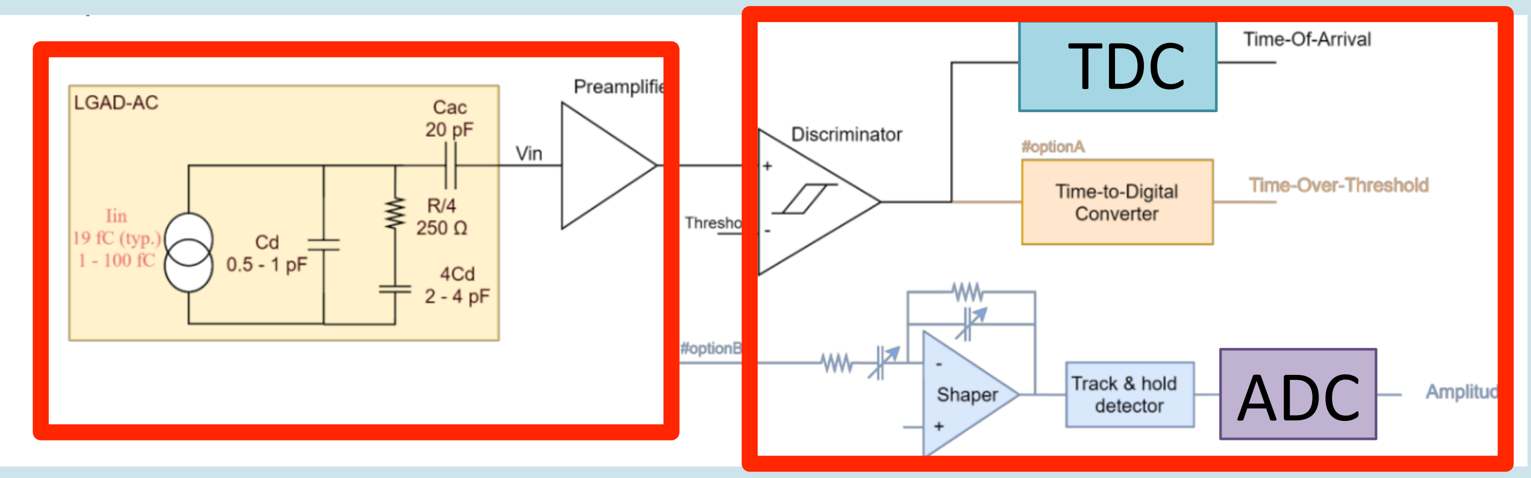

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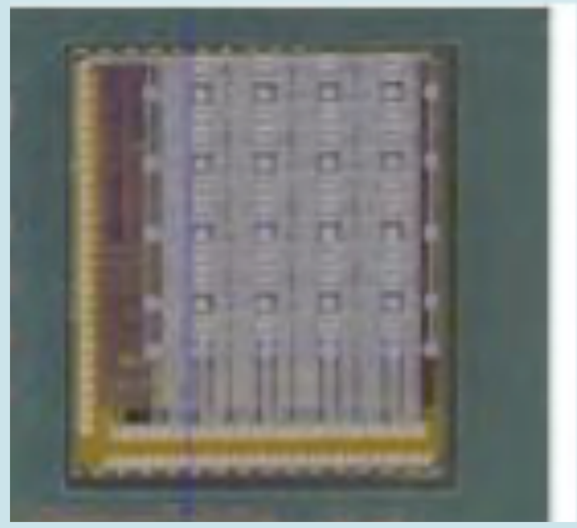

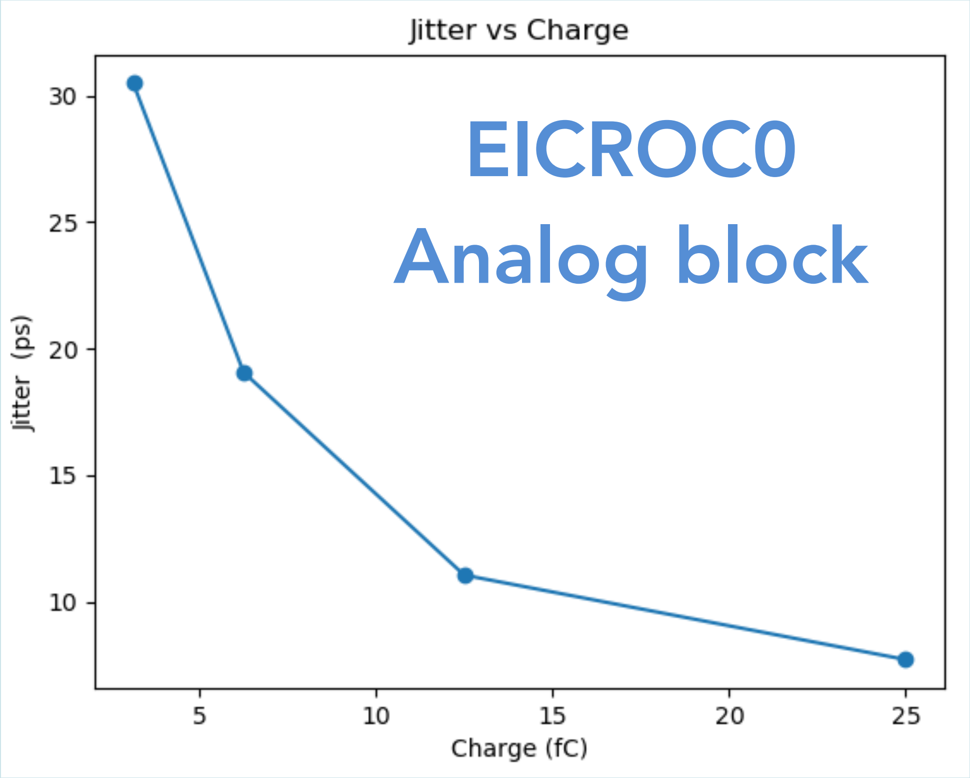

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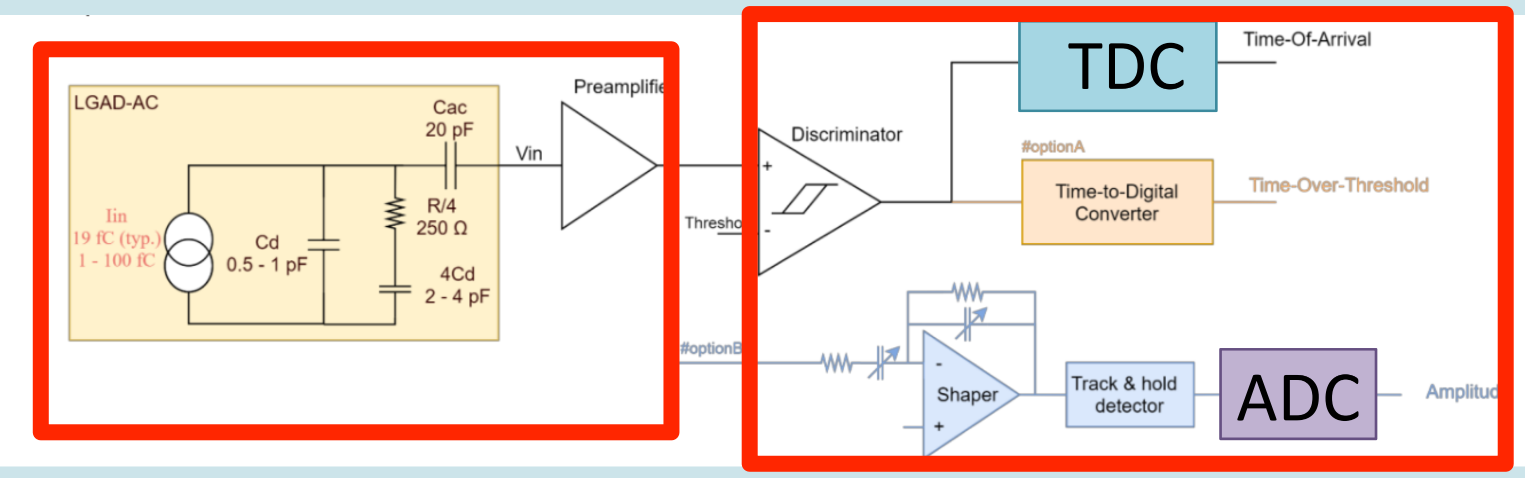

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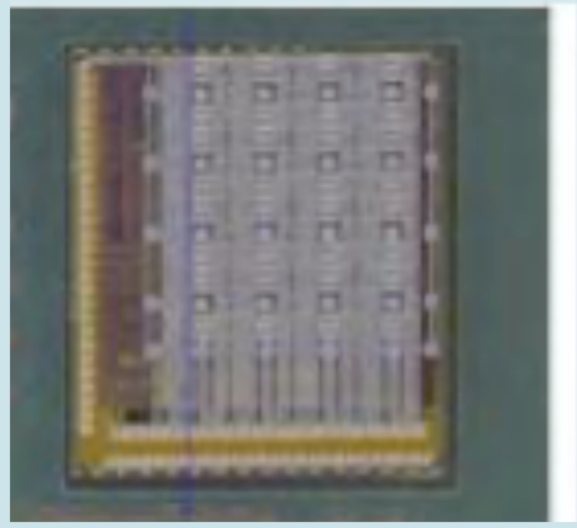
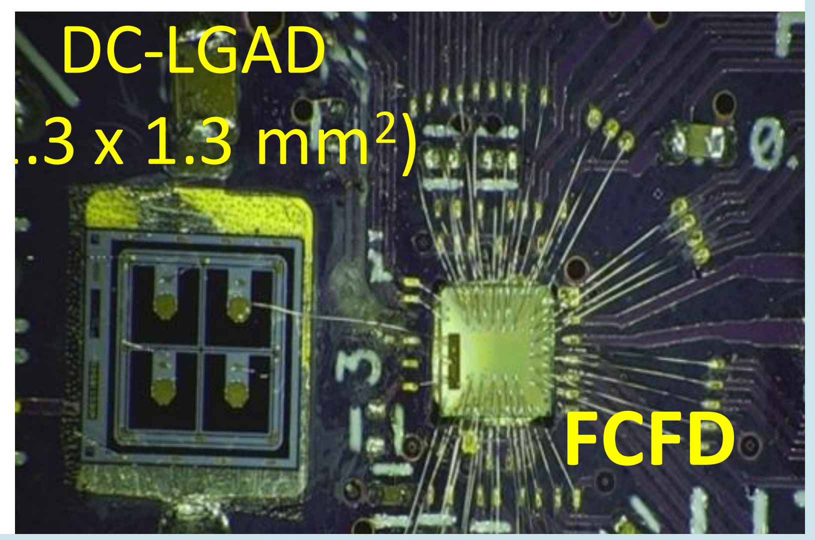
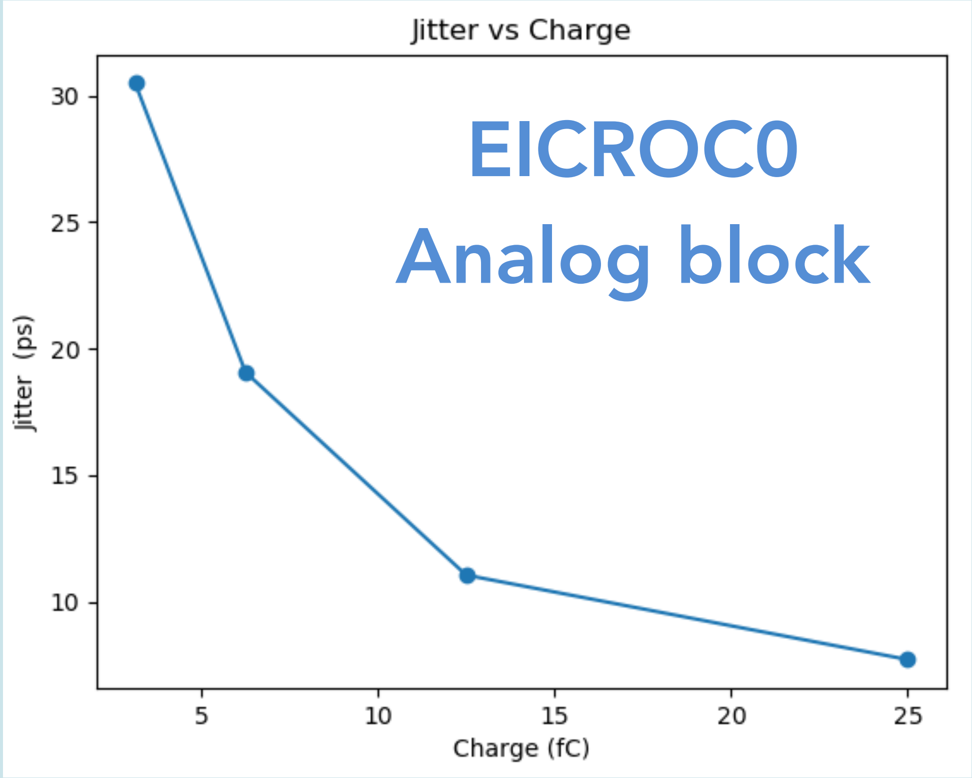


FCFDv1



HGCROC3



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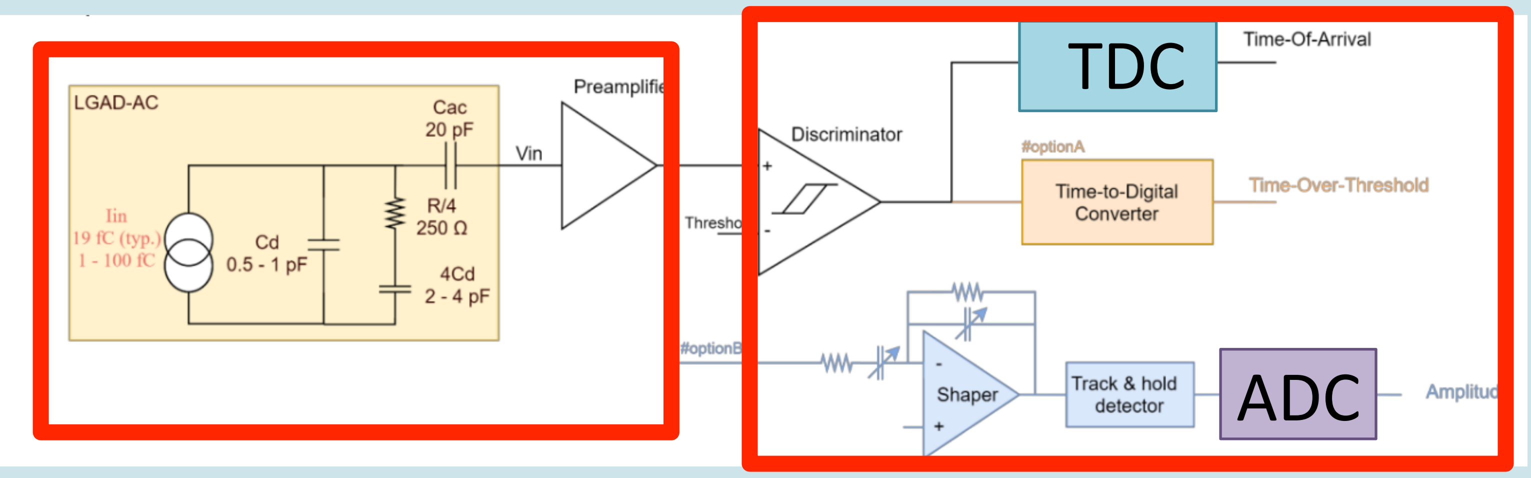

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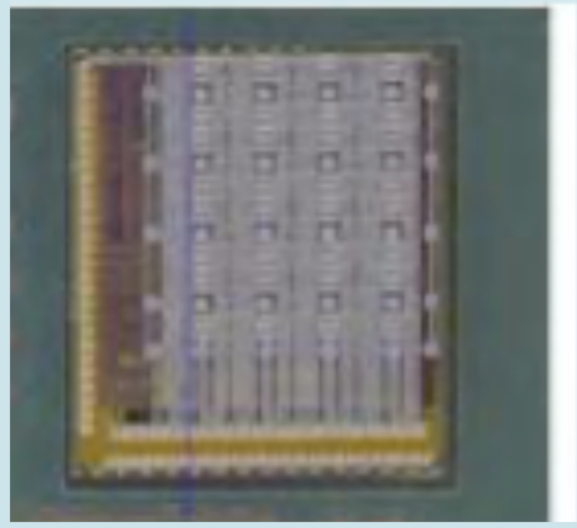

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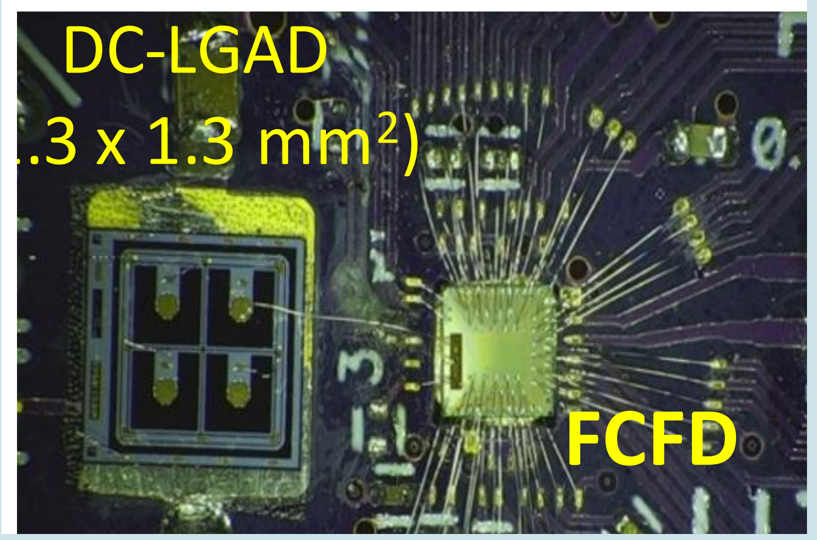
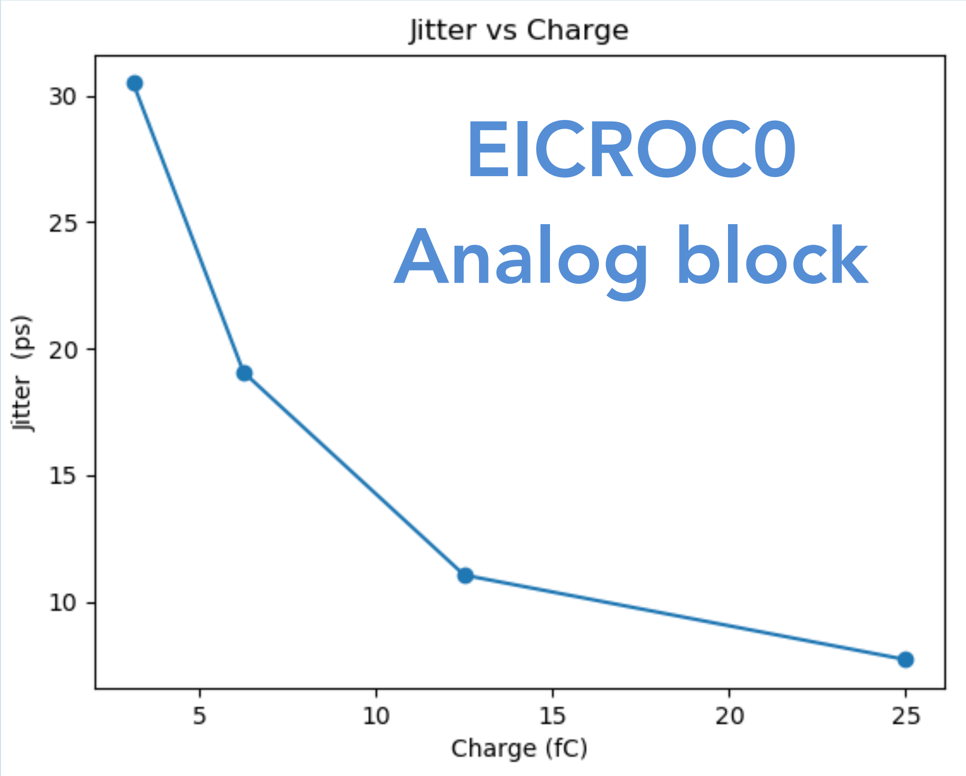
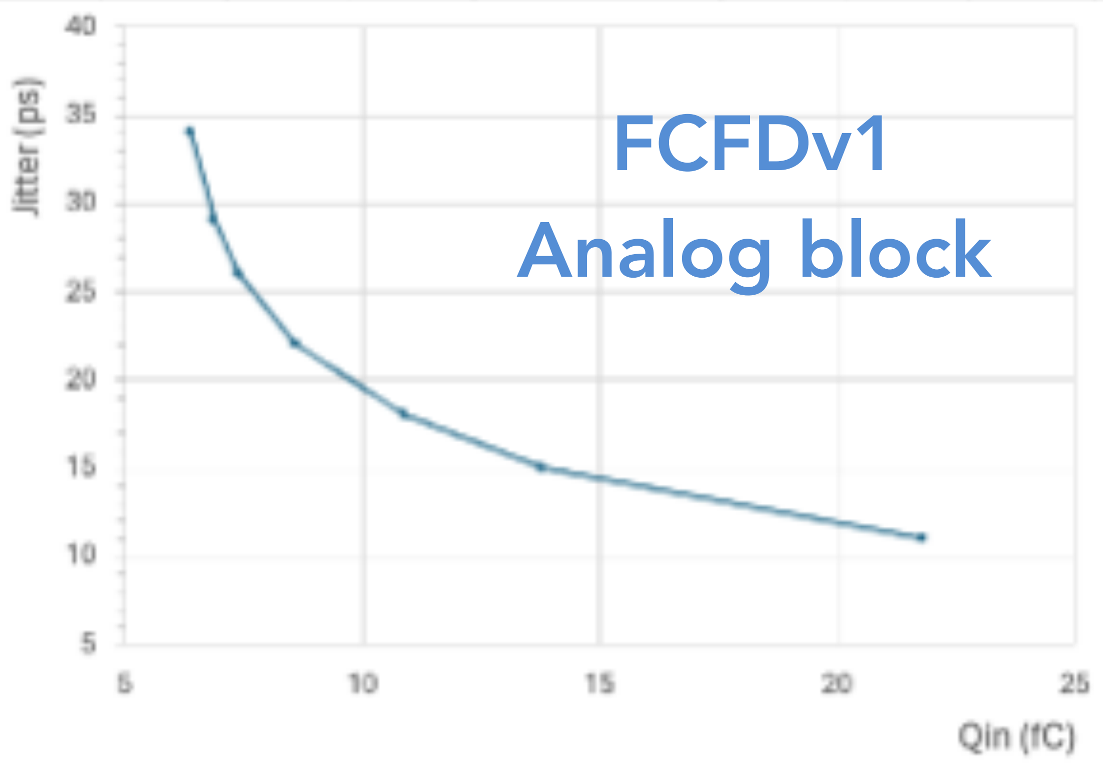


HGCROC3





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    - HGCROC has been developed for CMS Calorimeter and is ready
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- The possibility of third-party ASICs has begun to be discussed
  - ASROC and HPSoC are one of the options

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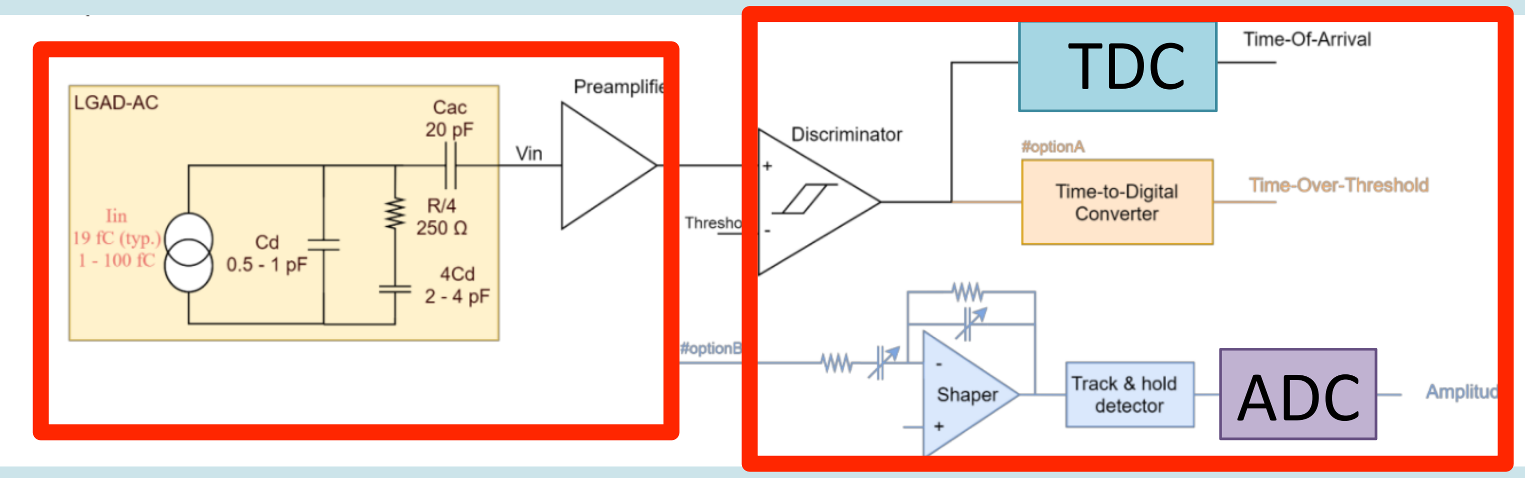

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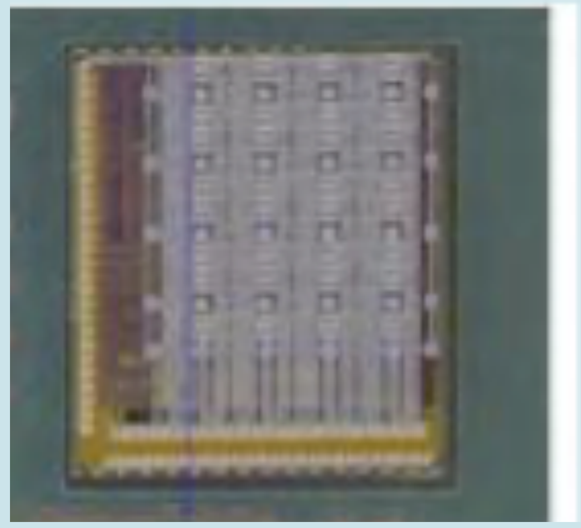
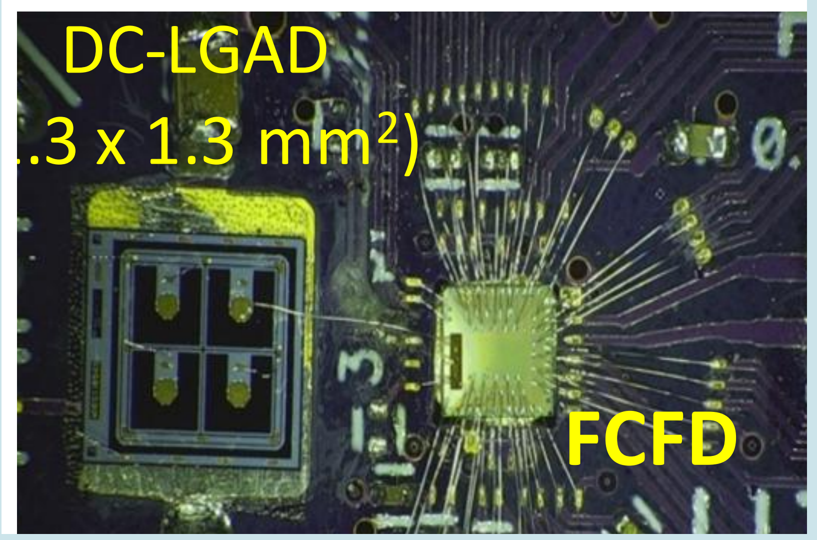
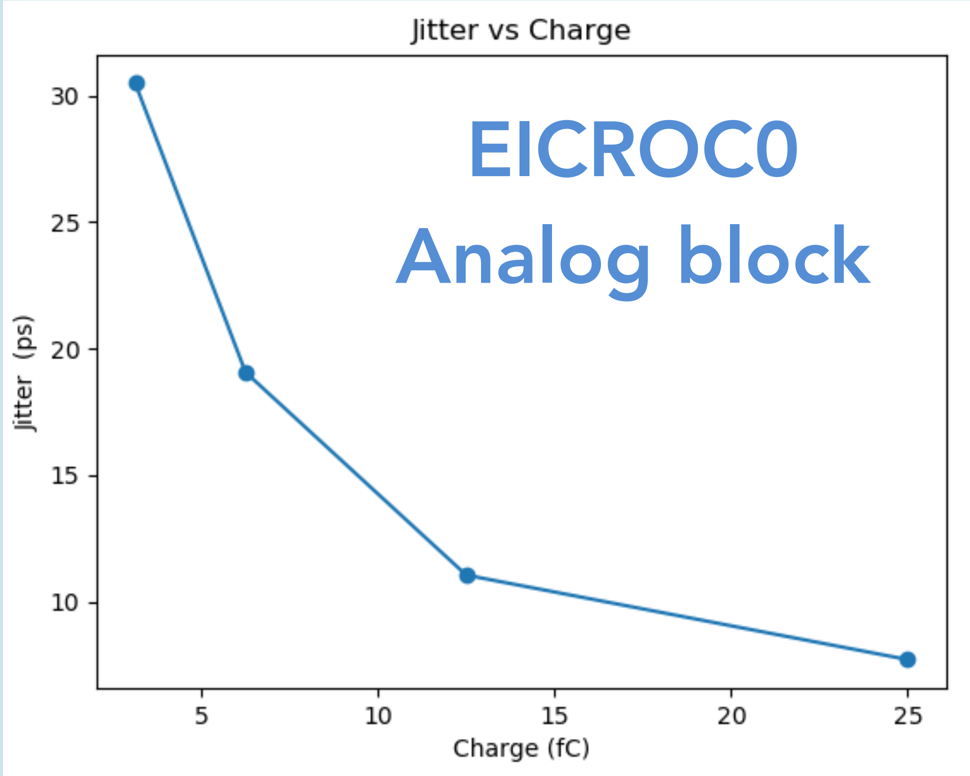
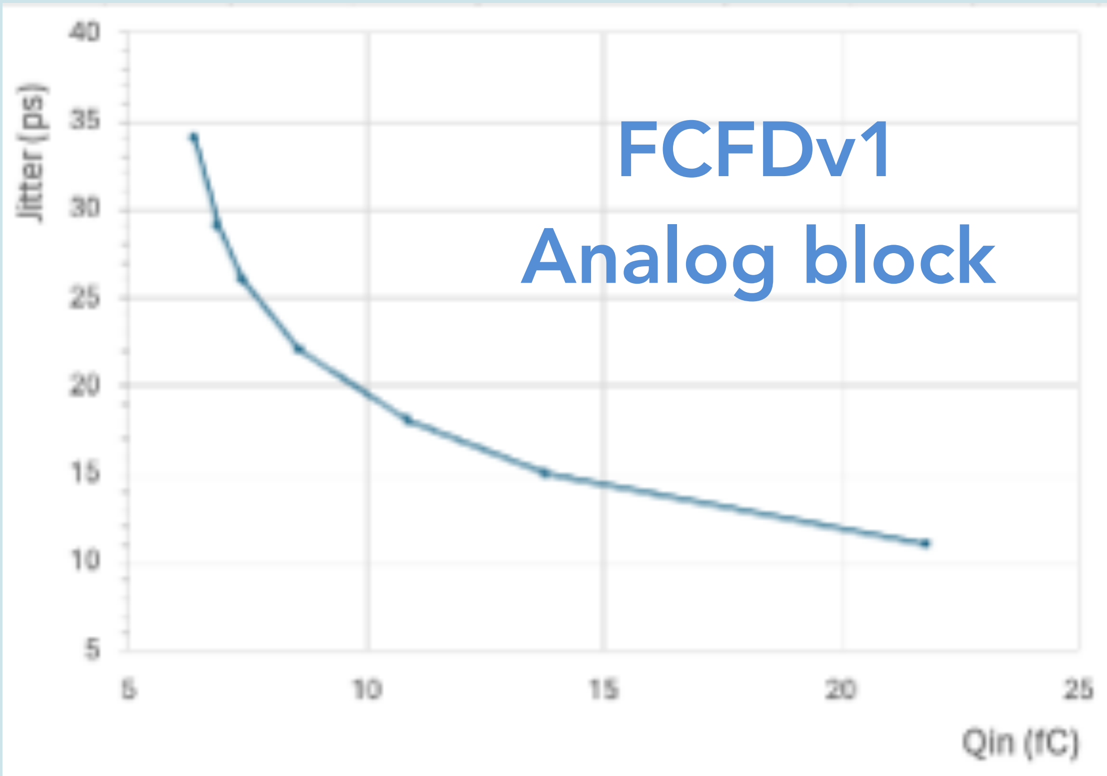


FCFDv1



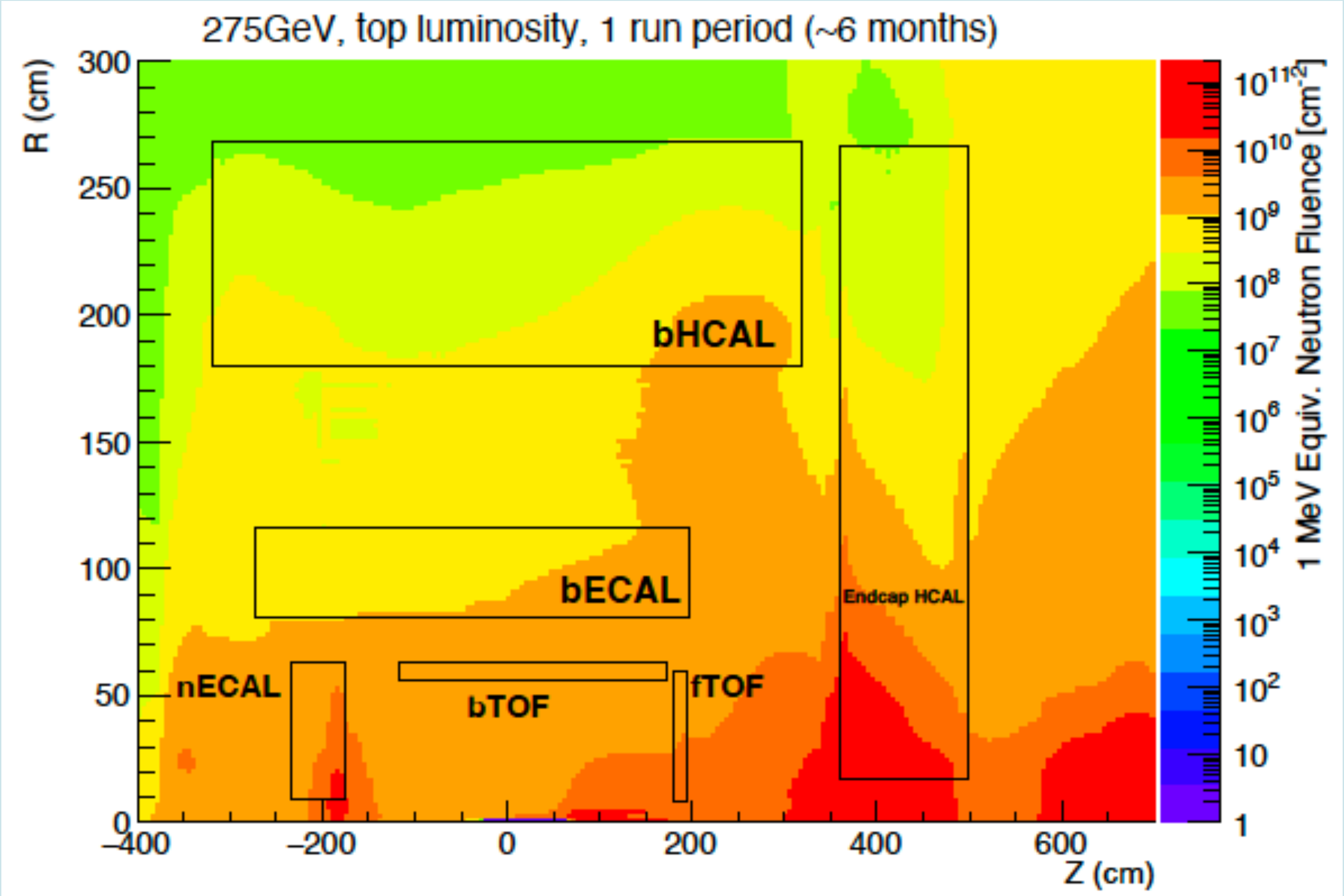
HGCROC3





Sensor irradiation test

- Not very large radiation is expected at both BTOF and FTOF ($10^{9\text{-}10} n_{eq}/cm^2$)



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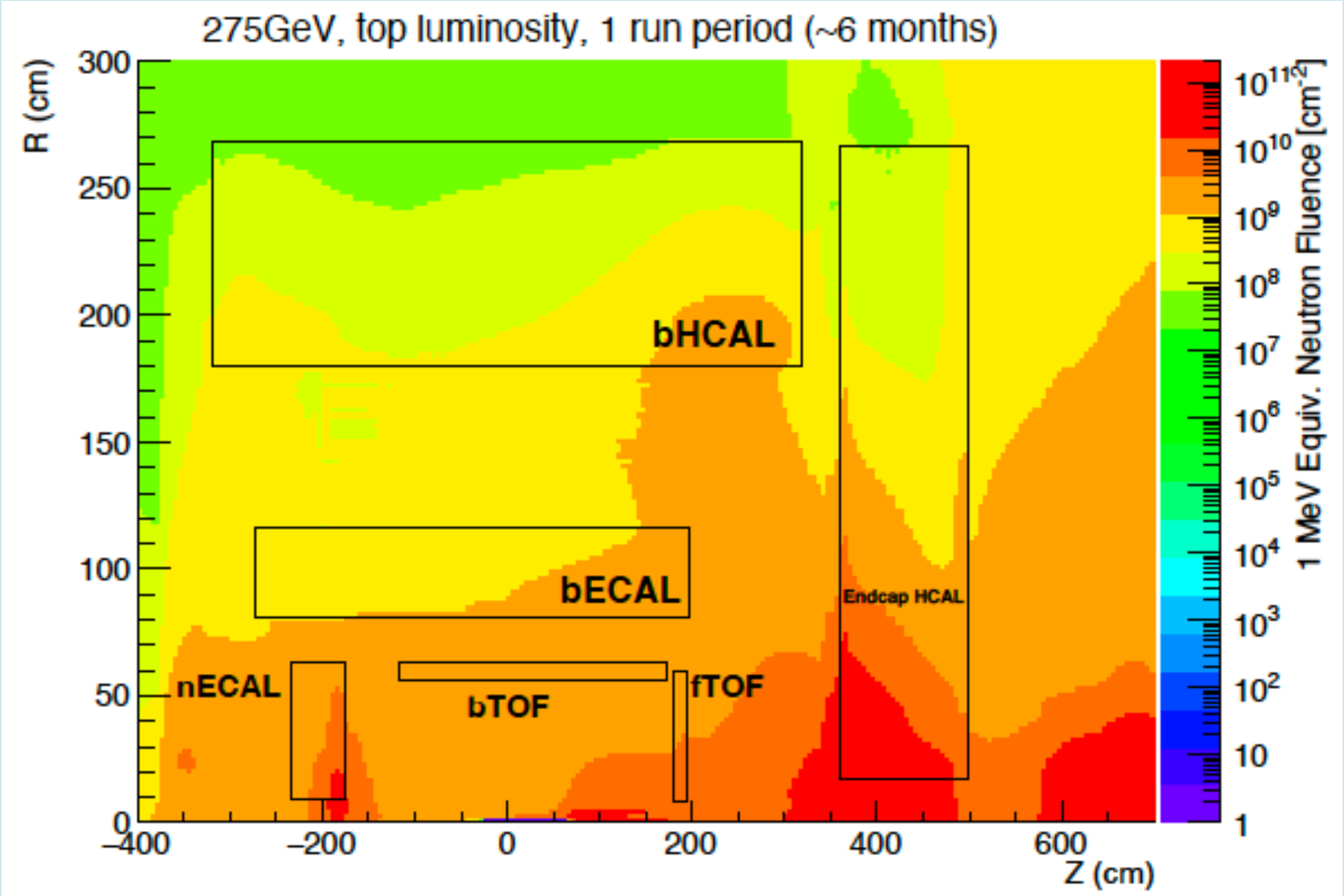
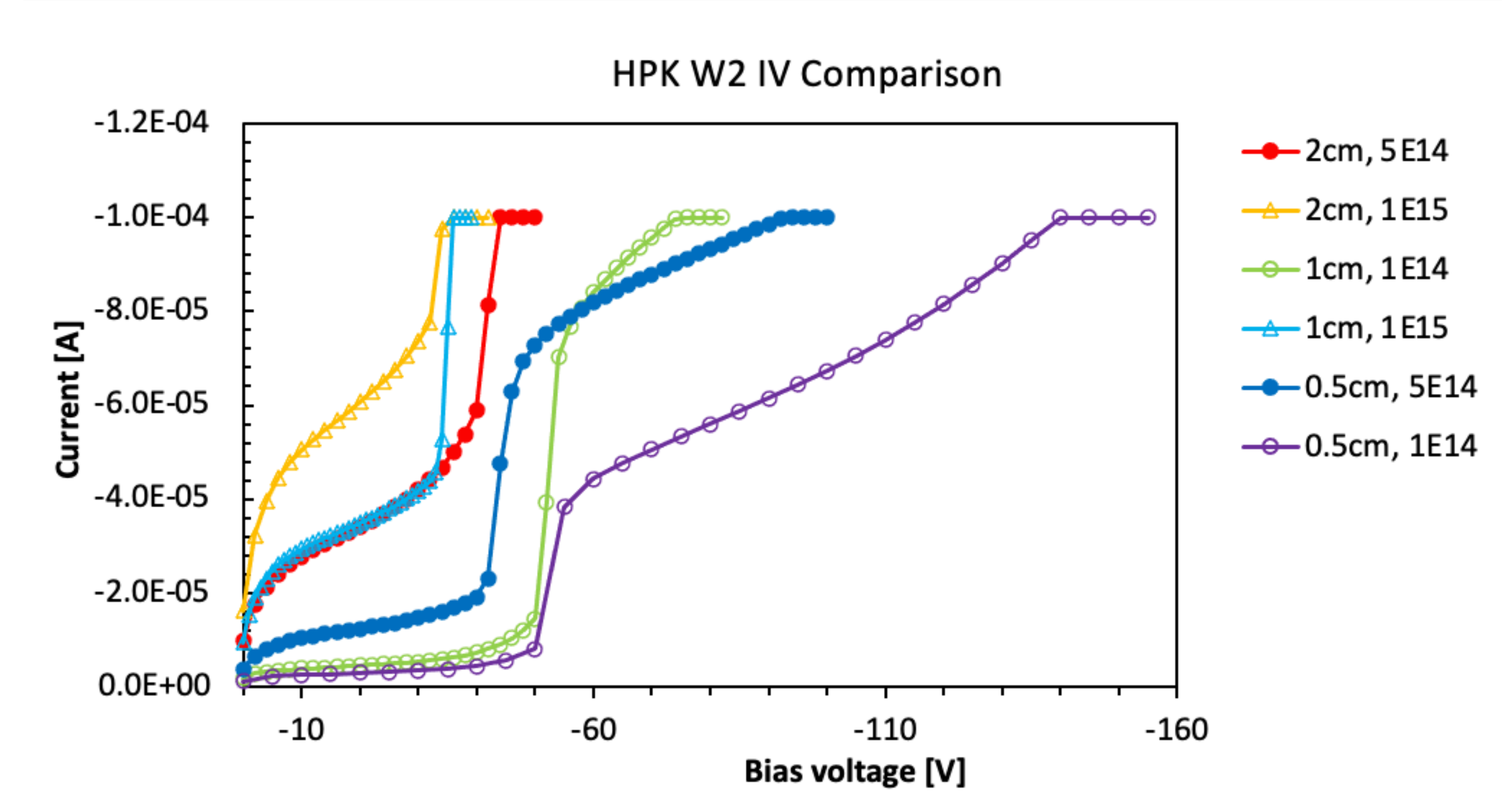
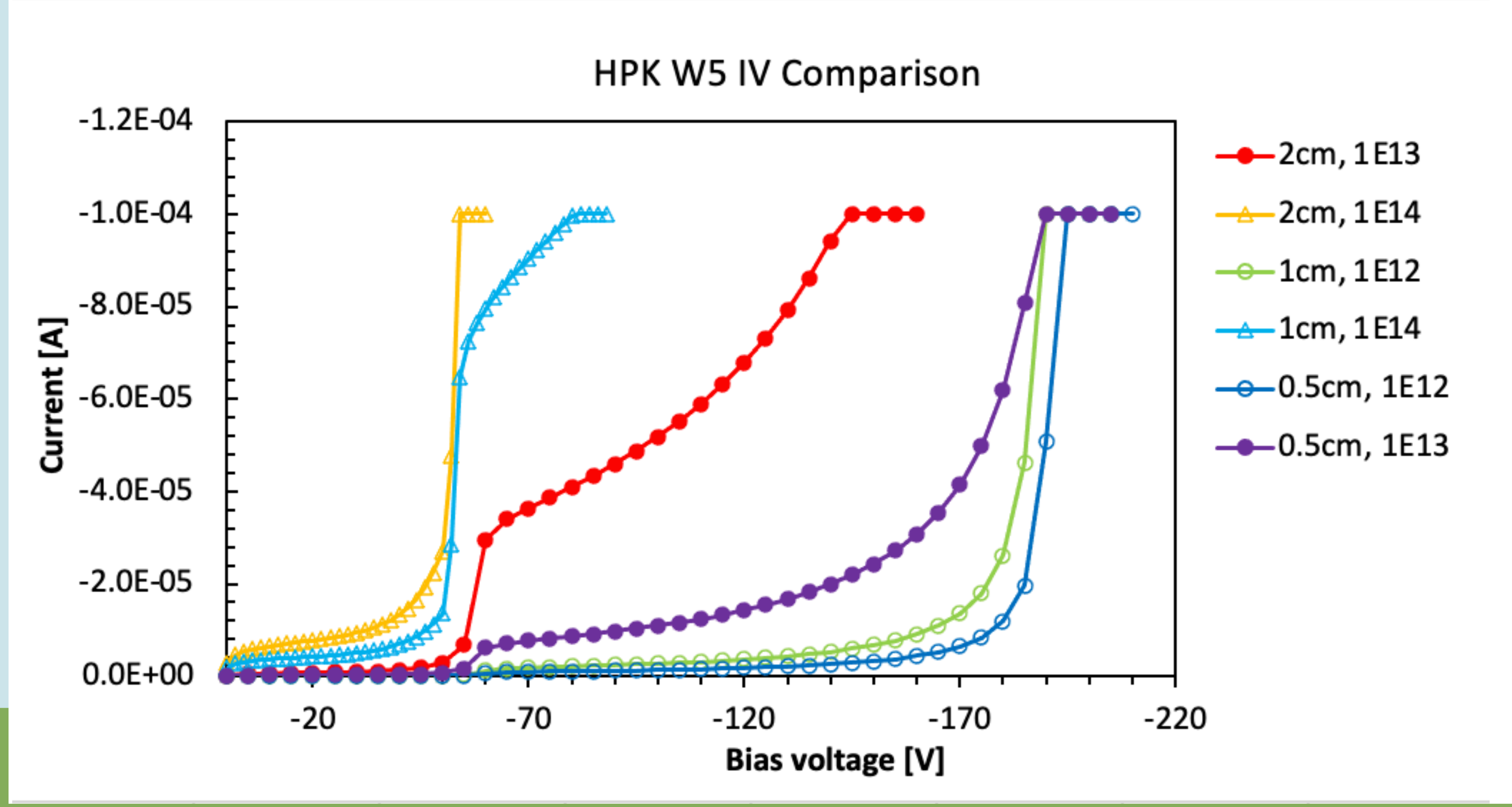
- Not very large radiation is expected at both BTOF and FTOF ($10^{9\text{-}10} n_{eq}/cm^2$)
- Irradiation test of strip sensor has been done at IJS with 1 MeV neutron
- All devices were annealed for 80 min at 60°C to avoid rapid change in sensor behavior
- Testing done at room temperature with a probe station, the current is higher for high irradiation devices
- The irradiation effects should be corrected in the experiment







Support structure and temperature control

- BTOF consists of long staves with a lower material support structure than ever before

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sPHENIX INTT FPC

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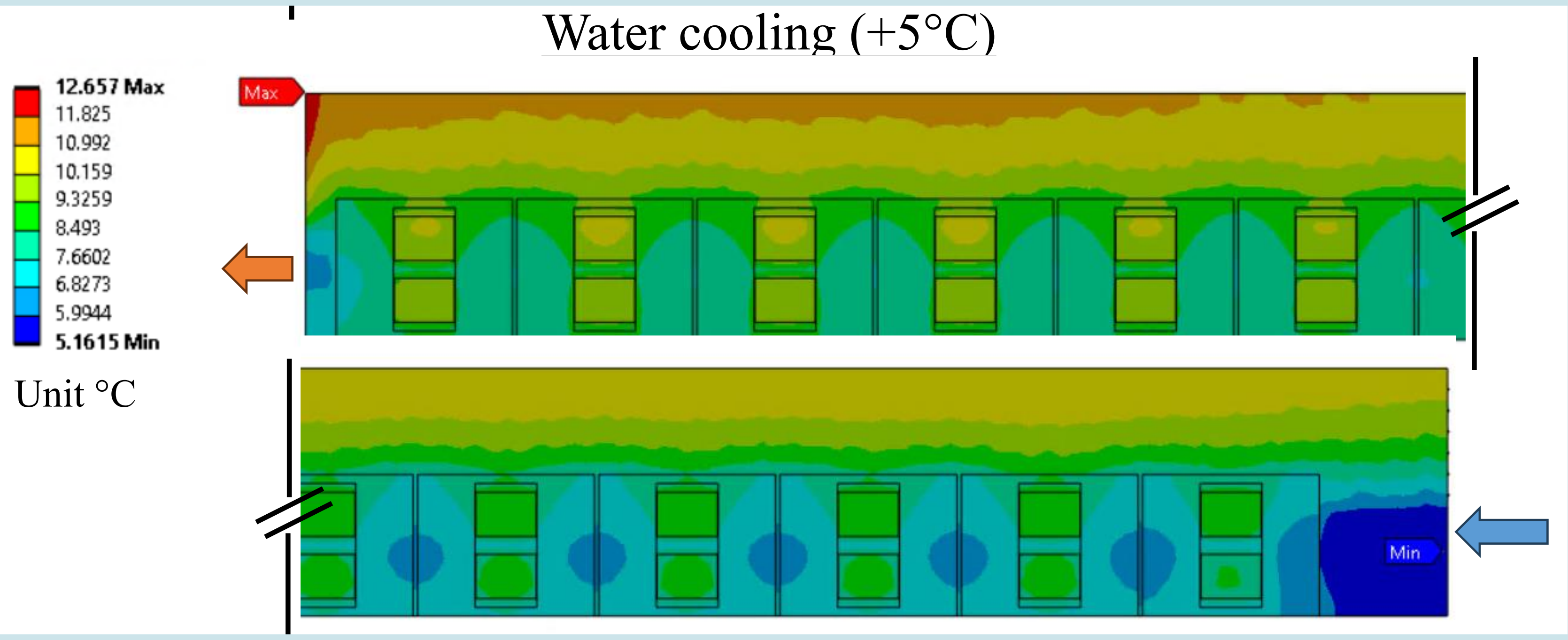
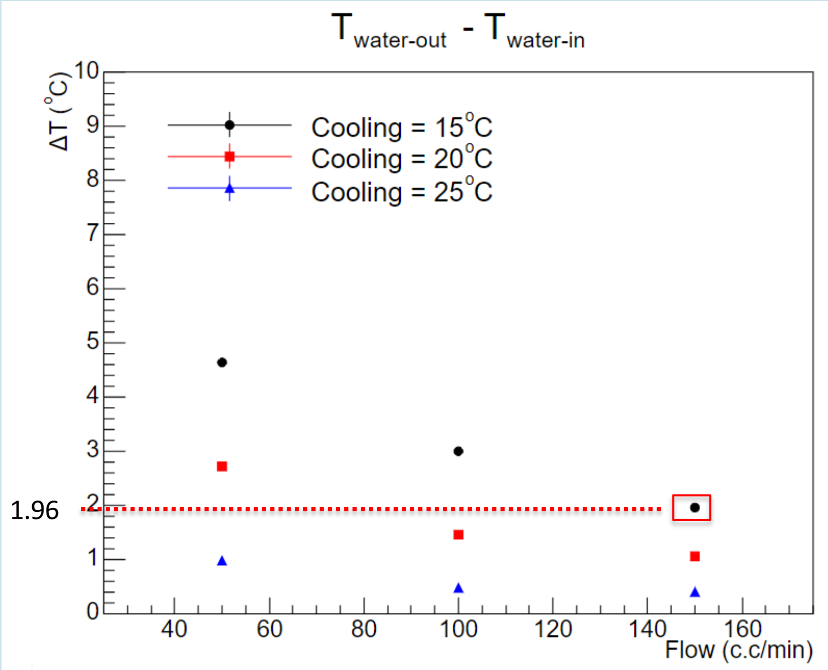
- The thermal conductivity of the stave is under investigation
  - Full-size stave (270 cm) thermal conductivity is being studied with simulation
  - Mini-size support structure (30 cm) thermal conductivity is being studied under several conditions
  - Middle-size support structure (100 cm) is available now and the results will be out soon

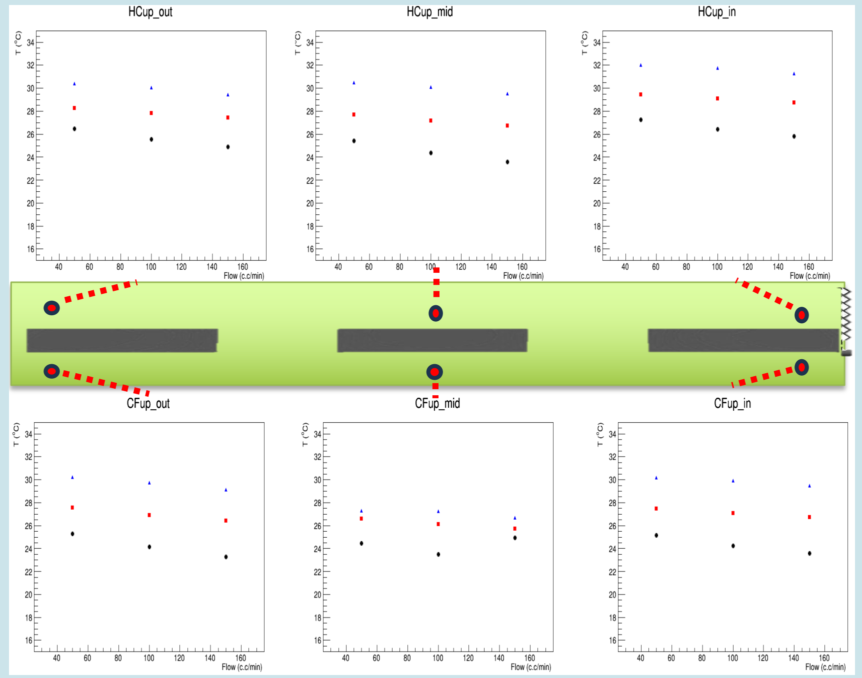
sPHENIX INTT FPC

Full-size stave test with simulation



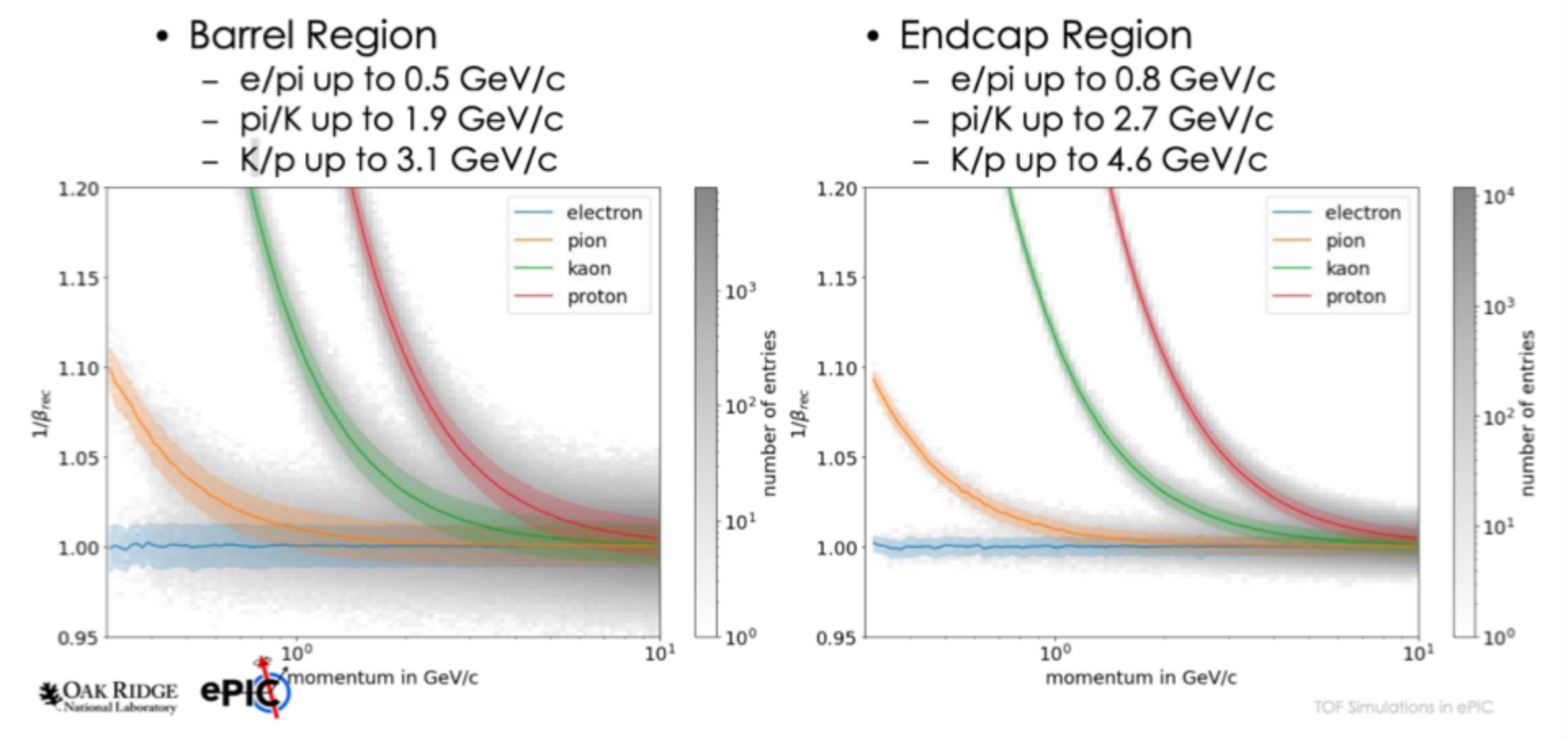
Mini-size stave test results





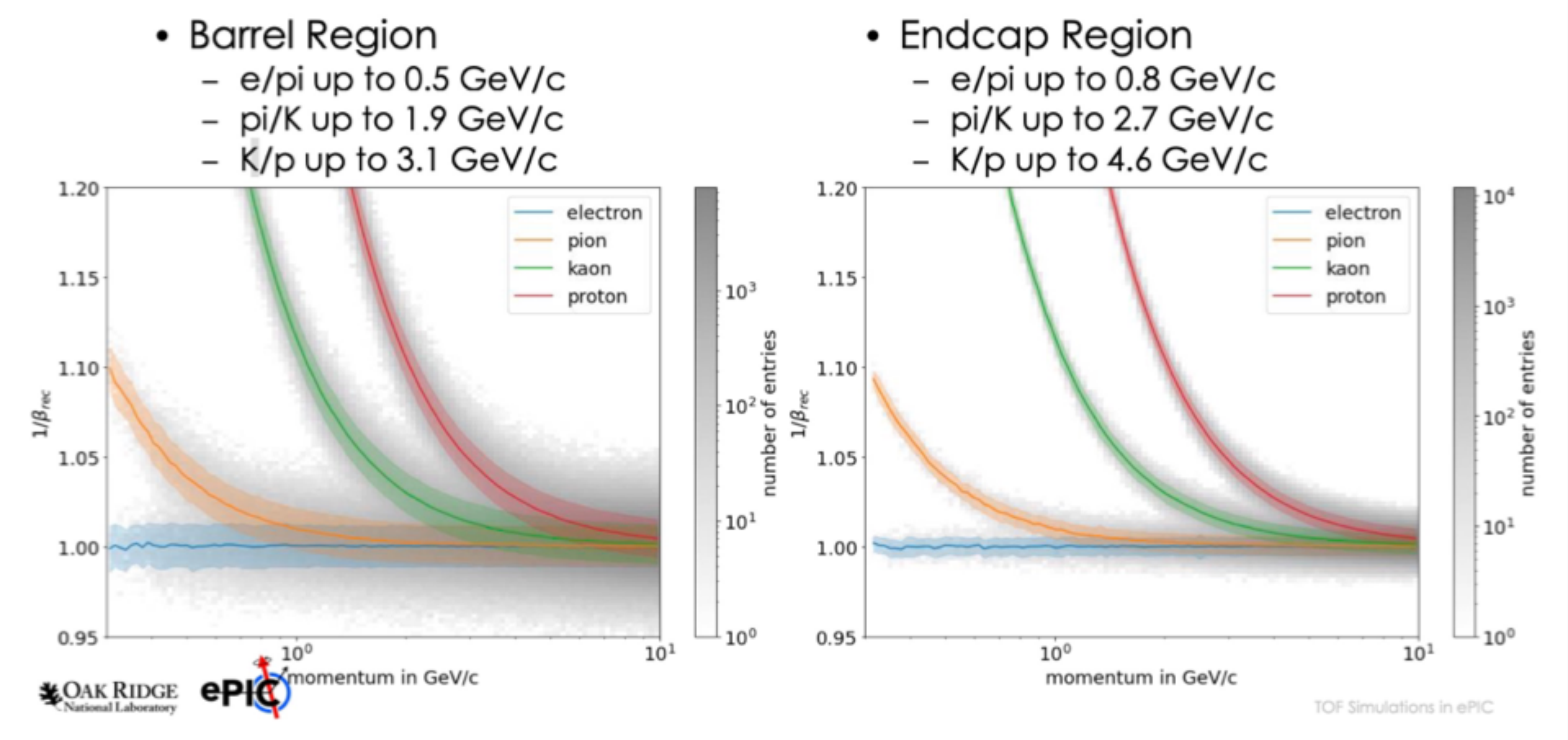
Simulation development

- The LUT PID has been implemented into the official simulation

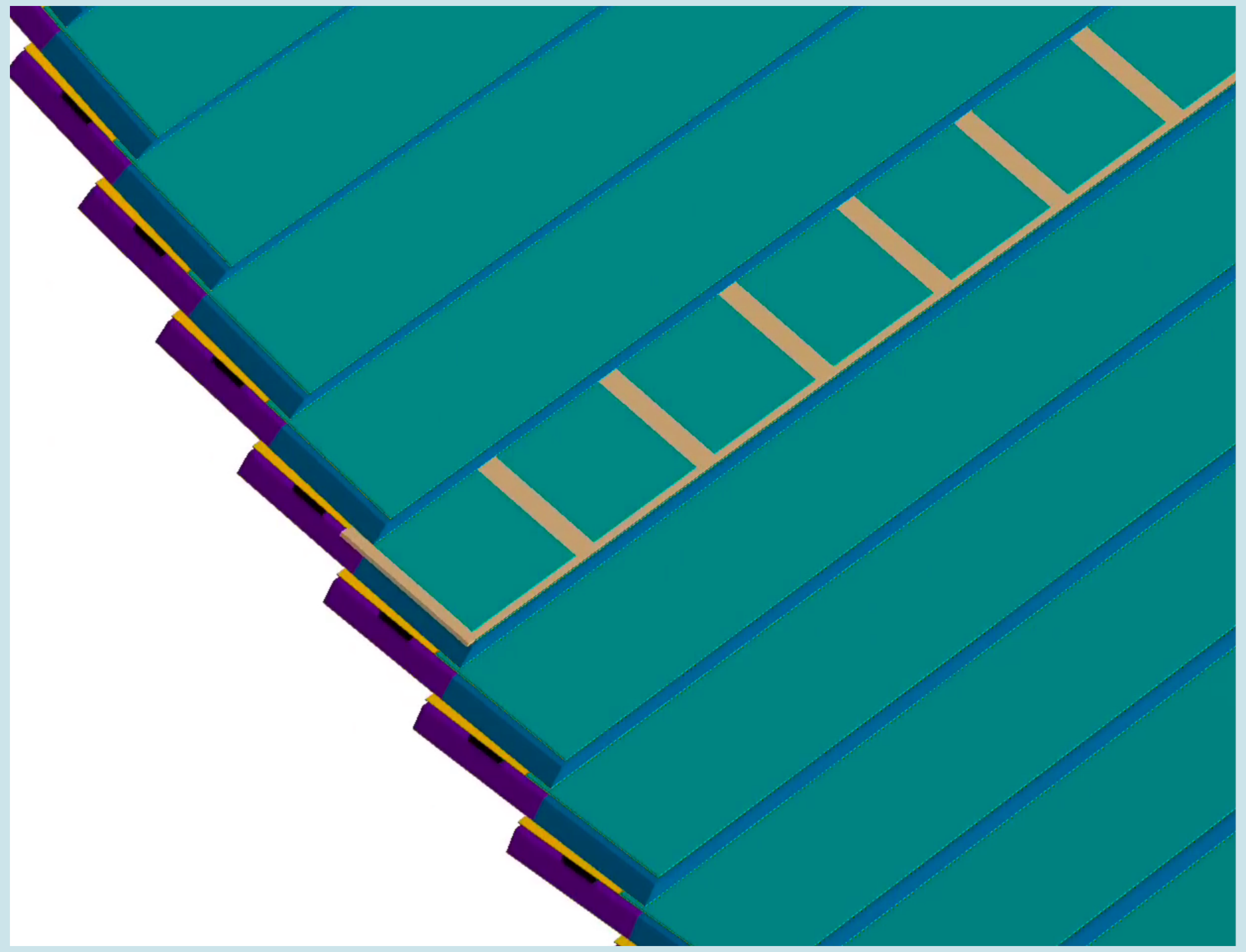


Simulation development

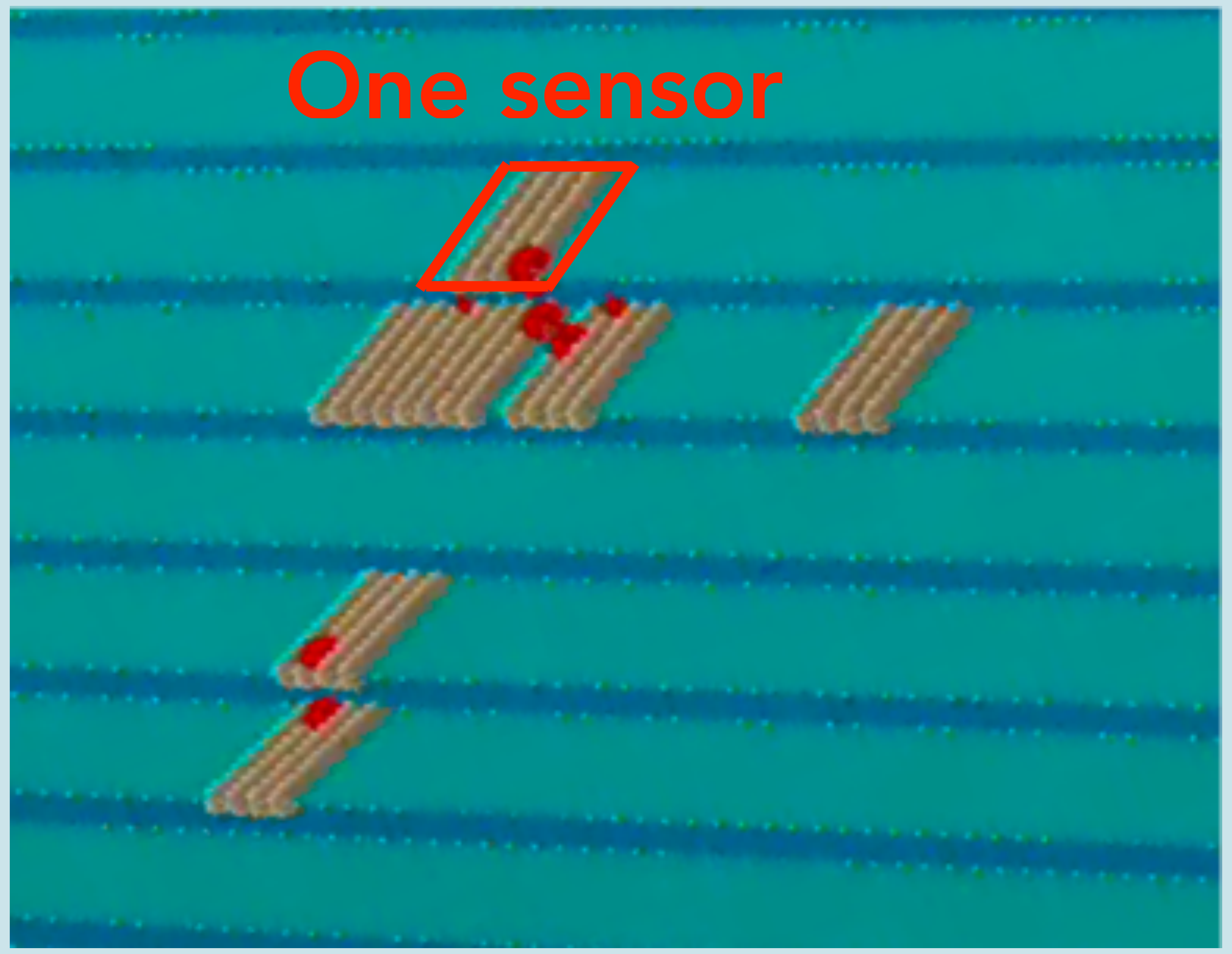
- The LUT PID has been implemented into the official simulation
- More realistic sensor segmentation is being implemented in the simulation



Sensor segment

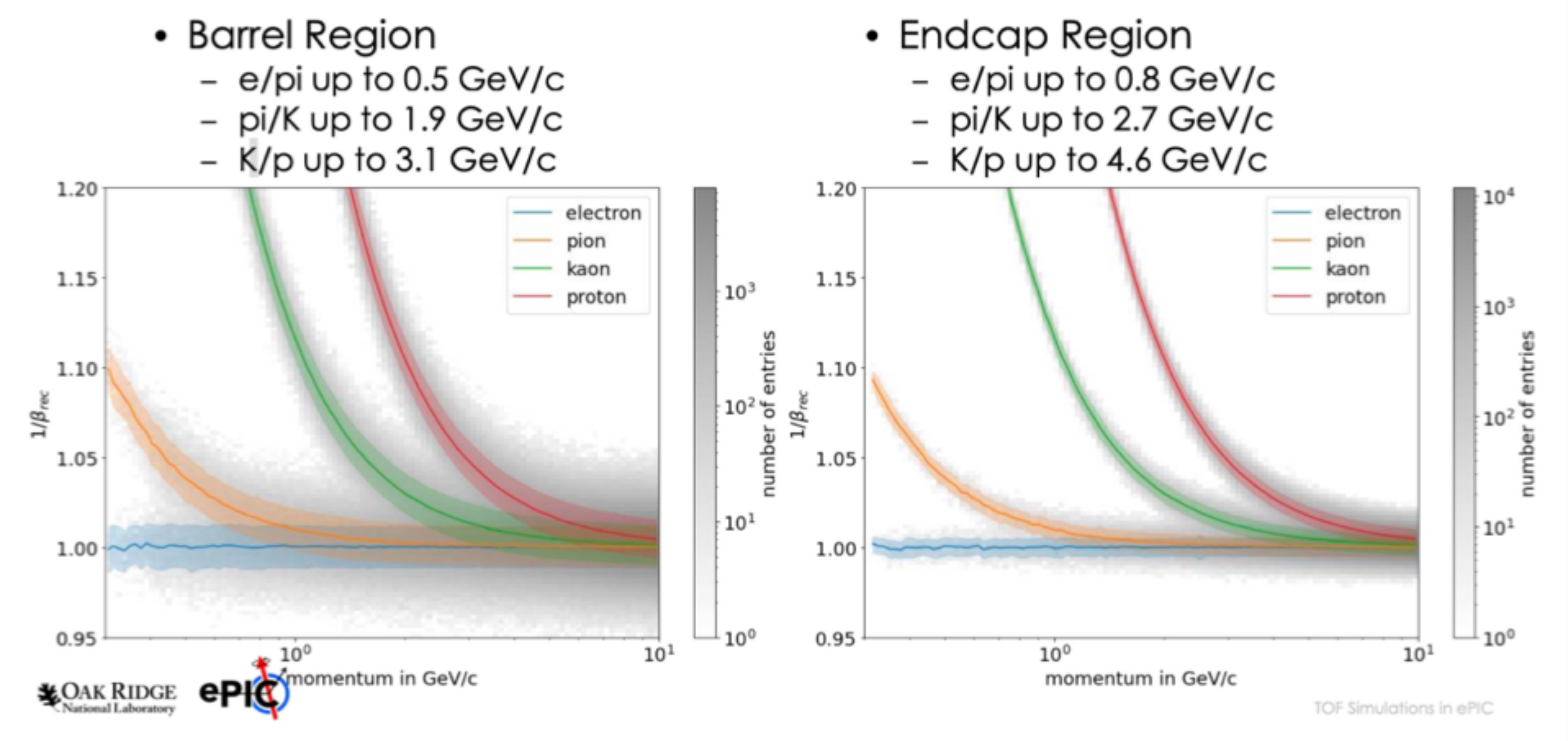


Readout metal visualization



Simulation development

- The LUT PID has been implemented into the official simulation
- More realistic sensor segmentation is being implemented in the simulation
- Digitization mimicking charge sharing has been implemented in the simulation



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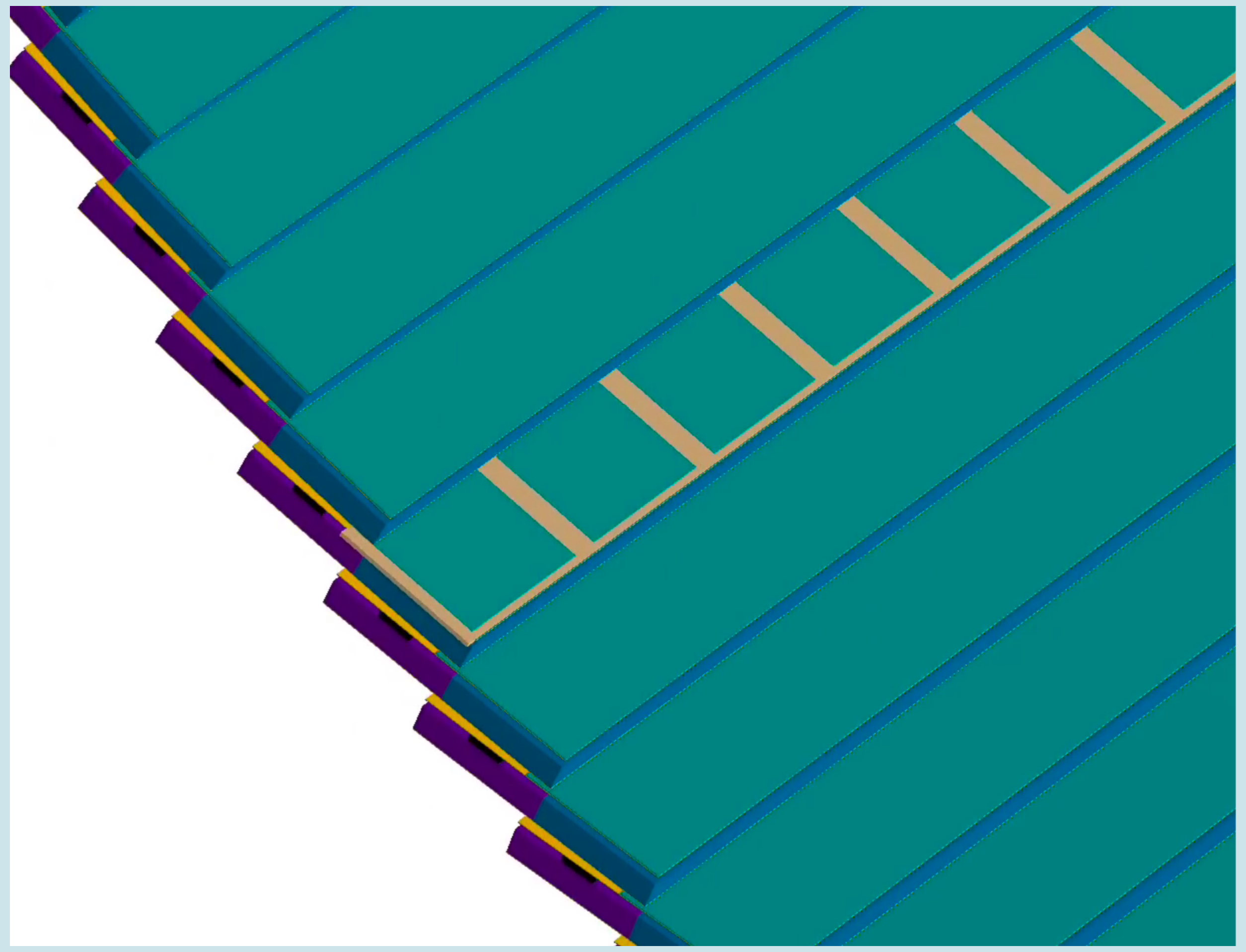

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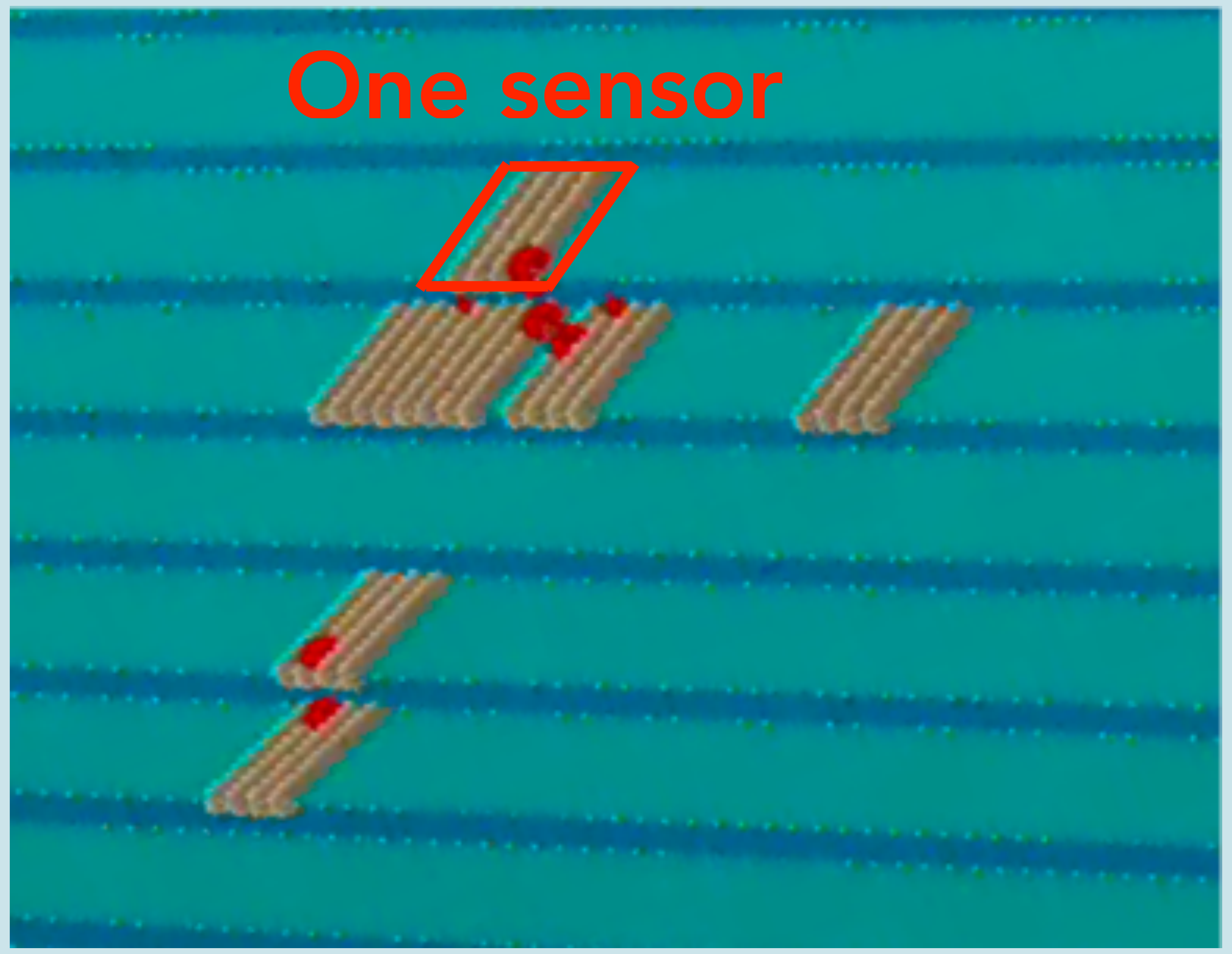
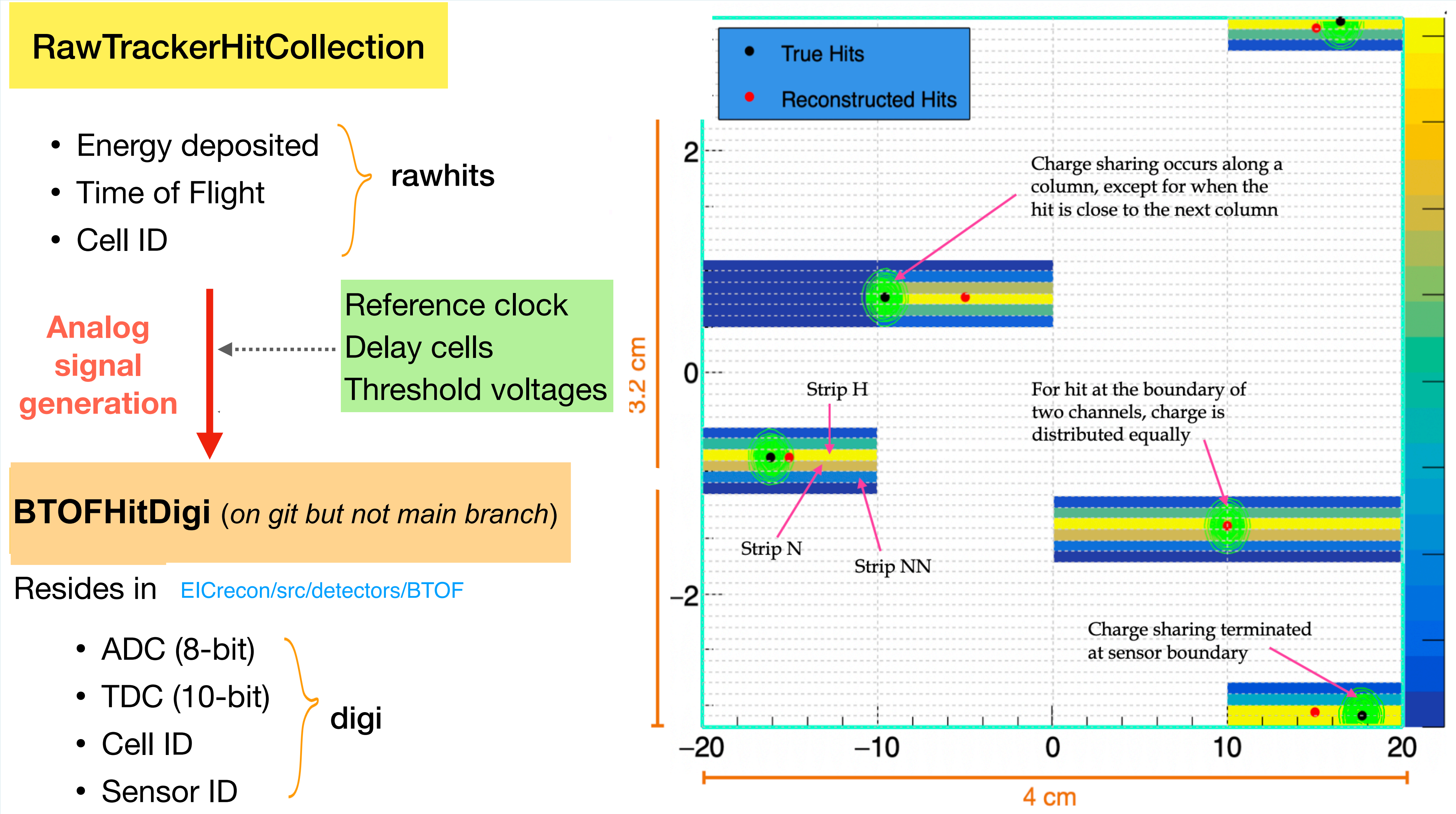
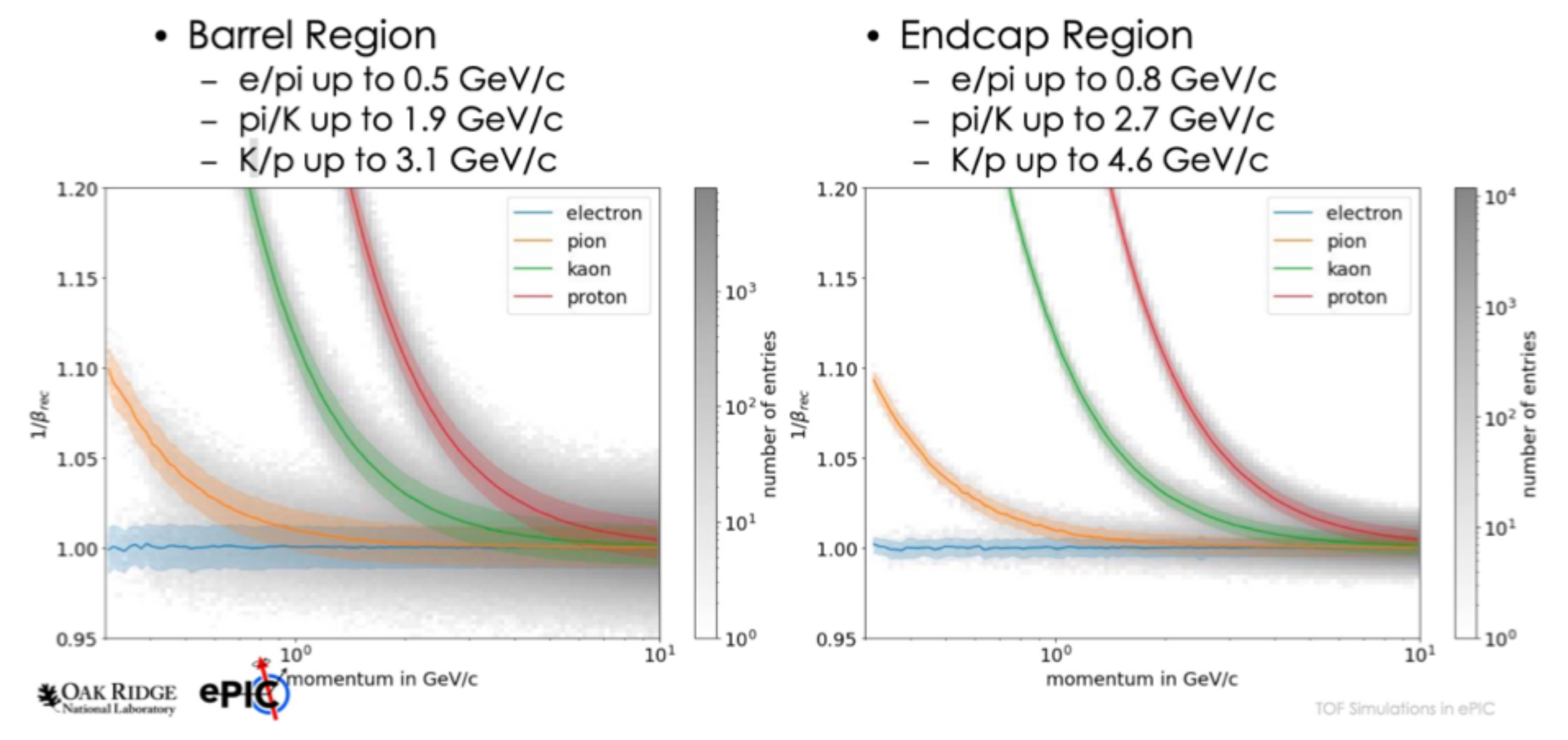


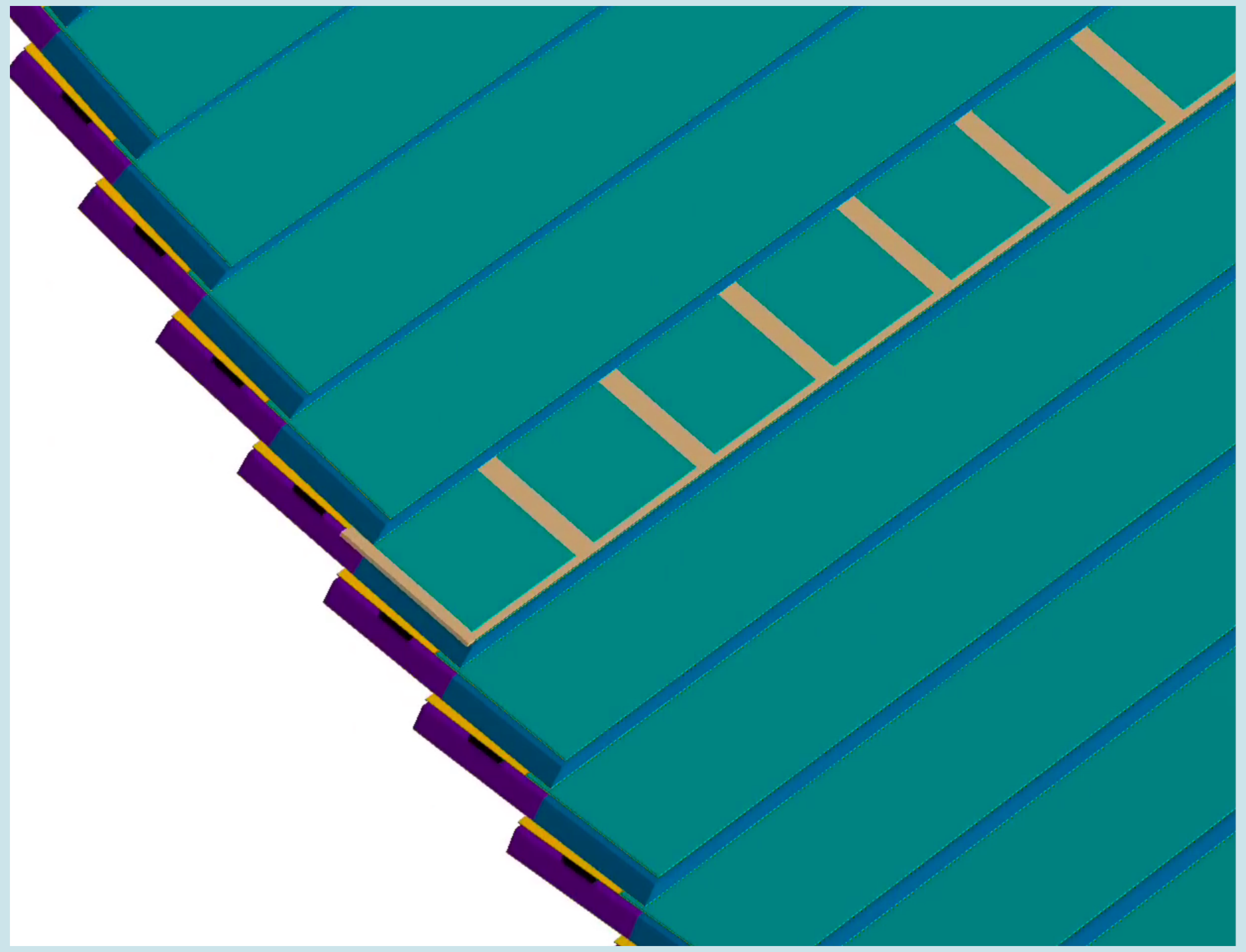


Simulation development

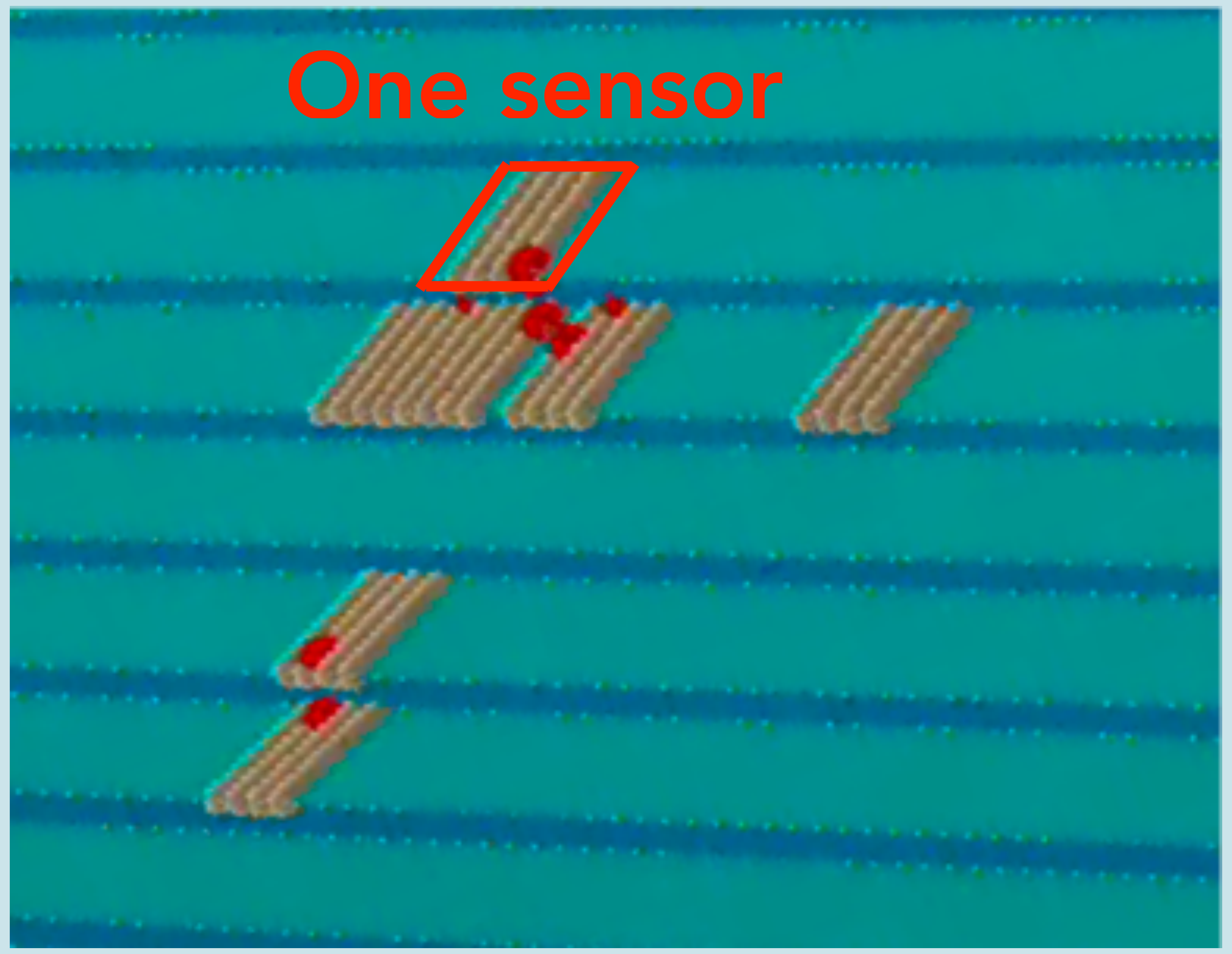
- The LUT PID has been implemented into the official simulation
- More realistic sensor segmentation is being implemented in the simulation
- Digitization mimicking charge sharing has been implemented in the simulation
- Material budget effect on the outer detectors by BTOF is under evaluation

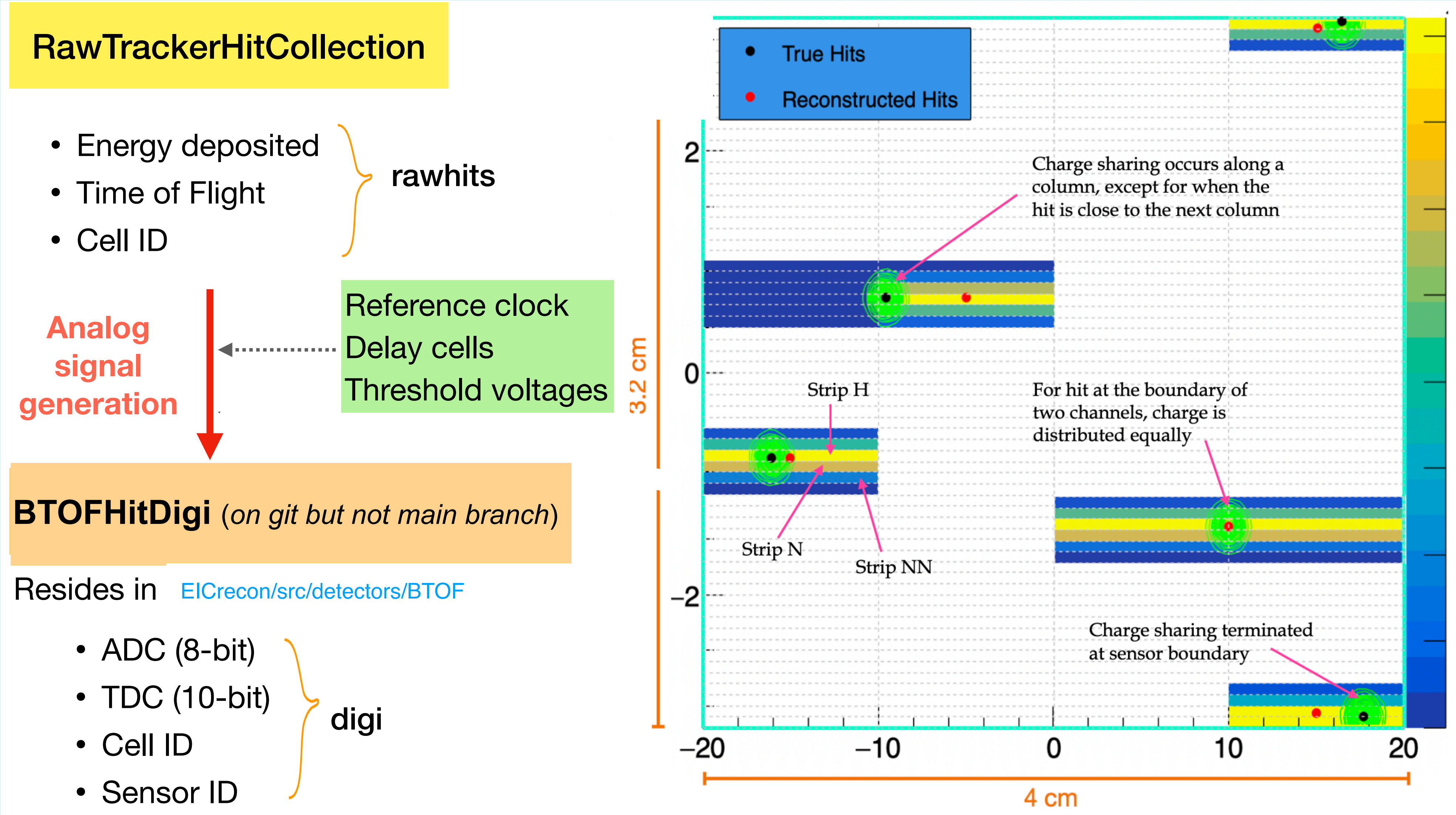


Sensor segment



Readout metal visualization

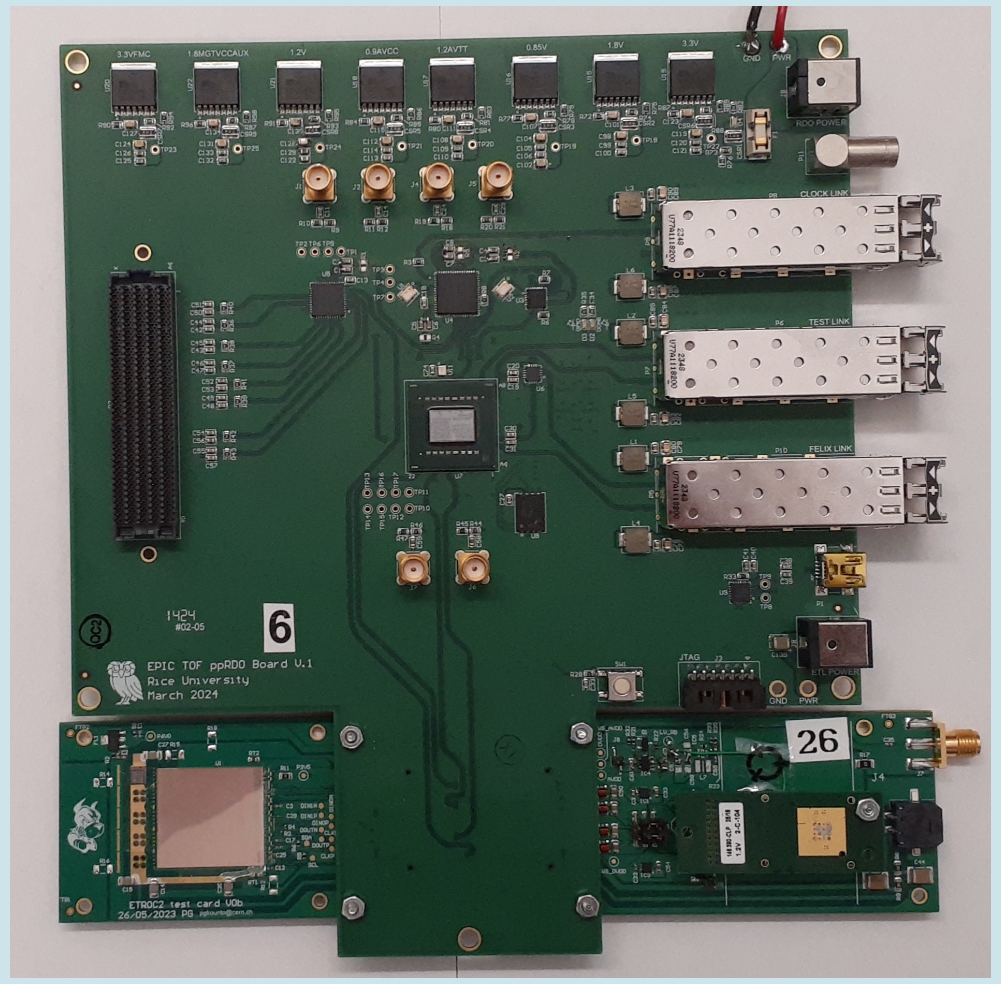




Front-end electronics

- Pre-prototype readout board (ppRDO) has been made with ETROC2 ASIC
  - 6 boards are available
- Several tests are ongoing
  - FPGA firmware development
  - Readout test with ETROC2
  - Evaluation of power consumption

ppRDO



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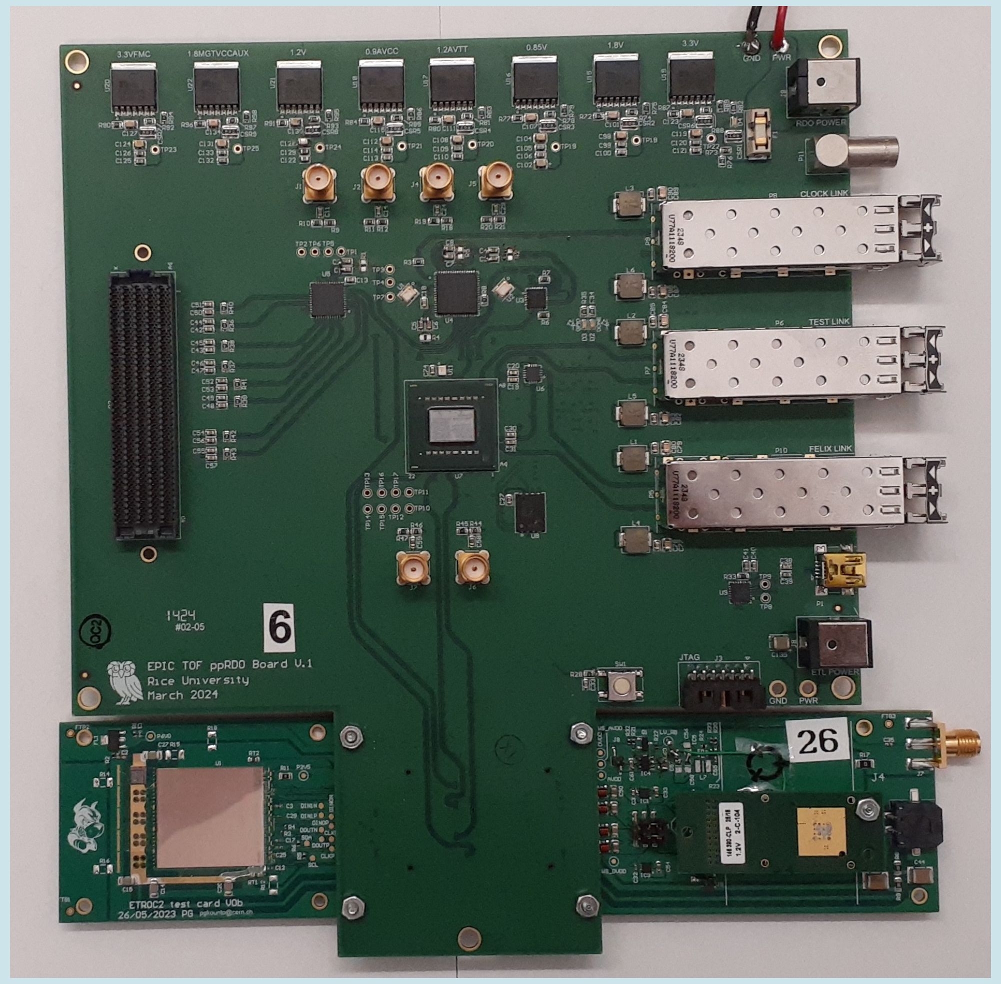
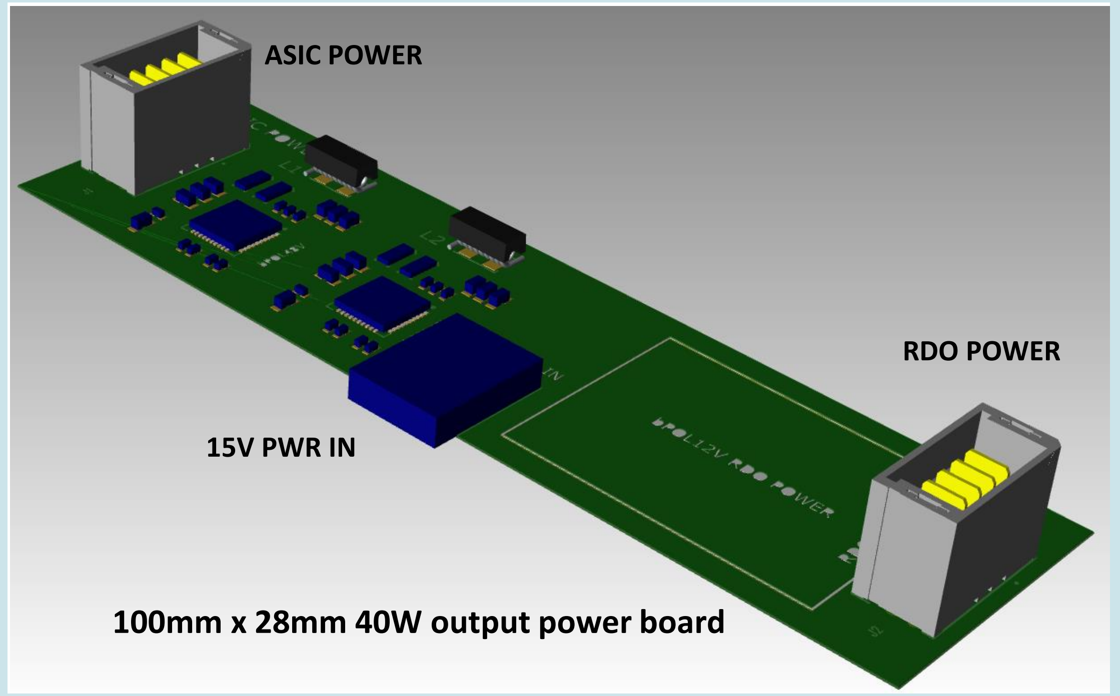
- Power board (PB) design is ongoing
  - PB supplies 5 different voltages
    - ASIC: 1.2 V (EICROC case)
    - FPGA: 1.8, 1.2, 0.9, 0.85 V
    - SFP+: 3.3 V
  - Several options for DC-DC converters are being tested

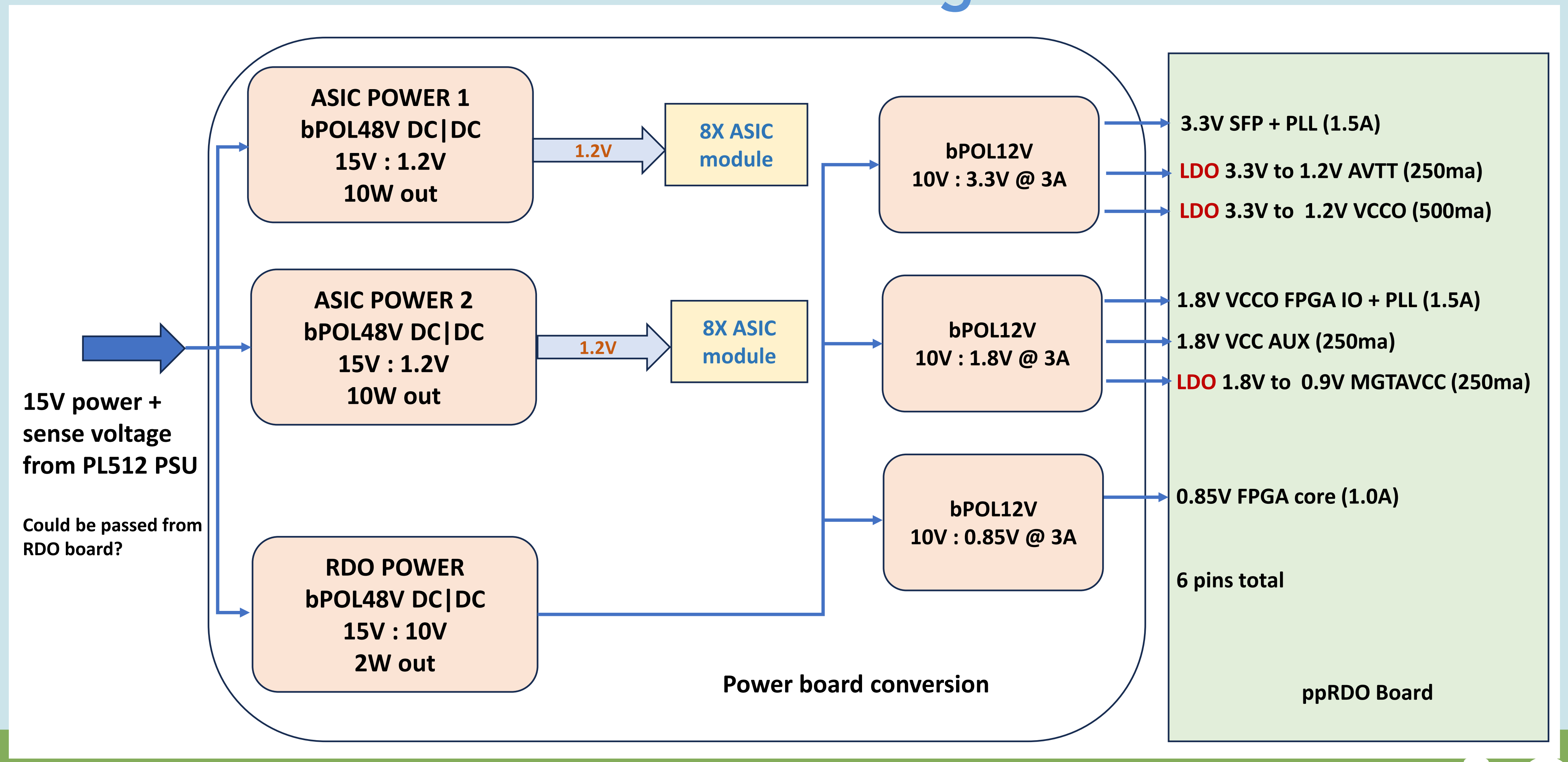
ppRDO



PB design



Power distribution design for FTOF



Summary

- AC-LGAD TOF is the key detector in the ePIC project for the PID at low *p* region and background rejection

- Prototypes of BNL and HPK fulfill the requirements, but it is under the BEST environment
  - Breakdown voltage is expected to depend on the temperature strongly
  - Performance redundancy should be considered
  - The first irradiation test with strip sensors has been done

- ASIC analog part performance of EICROC and FCFD meet the requirement
  - Not only ASIC but also AC-LGAD sensor + ASIC performance must be evaluated in the coming year

- Support structure thermal properties are being investigated with a 30 cm-long prototype
  - The first 100 cm prototype will be tested soon

- The prototype RDO is available and being tested with ETROC2

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TOF project is making steady progress!

Backup slides

Institutes in TOF tasks (official)

- Brookhaven National Laboratory (USA)
- Fermi National Accelerator Laboratory (USA)
- Rice University (USA)
- Oak Ridge National Laboratory (USA)
- Ohio State University (USA)
- Purdue University (USA)
- University of California Santa Cruz (USA)
- University of Illinois at Chicago (USA)
- Hiroshima University (JP)
- RIKEN (JP)
- Shinshu University (JP)
- Nara Woman University (JP)
- National Chen-Kung University (TW)
- National Taiwan University (TW)
- IJCLab, OMEGA, CEA-Saclay (FR)

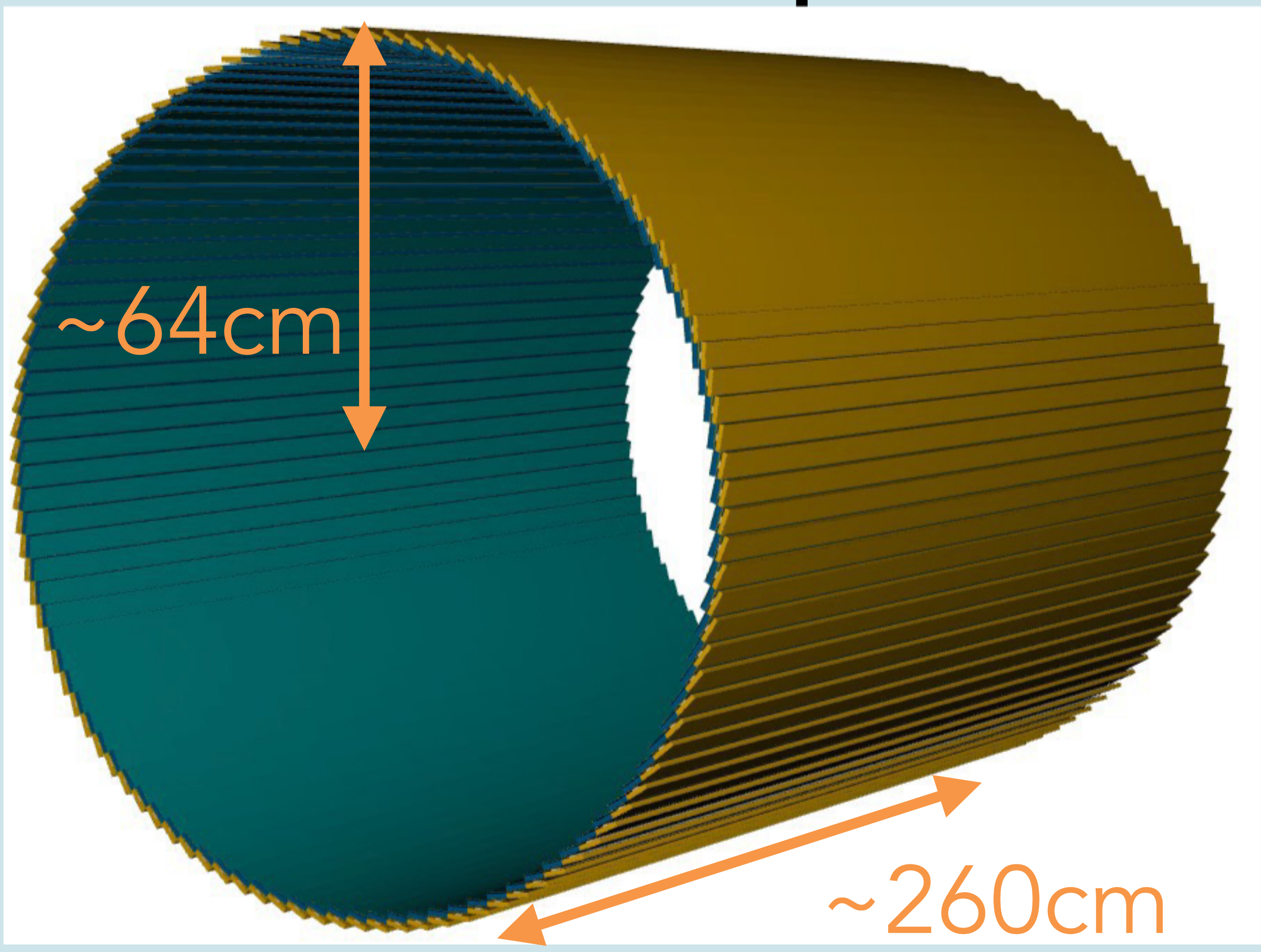
Tasks in BTOF

- **AC-LGAD sensor**
  - BNL
  - ORNL
  - Univ. of California, Santa Cruz
  - Univ. of Illinois, Chicago
  - Hiroshima University
  - Shinshu University
- **Frontend ASIC**
  - Fermilab
  - Rice University
  - ORNL
  - Hiroshima University
  - National Taiwan University
  - IJCLab/OMEGA/CEA-Saclay
- **Sensor-ASIC integration**
  - BNL
  - ORNL
  - Univ. of California, Santa Cruz
  - Univ. of Illinois, Chicago
  - National Taiwan University
- **Module structure**
  - Purdue University
  - National Cheng-Kung University
- **Module assembly**
  - BNL
  - ORNL
  - Ohio State University
  - Univ. of California, Santa Cruz
  - Hiroshima University
  - RIKEN
  - Nara Woman University
  - National Taiwan University
- **Flex PCB**
  - ORNL
  - Nara Woman University
- **Service Hybrid**
  - Rice University
- **Backend electronics**
  - BNL

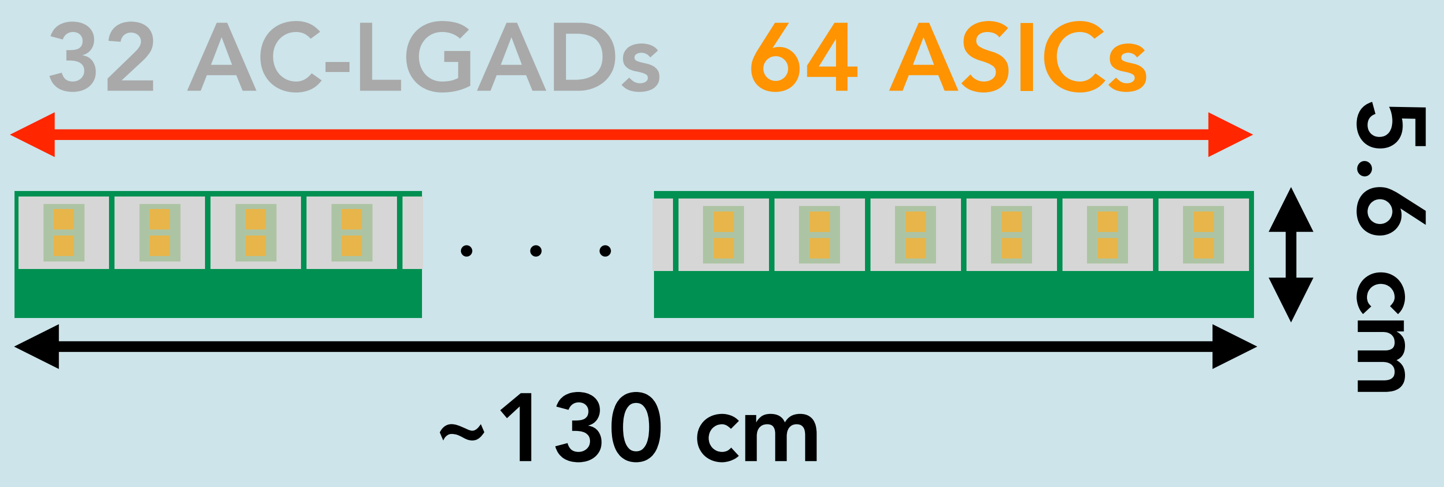
Detector Layout of BTOF

- BTOF is composed of 288 (2x144) staves to form a cylindrical shape
- 32 AC-LGAD **strip-type** sensors are attached to one stave
  - Two ASICs are placed just above one sensor
- Radius is 63 - 66 cm from the beam pipe covering -1.42<η<1.77
- Total material budget in acceptance is ~0.01 X/X_0

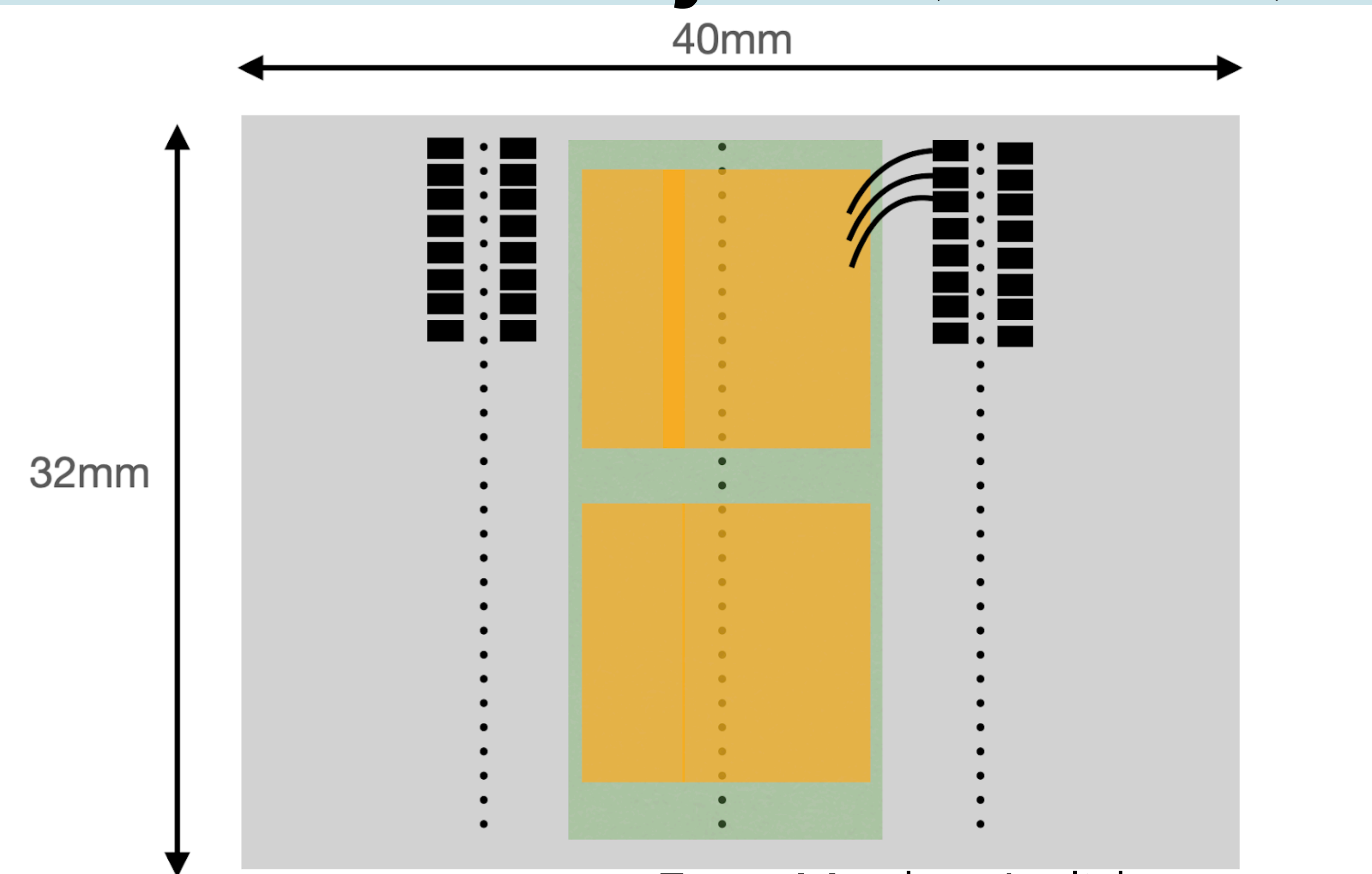
BTOF shape



BTOF Stave

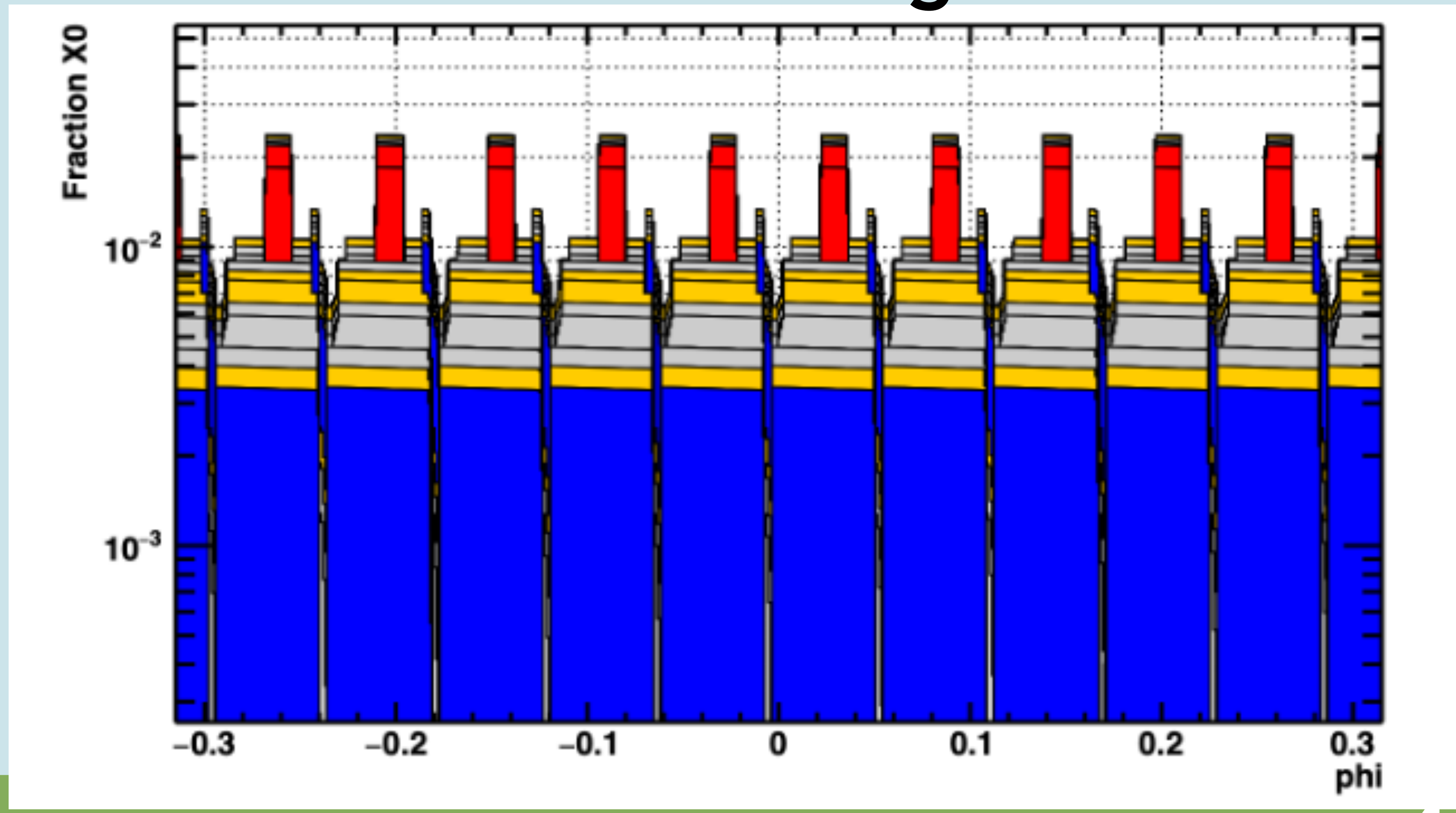


Sensor-ASIC hybrid (module)



From Matthew's slide

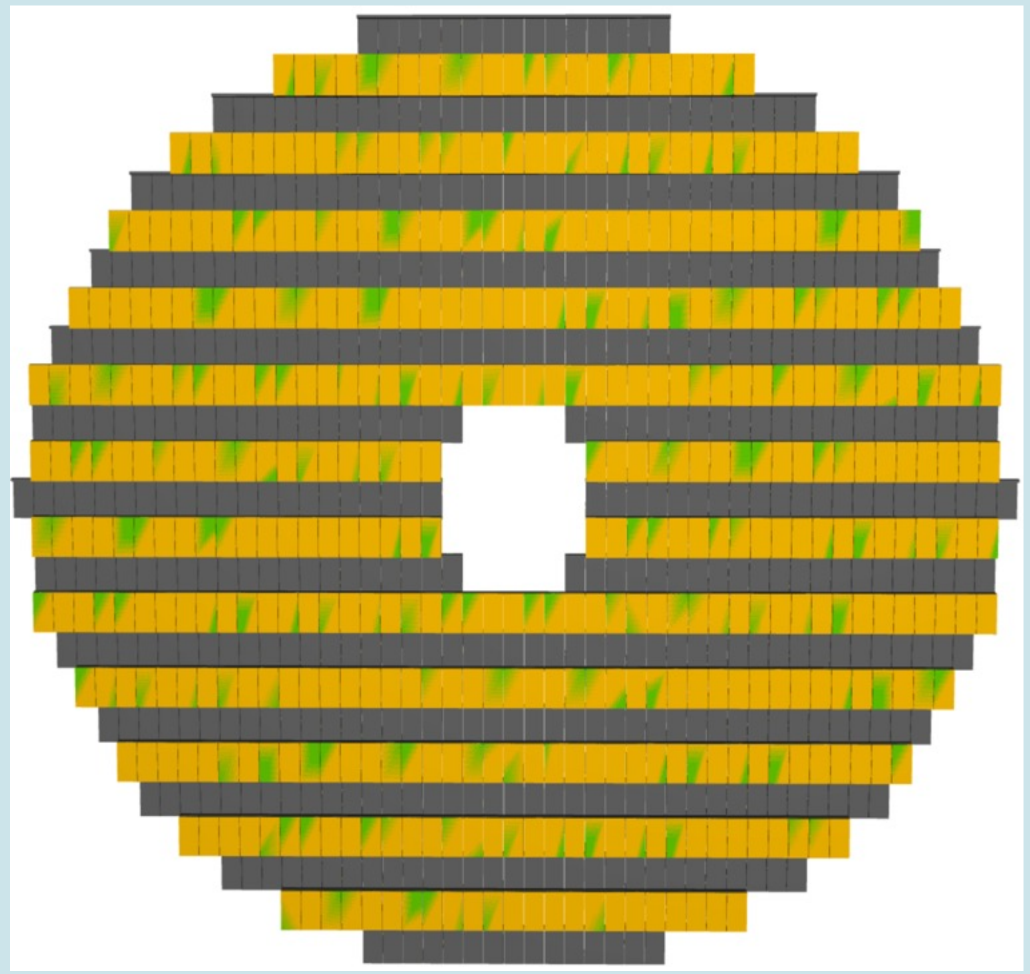
Material budget

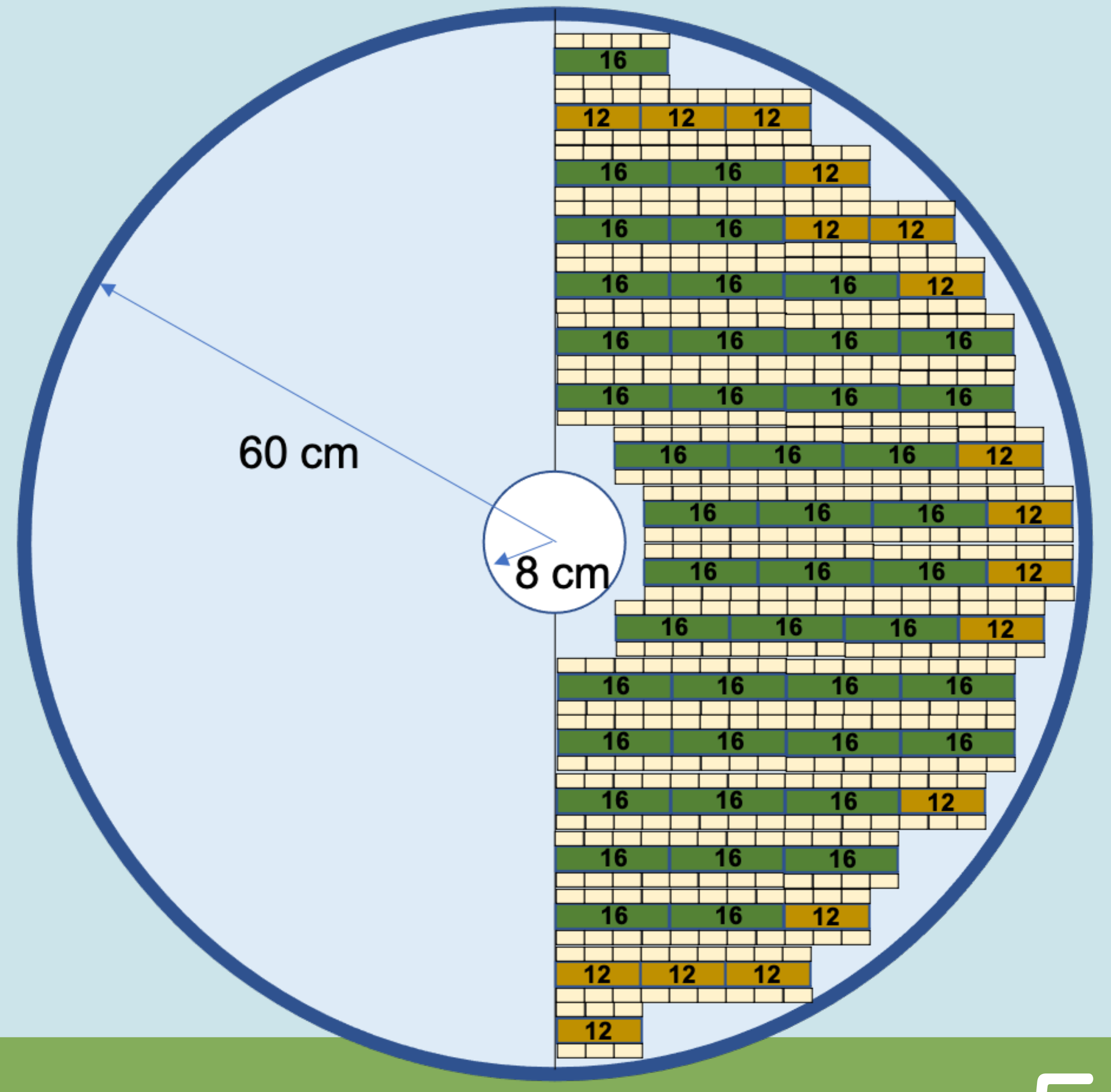


Detector Layout of FTOF

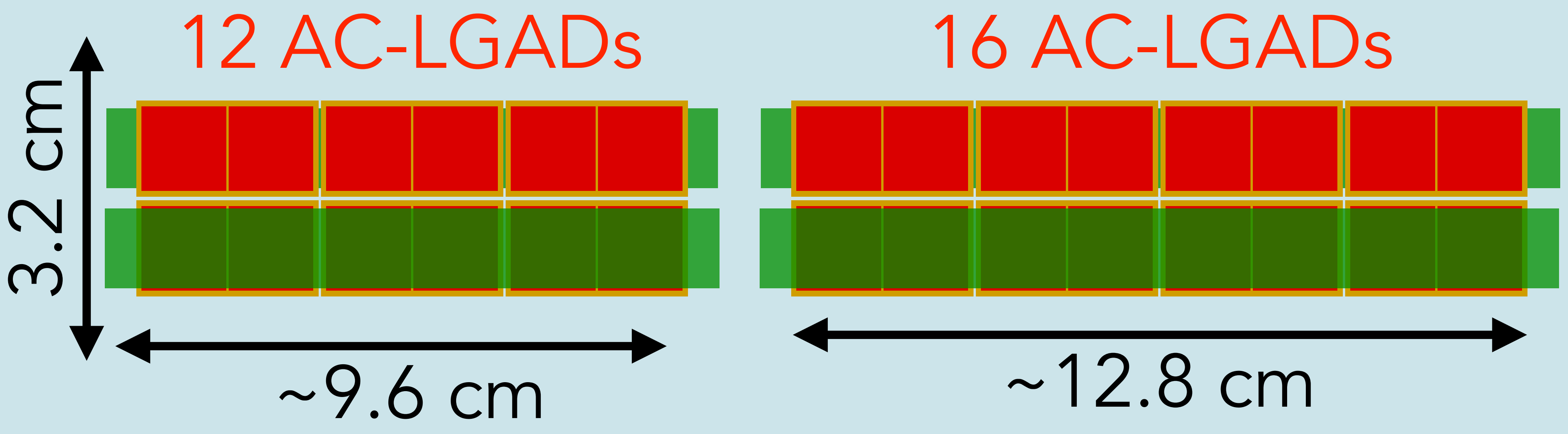
- FTOF is composed of 1816 modules to make a disk
- 12 or 16 AC-LGAD **pixel-type** sensors are attached to one module
  - One ASIC is used for one sensor
- Radius is 10.5 - 60 cm from the beam pipe covering $1.86<\eta<3.85$
- Service hybrid, readout board + power board, is placed in the acceptance
- Total material budget in acceptance is ~0.05 X/X_0

FTOF shape

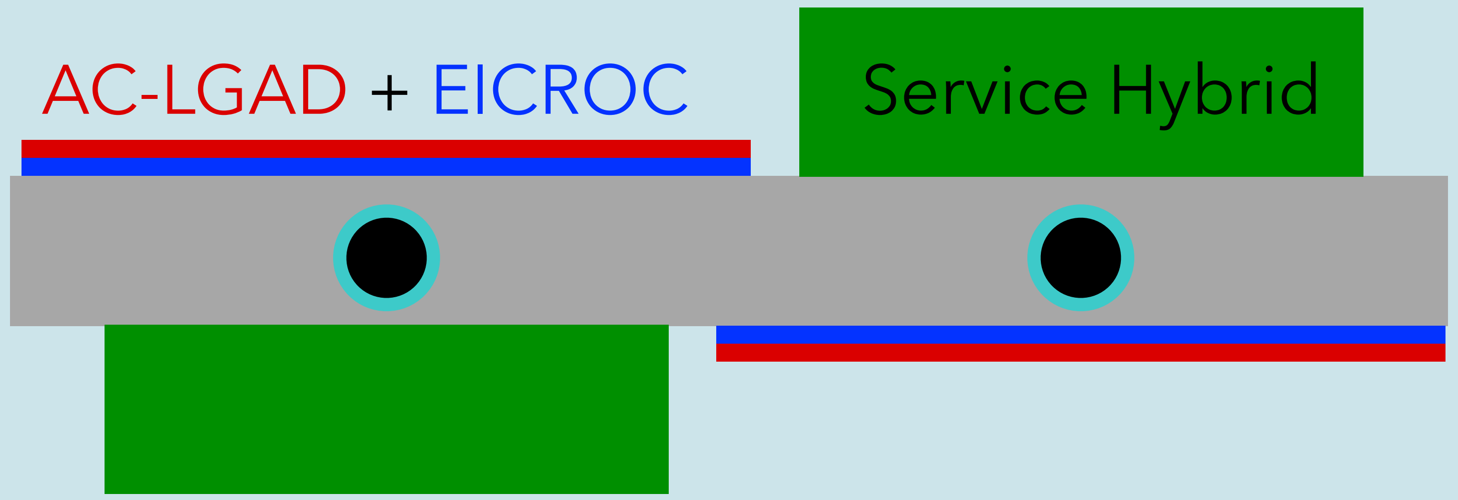




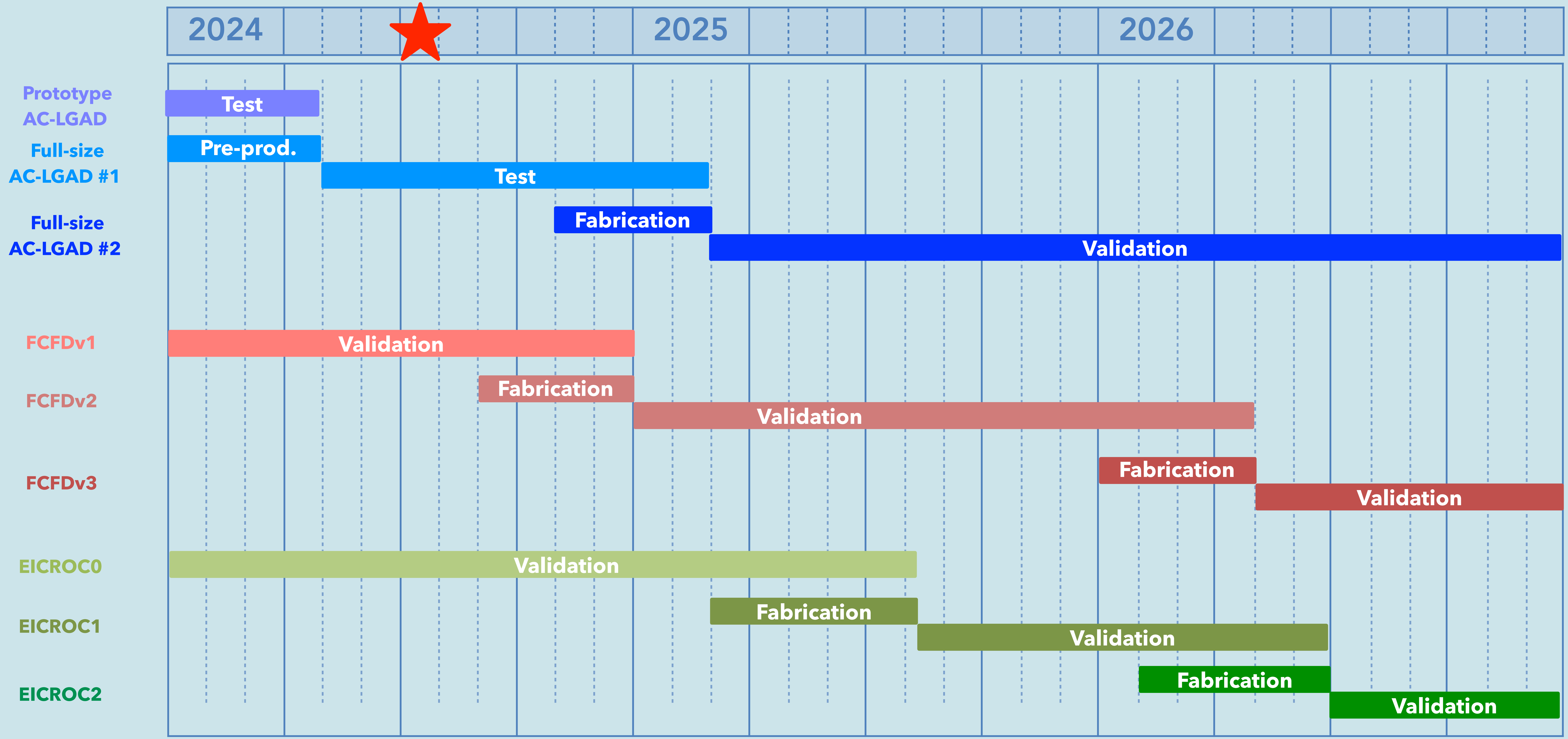
Module top view



Module cross section



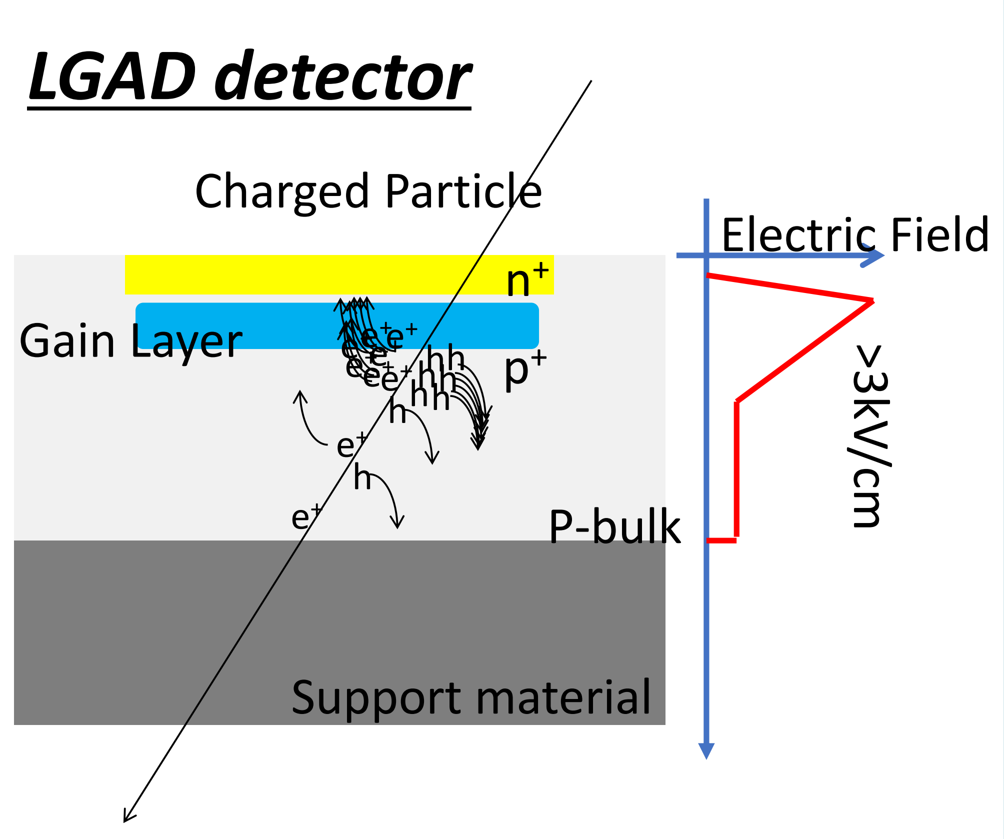
Original schedule of sensor + ASIC (Jan. 2024)

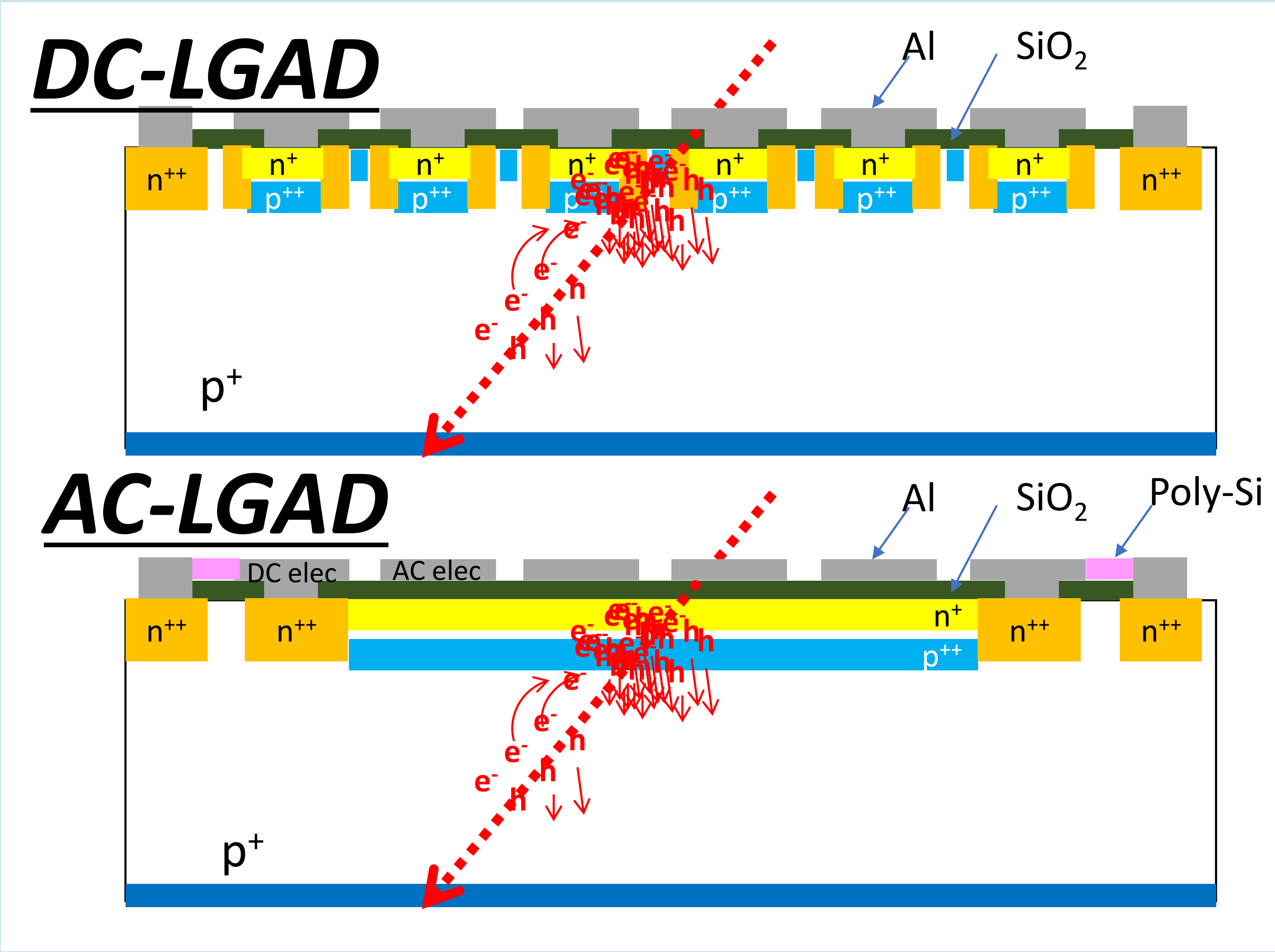


AC-LGAD technology

- Low Gain Avalanche Diode (LGAD)
  - The gain layer (p+ under n+ layer) makes a high electric field inducing electron avalanche → rapid signal raising
  - Standard LGAD (DC-LGAD) has much nonnegligible inactive area in fine segment case
  - CMS and ATLAS adopt DC-LGAD technology at HL-LHC

- AC-coupled LGAD (AC-LGAD)
  - One large gain layer with multiple AC-coupled readout metals on an oxide layer makes possible fine-segment readout keeping high timing resolution
  - High spatial resolution can be achieved with charge sharing even with relatively large pitches
  - EIC can adopt AC-LGAD technology thanks to the low multiplicity environment





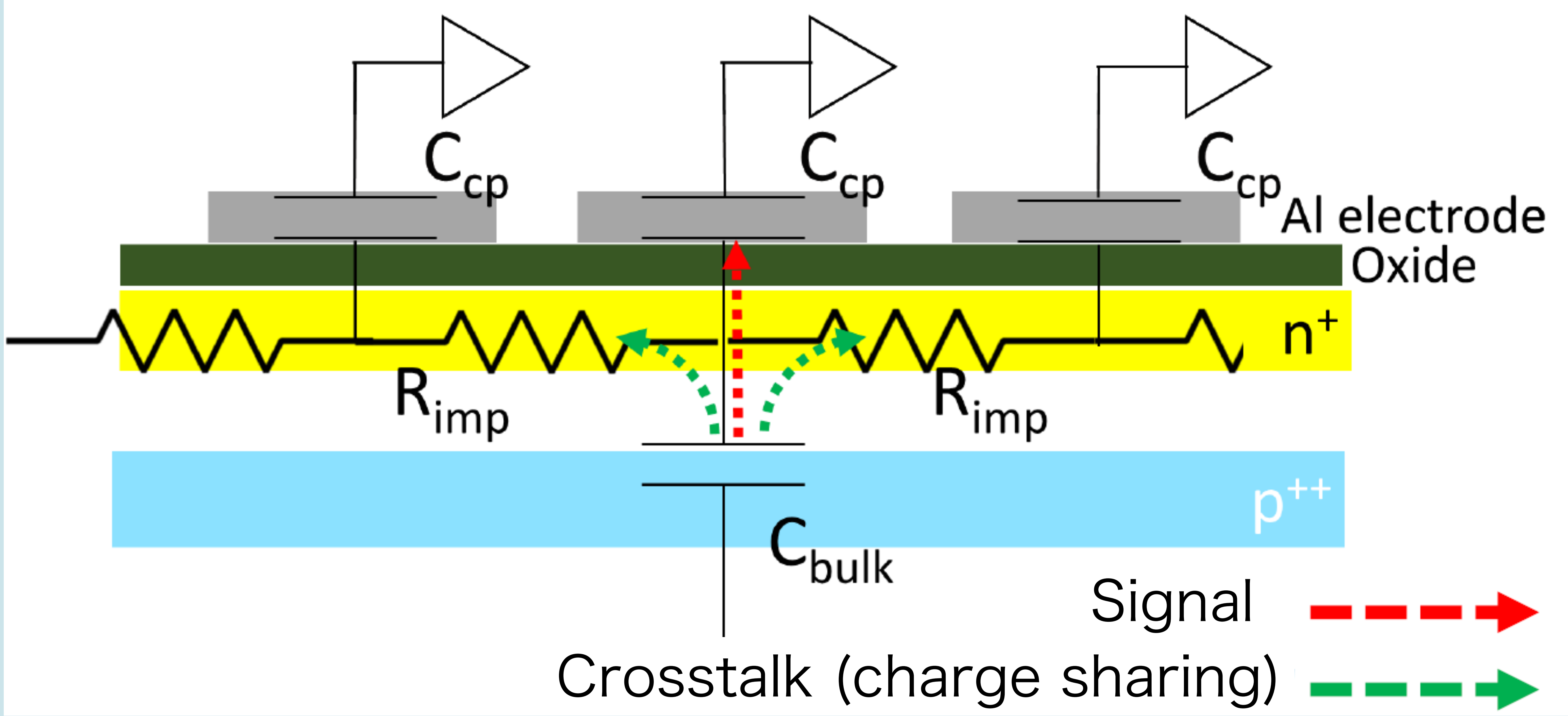
K. Nakamura et al.,
JPS Conf. Proc. 34, 010016 (2021)

R&D elements for AC-LGAD

- Issues of AC-LGAD
  - Crosstalk in n^+ layer
  - Small signal due to AC-coupling
- Signal size Q

$$Q = \frac{Z_{R_{imp}}}{Z_{R_{imp}} + Z_{C_{CP}}} Q_0$$

- Two important parameters
  - R_{imp} → larger is better
    - n^+ doping concentration
  - C_{cp} → larger is better
    - Smaller electrode size → smaller C_{cp}
    - Thinner oxide → larger C_{cp}



K. Nakamura et al., JPS Conf. Proc. 34, 010016 (2021)

Development goal

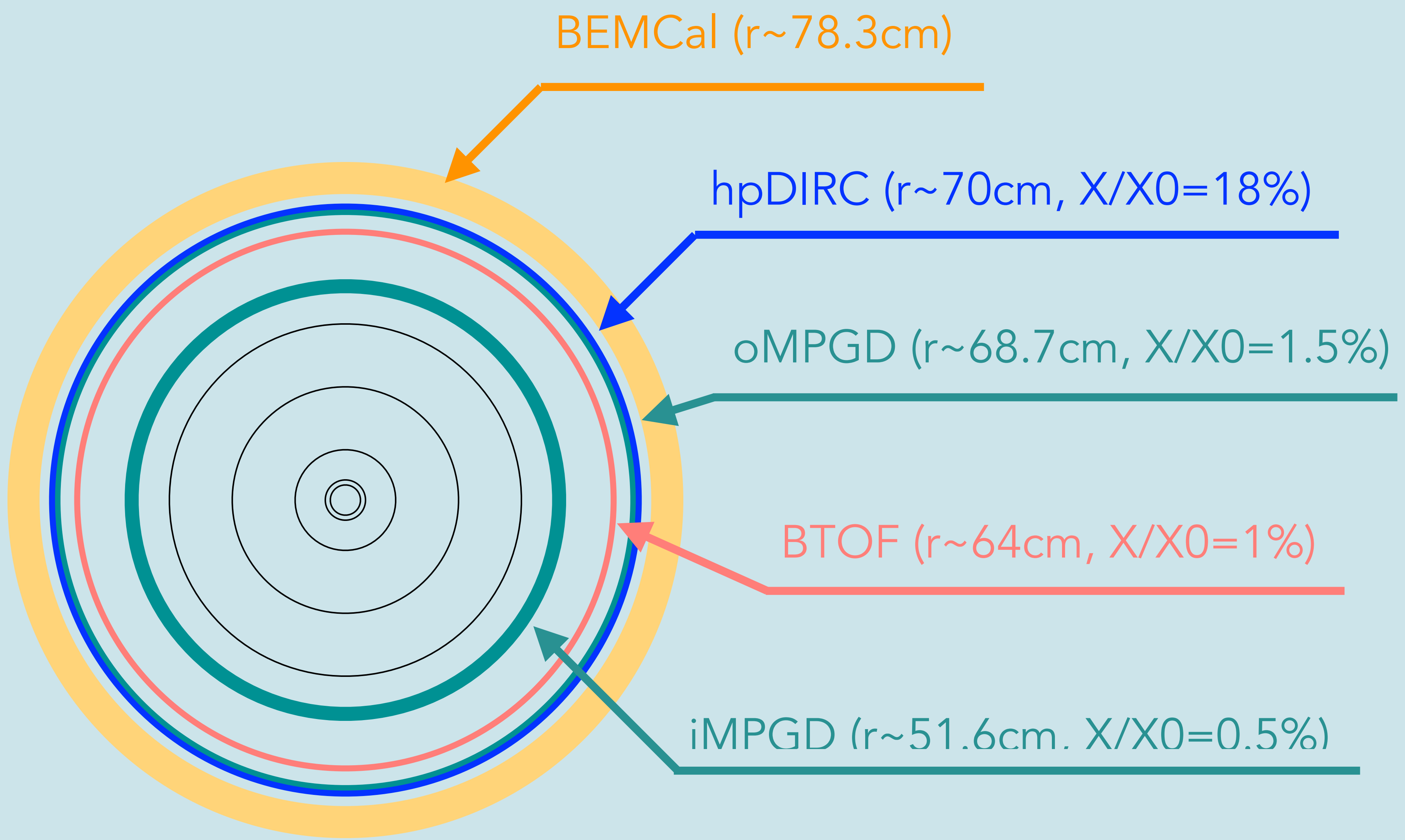
Keep a larger signal and smaller crosstalk with a good time and spatial resolution

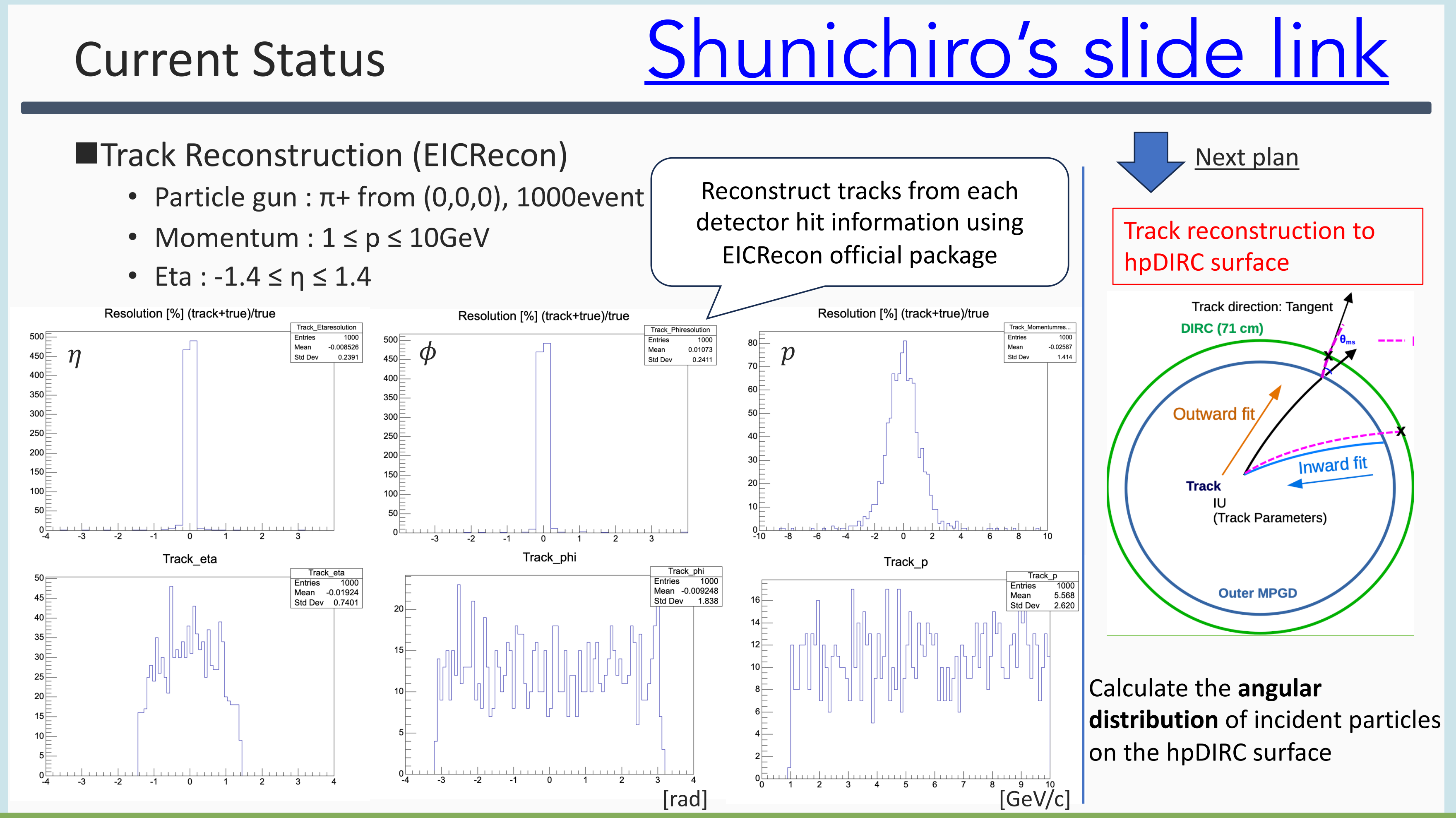
Material budget study (Hiroshima)

- **Shunichiro Muraoka** (M2 student) is working on the BTOF material effects on hpDIRC and BEMCal performance

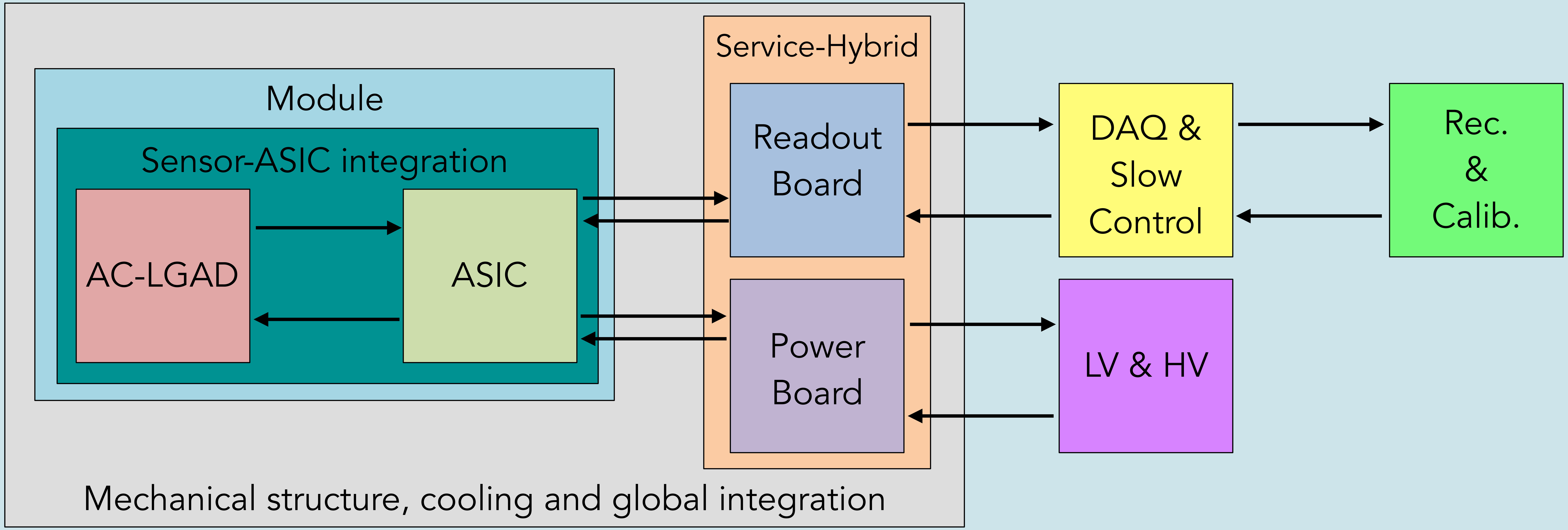
- This study is significant for the stave structure design
  - oMPGD is placed just in front of hpDIRC in the latest design →Not big effects on angular determination resolution by the BTOF material
  - The material budget of hpDIRC in the active area is approximately 18% → Not big effects on the EMCal performance by the BTOF material

- The study will reveal if the very strict limit of 1% material budget imposed on BTOF is really necessary
  - This will open new options for the stave material selection and 1.3 m FPC design





TOF structure



- **Barrel-TOF (BTOF)**
  - Strip-type AC-LGAD
  - ASIC (FCFD)
  - Sensor-ASIC integration
  - Module
  - Service-Hybrid
  - Mechanical structure
  - Global integration
- **Forward-TOF (FTOF)**
  - Pixel-type AC-LGAD
  - ASIC (EICROC)
  - Sensor-ASIC integration
  - Module
  - Service-Hybrid
  - Mechanical structure
  - Global integration
- **Common system**
  - DAQ
  - Cooling
  - Software (Rec. & Calib.)
  - HV & LV
  - Slow control

New clean room (100m²) @ HU
2024
2025
2026
2027
2028
2029
2030
Sensor
ASIC
Flex module PCB
Sensor-ASIC integration
Module Structure
Service Hybrid
Module Assembly
Support structure & cooling
Backend electronics
Alignment & Database
Assembly
Install into ePIC