Update on sketching readout for the Insert

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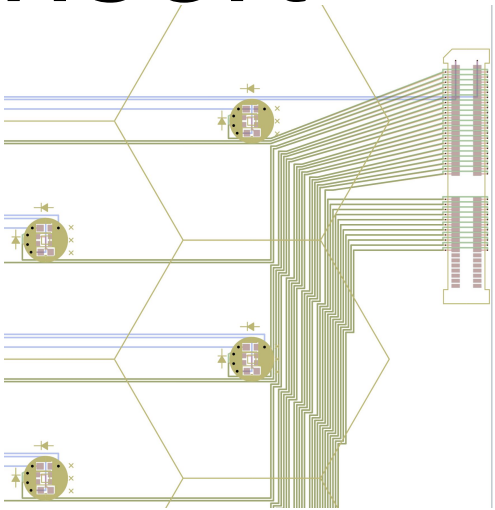
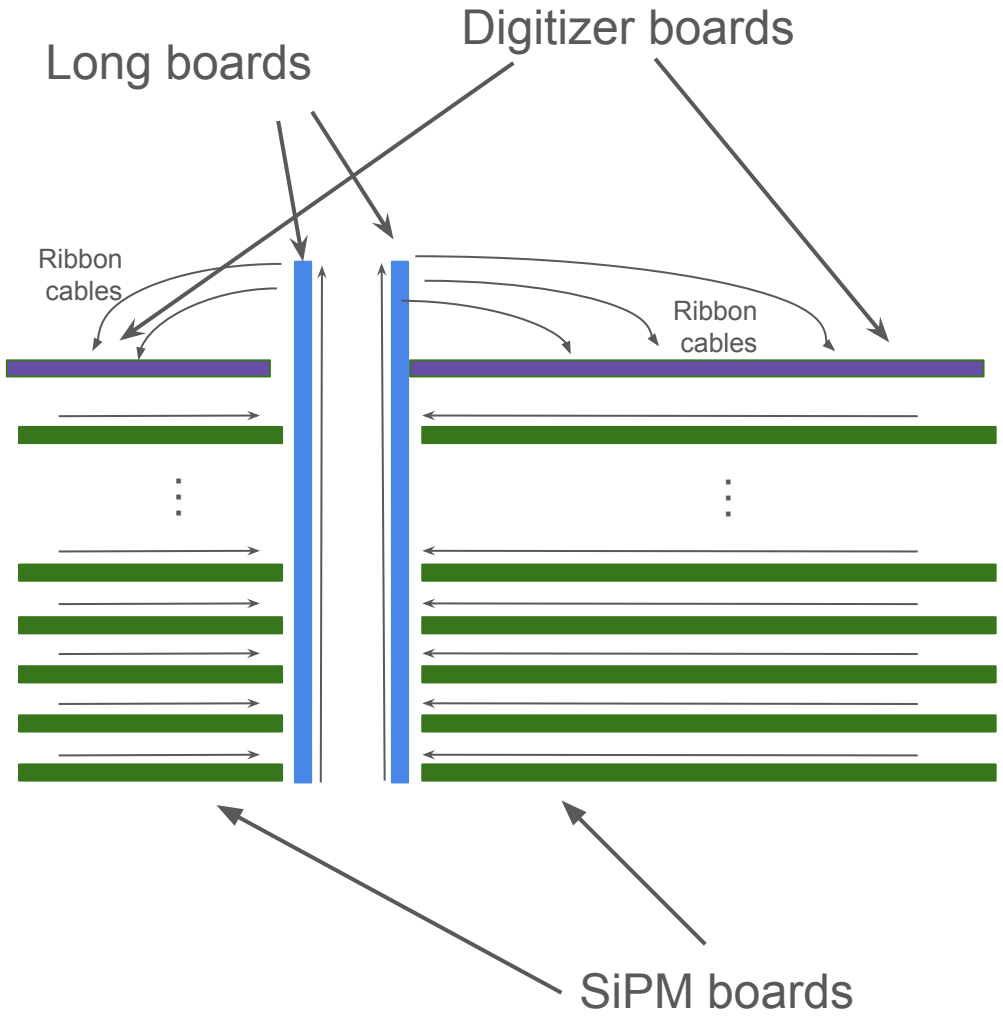


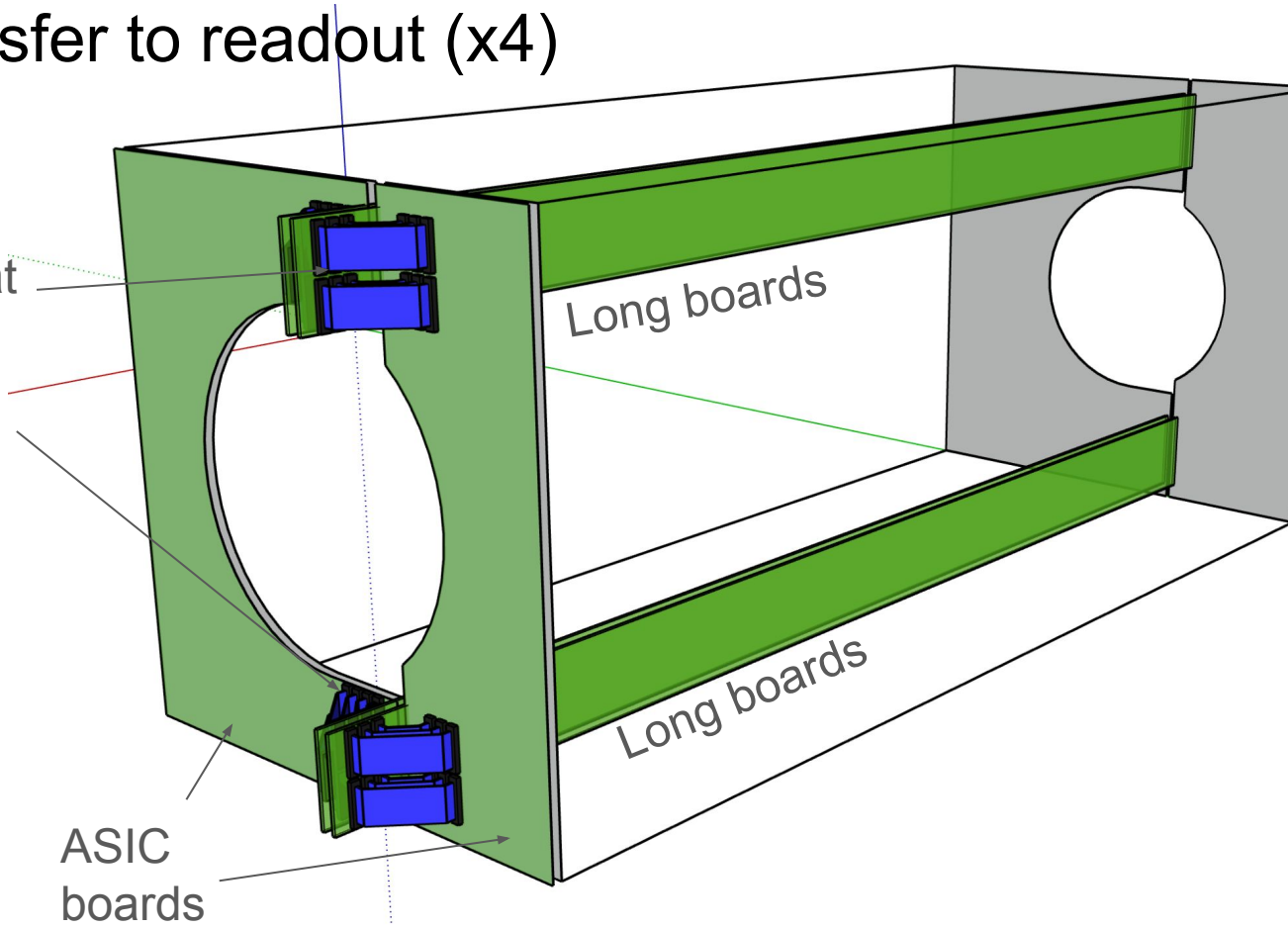
General schematics

- PCB boards with PCBs connect to the 4 long boards (2 on right, 2 on left)
- Long boards transfer signals to the ASIC digitizer boards at the back with ~100 CALOROC chips via ribbon cables

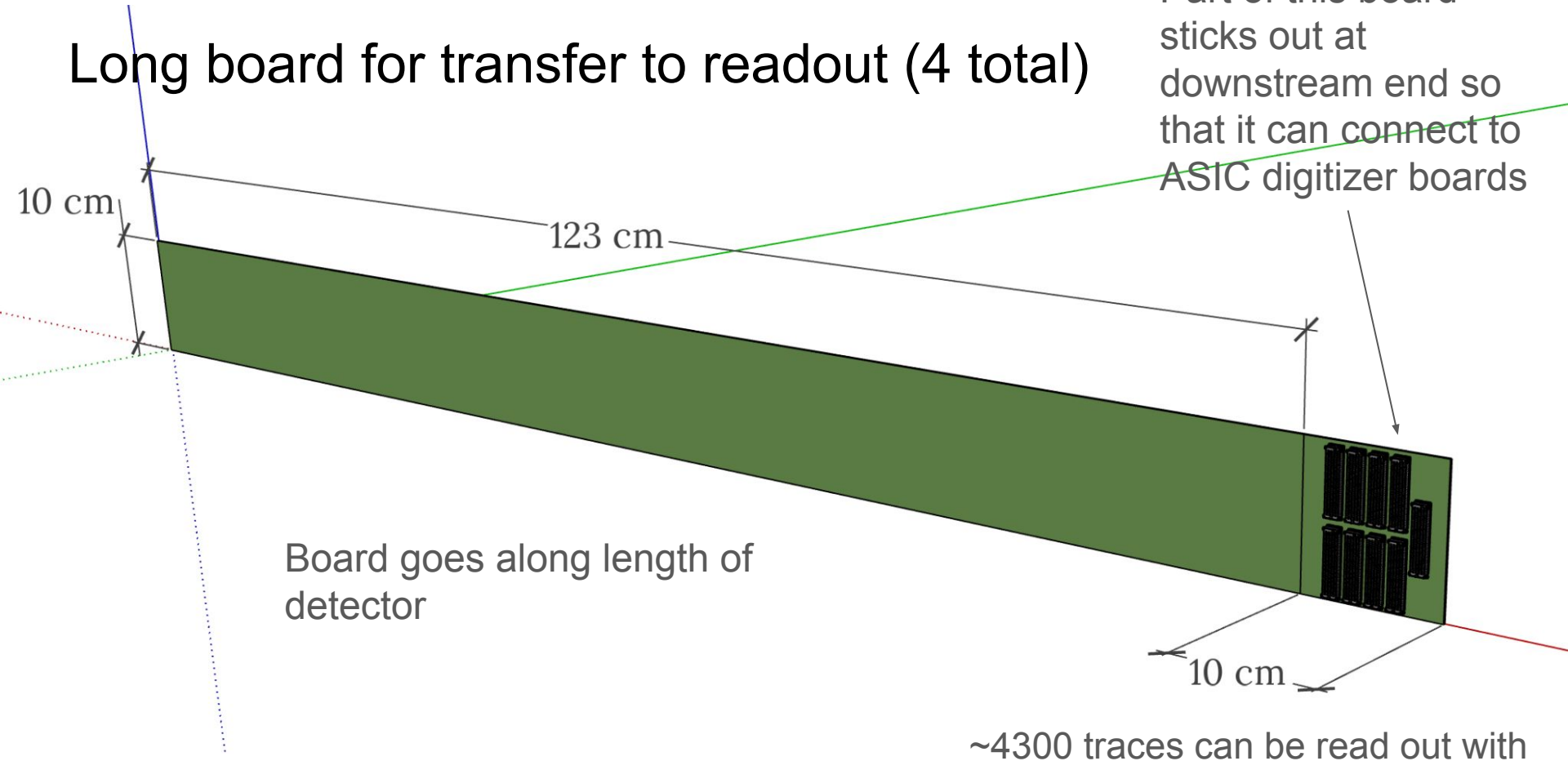


Long board for transfer to readout (x4)

Connects to ASIC boards at the downstream end of the detector via ribbon cables



Long board for transfer to readout (4 total)



Part of this board sticks out at downstream end so that it can connect to ASIC digitizer boards

Board goes along length of detector

*connectors shown are one possible implementation

~4300 traces can be read out with nine 500-pin ribbon connectors*

Possible connector for the long boards

500 pins per connector

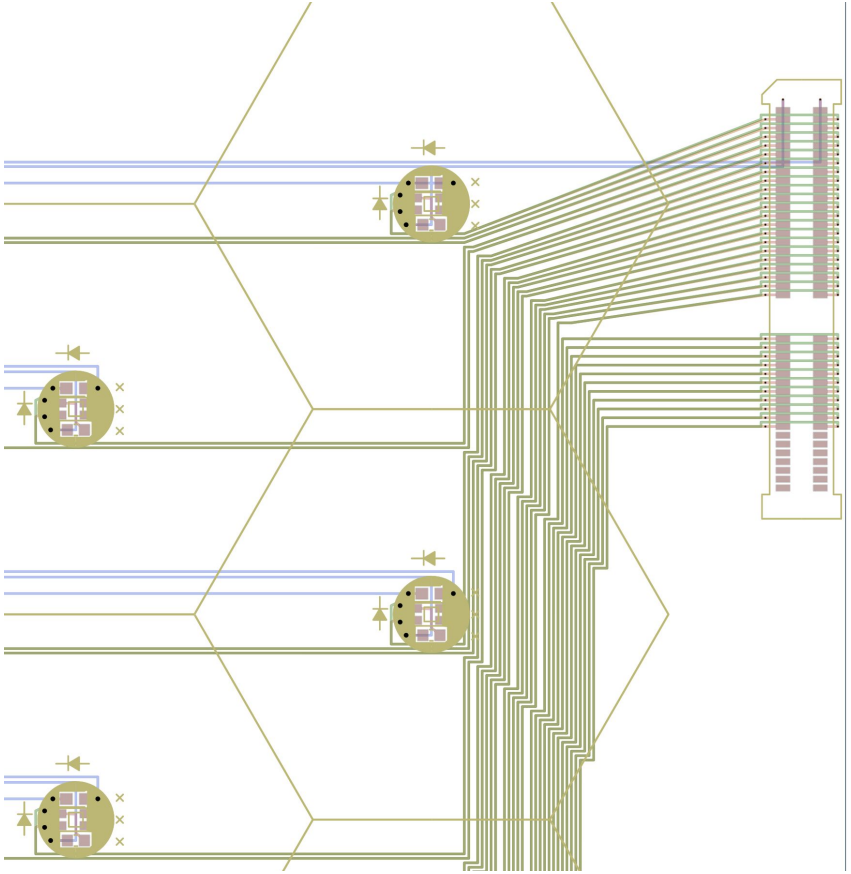
Images are for reference only
See Product Specifications

https://www.mouser.com/ProductDetail/Samtec/SEAM8-50-S05.0-S-10-3?qs=A6eO%252BMLsxmSKSxSzAdCA4g%3D%3D

Sketch of PCB board with SiPMs and traces to connectors

Multi-layer PCBs:

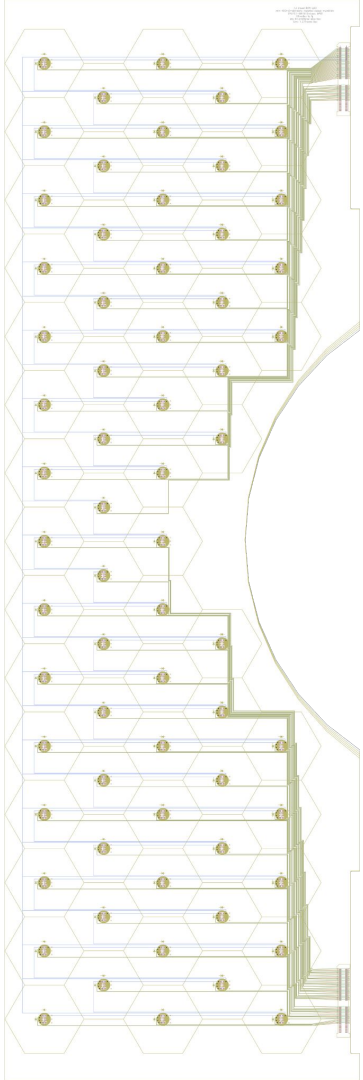
- Cathodes and anodes overlap one another in transverse position (makes it easier to program)
- Also connect LEDs in series, and capacitors to ground



*connectors shown are one possible implementation

Left side boards:

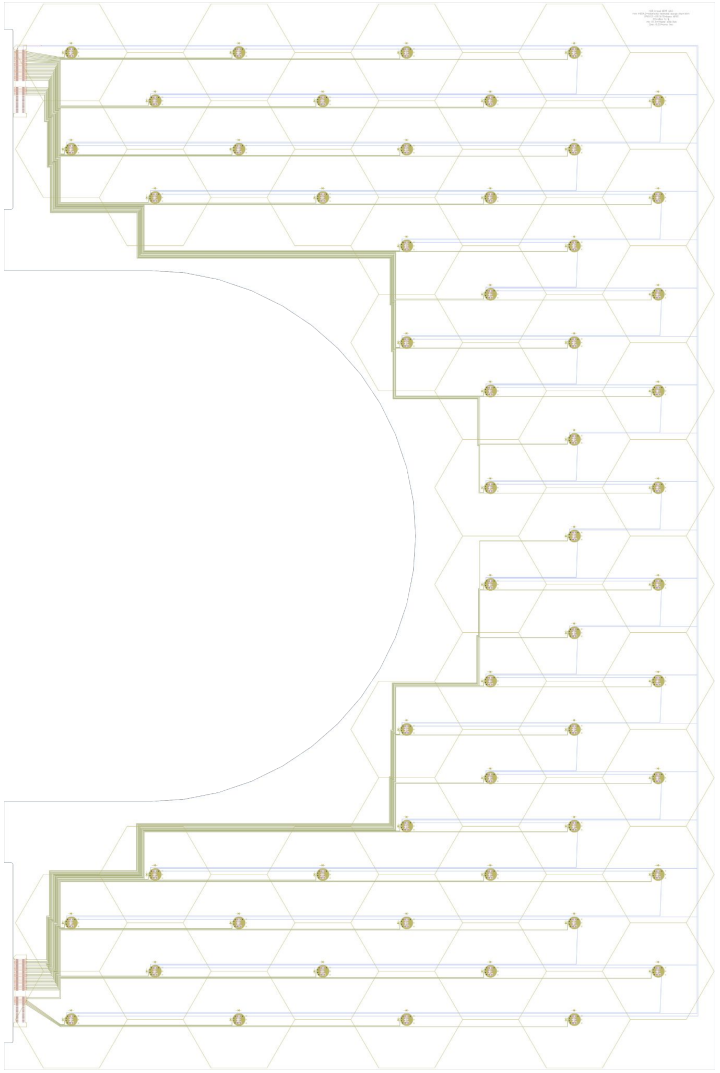
- Only two internal copper layers needed
- 5 total layouts:
  - Layers 1-20: 4 designs due to staggering
  - Layers 21-60: 1 non-staggered design
- Because the hole center moves to the right at about the same rate that the hole radius increases… the left edge of the hole stays in about the same location
  - We can just use the largest size hole for a given layout and reuse the board design without milling the holes to the right size



Right side boards

More complicated than left-side boards:

- Hole size and position changes:
  - May require a larger number of board variants
- Layers 21-60 (low granularity) can be done with 2 internal copper layers
- Layers 1-20 (high granularity) cannot be done with 2 internal copper layers; will require 4 or more internal layers



Summary

- Progress is being made towards algorithmically traced SiPM-carrying boards
  - SiPMs, LEDs, and capacitors to ground in each dimple, with their respective connections
  - Left-side boards are nearly completed
  - Right-side boards will require a little more work
  - Estimated number of total board layouts: between 10 and 25
  - Connectors not finalized yet, but the algorithm to connect them to the SiPMs can be adapted
- Long boards will transfer signals from SiPM boards to the digitizer boards
  - There is sufficient space at the downstream end of the board for connectors to ribbon cables