Streaming Readout Workshop SRO-XII
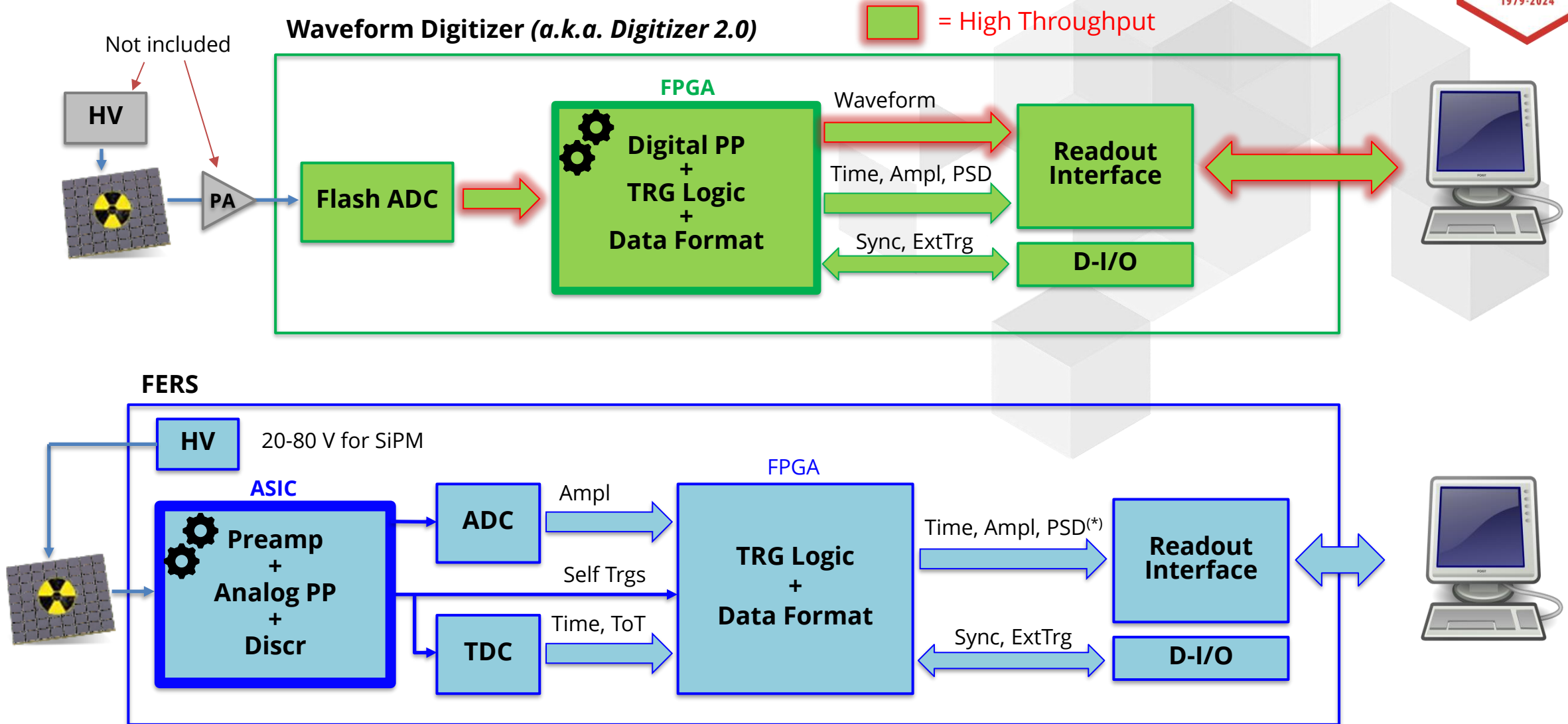
CAEN solutions for SRO

Giovanni Cerretani

Introduction
Two different approaches to the detector readout chain

- New physics experiments and medical imaging applications are using detectors with **higher density, lower cost per channel** and **faster signal outputs**. The most representative example is the transition from PMT to SiPM.

- Readout electronics must follow this transformation: CAEN has developed two complementary product lines to meet the increasing demands for channel count, scalability, and data throughput.

1. **Waveform Digitizer**: full digital readout chain (Flash ADC + FPGA) with the possibility to develop and upload **user-defined algorithms** for the digital pulse processing. Maximum flexibility in customizing the hardware for a wide range of detectors and applications.

2. **FERS**: all-in-one readout chain based of dedicated ASIC chips directly connected to the detectors. The system is composed of multiple distributed cards, all controlled and synchronized by a single data concentrator via an optical link, ensuring maximum scalability starting from low-cost single units.

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Waveform Digitizer vs FERS (ASIC readout)

Digitizer 2.0 – Flavors

|	2740/2745	2730	2751
Channels	64	32	16
Sampling	125 MS/s @ 16 bit	500 MS/s @ 14 bit	1 GS/s @ 14 bit
Variable Gain Amplifier	x100 *(2745 only)*	x20	x10
Max record length	84 ms per channel *(extendable by disabling channels, WIP)*		
Applications	• PMT with slow scintillators (e.g. NaI) • Spectroscopy with segmented Si and HPGe • Dark Matter and Neutrino experiments	• High Resolution Timing • Fast detector readout (PMT, SiPM, etc…) • Pulse Shape Discrimination with liquid and plastic scintillators (n/γ discrimination) • Multi parametric acquisition (Energy + Time + PSD)	

New families coming soon! Stay tuned!

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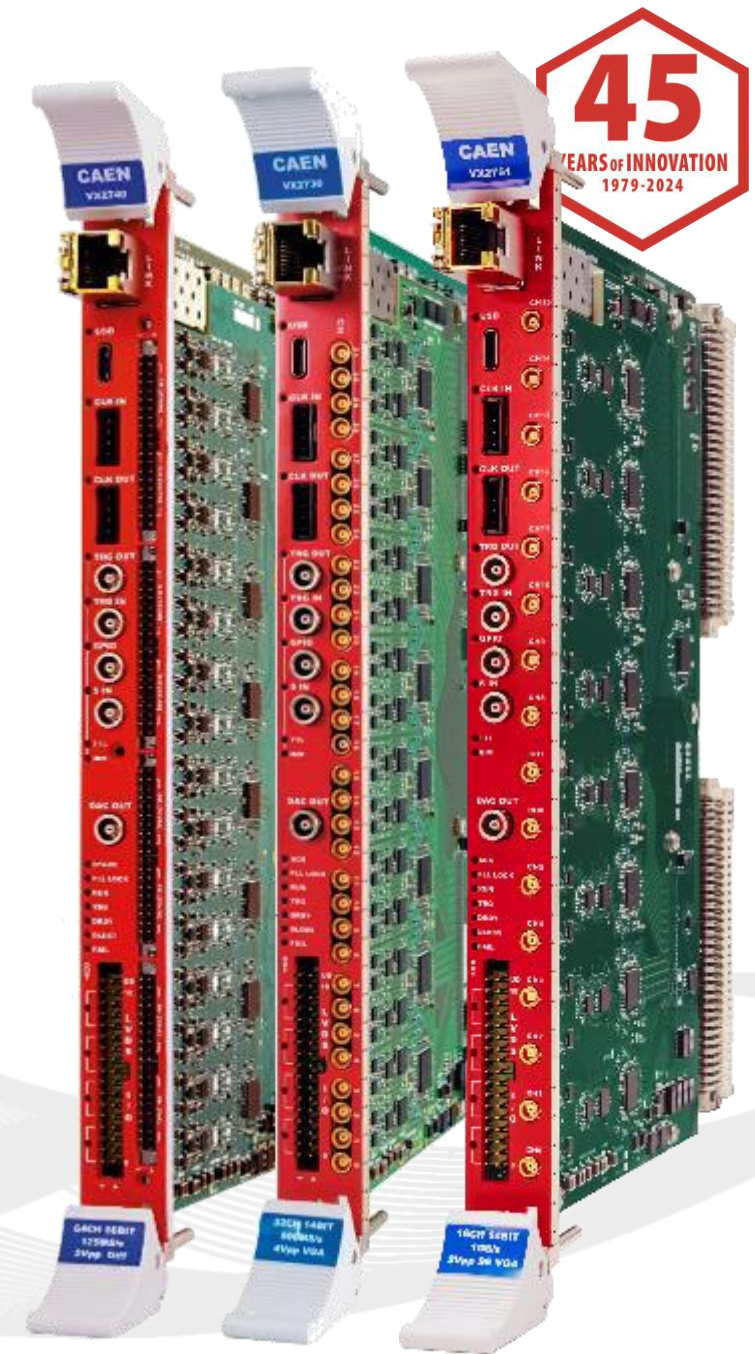
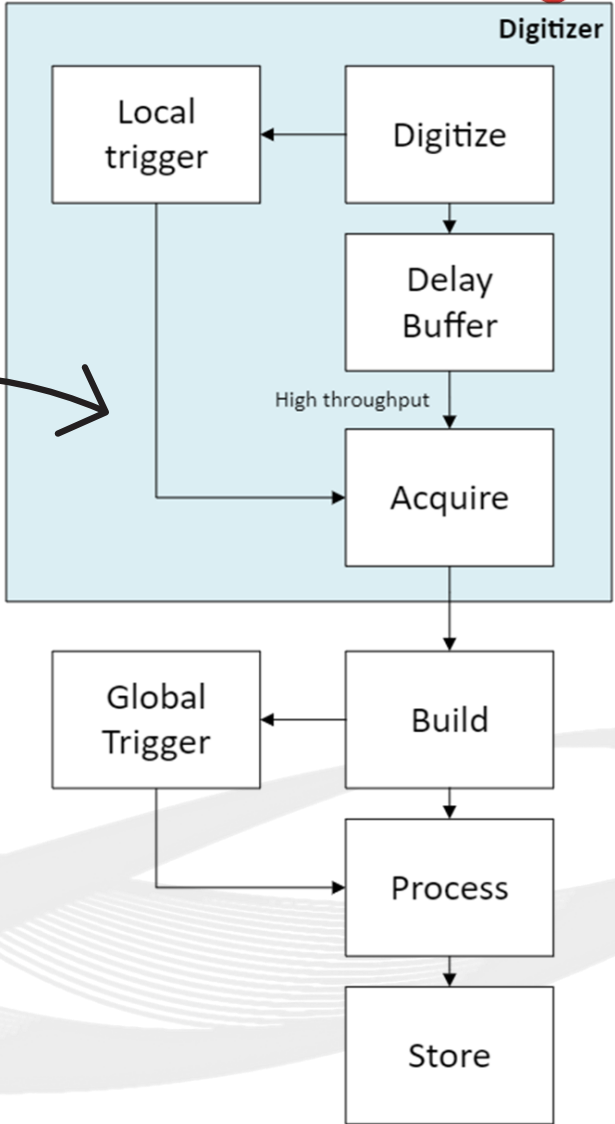# Digitizer 2.0 – Triggered and Streaming Readout

Triggered Readout
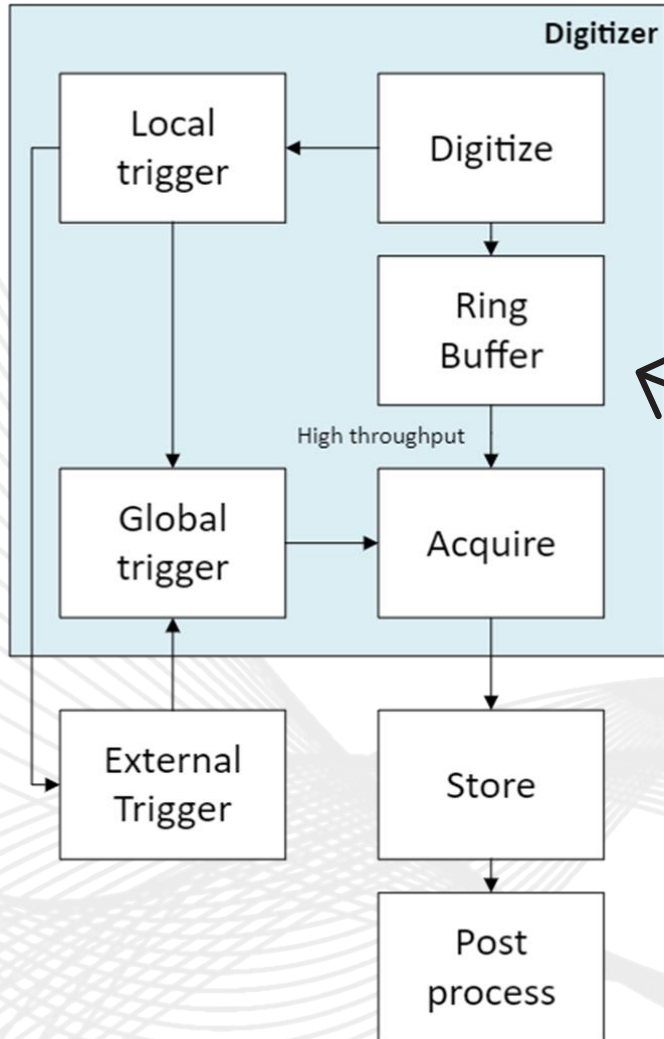
Two firmware families:

Waveform recording (a.k.a. Scope)
- Common trigger (an event contains the waveforms of all channels)
- Big events (24 + 2 bytes per sample):
  - Timestamp
  - Waveforms

Digital Pulse Processing (DPP)
- Individual trigger (an event contains only one channel)
- Many flavors (PHA, QDC, PSD, CFD, ZLE, DAW, Open DPP)
- Small events (16 or 8 bytes):
  - Channel
  - Timestamp
  - Energy and PSD
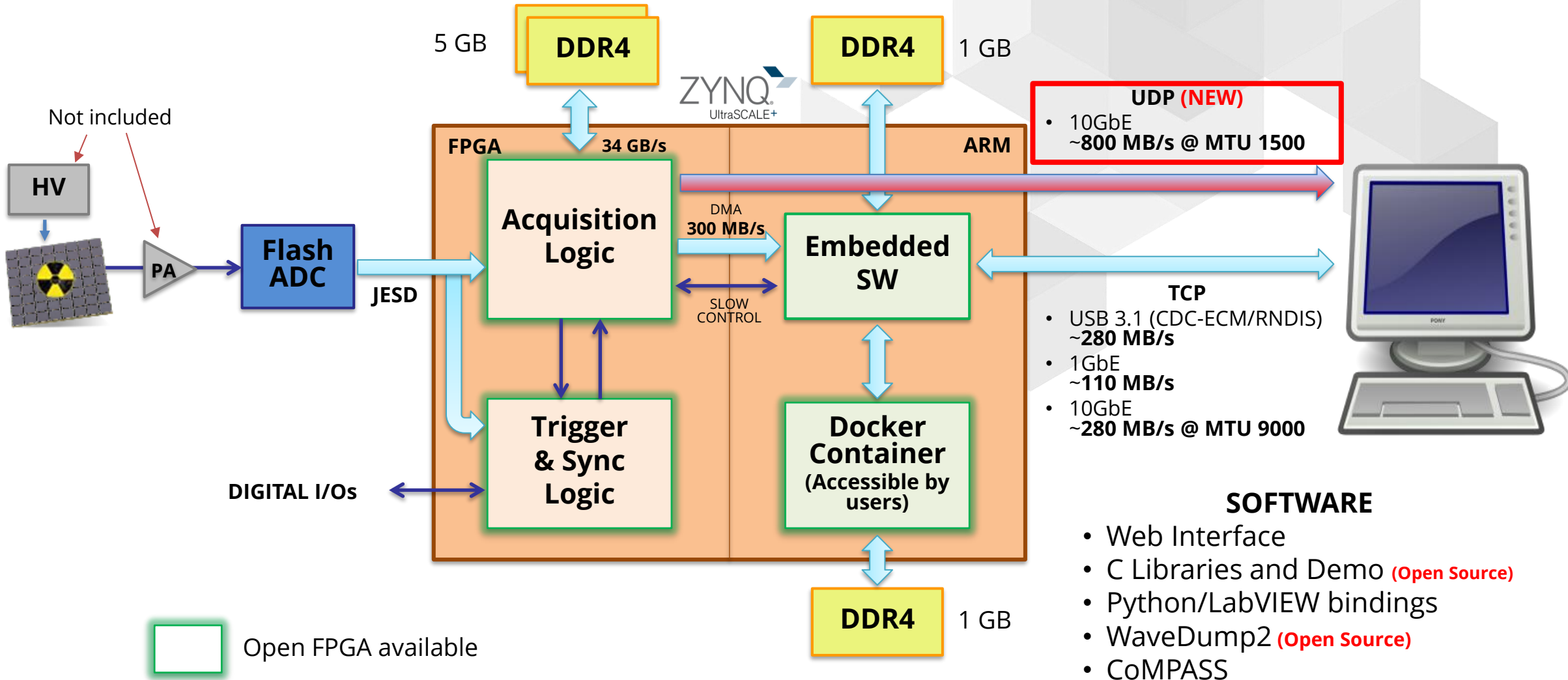 - Flags
  - *Waveforms (optional)*

Streaming Readout

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Digitizer 2.0 - architecture

SOFTWARE
- Web Interface
- C Libraries and Demo (Open Source)
- Python/LabVIEW bindings
- WaveDump2 (Open Source)
- CoMPASS

Digitizer 2.0 – Why do we need UDP?

TCP bottleneck	Mitigation
Computationally expensive on ARM	Increasing MTU from 1500 to 9000, but not standard and eventually limited to 280 MB/s
DMA readout rate	Currently hard to go faster than 300 MB/s

	Connection	MTU	Max. readout rate	Max. trigger rate	
				Scope (2)	DPP (3)
TCP	USB 3.1	15000	~280 MB/s (1)	~140 kcps	~18 Mcps
	1GbE	1500	~110 MB/s	~56 kcps	~7 Mcps
	10GbE	1500	~200 MB/s	~100 kcps	~13 Mcps
		9000	~280 MB/s	~140 kcps	~18 Mcps
UDP	10GbE	1500	**~800 MB/s**	**~410 kcps**	**~52 Mcps**

Notes:

(1) Drops to 250 MB/s with 3 boards and to 185 MB/s with 4 boards due to client CPU overload

(2) Scope firmware, record length of 1024 samples per channel (8192 ns on a VX2740)

(3) DPP firmware, reduced event format disabled (16 bytes per event)

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Digitizer 2.0 - UDP readout implementation

Relatively easy to implement UDP in VHDL. Two main issues:

1. Data losses

   - Can be estimated by tagging each datagram with an incremental ID

2. Reassembly errors at high data rates

   1. UDP datagrams (size ≤ 65507) are fragmented in IPv4 packets (size ≤ MTU) that share the Identification field.

   2. Identification field rolls over in few seconds on 10 GbE maximum rate and 1500 MTU (see RFC 4963)

   3. In case of data losses, OS can reassemble a datagram using old fragments (reassembly timeout ~15 seconds)

Resolved by adding a 32-bit DJB2a checksum in the application layer on each datagram: reassembly error is detected as data loss.

IPv4 header
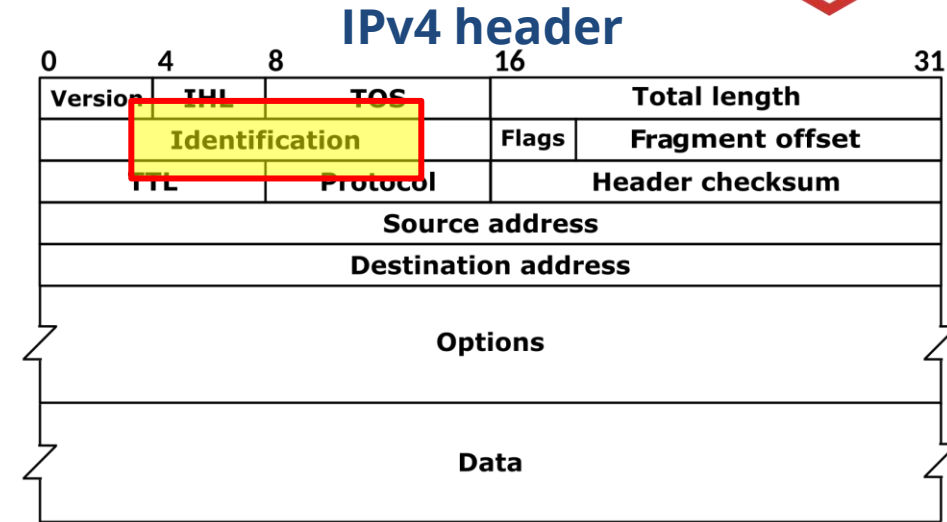
No data loss imply no reassembly error: no risks if the DAQ is properly configured and tuned.

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Digitizer 2.0 - UDP readout performance

CAEN hardware:
• VX2730
• Scope firmware

User hardware used for test:
• Intel® Ethernet Network Adapter X710
• Intel® Core i7 10700K
• Ubuntu 22.04 *(Windows 11 also supported)*

Using CAEN FELib, the transport layer is transparent to the user. **It is possible to estimate the amount of data losses.**

```
###########################################
          CAEN firmware Scope demo
###########################################
device path: dig2://10.0.0.254
Model name:      VX2730
Serial number:   30009
ADC bits:        14
Channels:        32
ADC rate:        500.000000 Msps
CUP version:     2024111900
Resetting...     done.
Configuring...   done.
Starting...      done.
###########################################
Commands supported:
       [t]      send manual trigger
       [q]      stop acquisition
       [w]      plot next waveform
###########################################
Time (s): 11.0  Events: 10544   Events lost: 17 Readout rate (MB/s): 850.120544
```
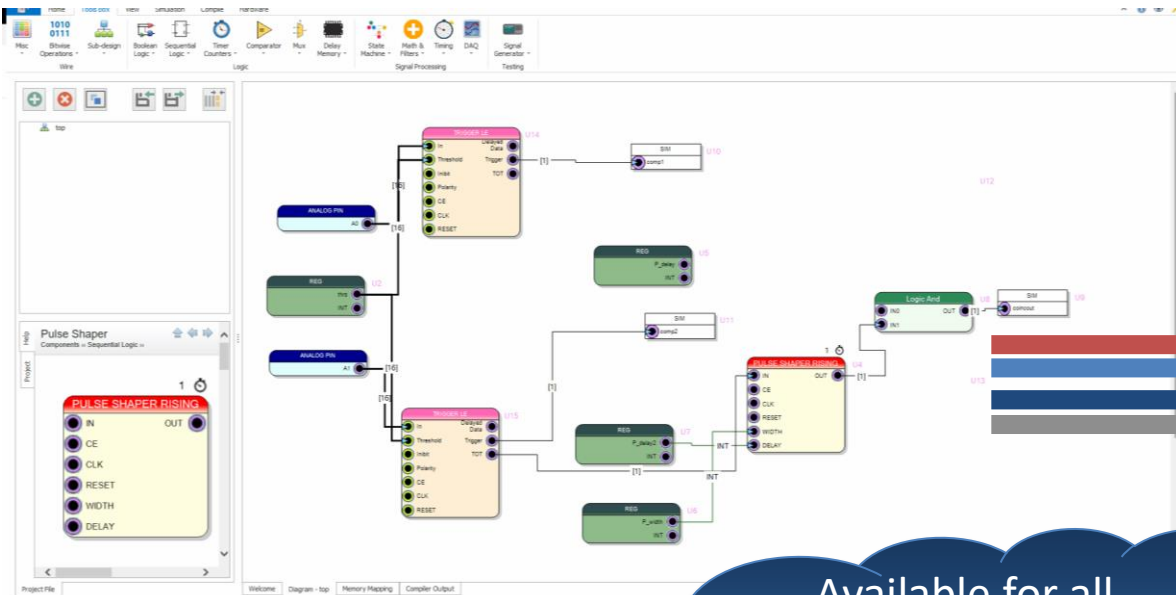
Since UDP sender has no feedback from the receiver, there are two parameters to control readout rate, inspired to iperf3 CLI:
• **UdpDatagramSize**, in range [0, 65504] bytes (cf. `iperf3 --length/-l`)
• **UdpBandwidth**, in range [50, 900] MB/s (cf. `iperf3 --bandwidth/-b`)

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Open FPGA - SciCompiler
A graphical tool for FPGA programming

- Easy and quick development of Data Processing algorithms and advanced Trigger Logic
- Remote Customization Service for compilation and simulation with minimal local setup
- Includes a library of precompiled IPs designed for physics applications
- No VHDL or Verilog coding expertise required

Block diagram — Define the functionalities of the firmware

Function blocks — Build the diagram relying on a wide library of blocks for physics and nuclear engineering

Firmware — Automatic generation of VHDL and bitstream. No coding expertise required

Testing — Easy-to-use embedded tools for debugging

Available for all Digitizer 2.0, both Waveform Recording and DPP

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FERS: all-in-one readout system based on FE ASICs

- Many research groups and spin-off companies develop **ASICs** for the readout of multi-detector systems in NP and HEP applications. Sometimes, they also develop the electronic boards housing the ASICs.

- The same ASICs may become interesting for other applications, but the electronics and the relevant software must be redesigned and adapted.

- **FERS** (Front End Readout System) aims to implement versatile modules facilitating the integration of ASICs, ensuring their adaptability across diverse applications through comprehensive hardware and software provision. **FERS can be used as a stand-alone evaluation board as well as a highly scalable solution.**

Synergies

Off-the-shelf front-end ASIC for scientific instrumentation.

Design of Readout Electronics and Power Supply for NP and HEP

First born: A5202, 64 channel SiPM readout with Citiroc

HV Bias (on the bottom)

uC

+12V DC-IN

2 In + 2 Out

Eth/USB

TDlink
Data + Sync

Detector inputs
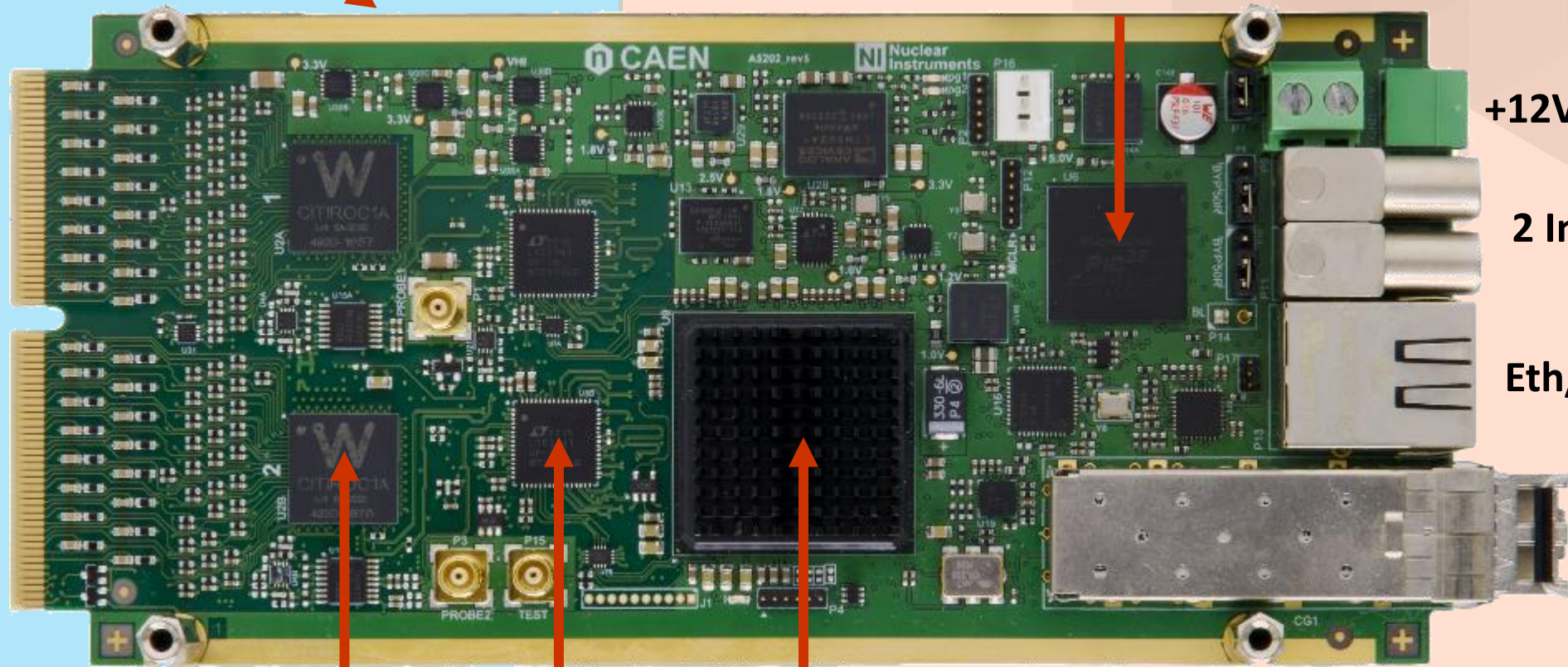
FE-ASIC

ADC

FPGA

DETECTOR SPECIFIC FRONT-END

COMMON INFRASTRUCTURE

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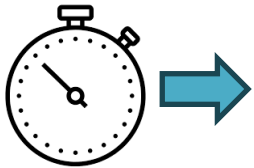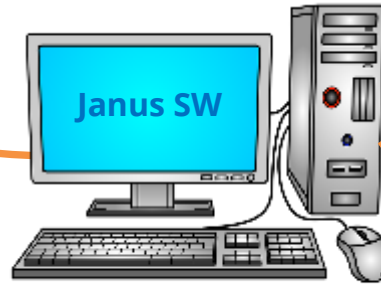
FERS scalable architecture

45 YEARS OF INNOVATION 1979-2024

DT5215 Data Concentrator:

- 1 TDlink => up to 16 FERS
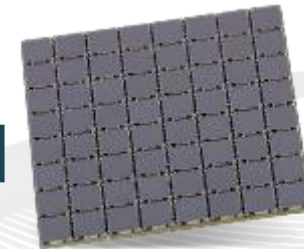- 1 DT5215 => 128 FERS = 8k/16k ch.

Global Time

1/10G Eth USB 3.0

Janus SW

10/100M Eth USB 2.0

Desktop Evaluation Setup: Low Cost, Plug & Play

3.125 Gb/s TDlink
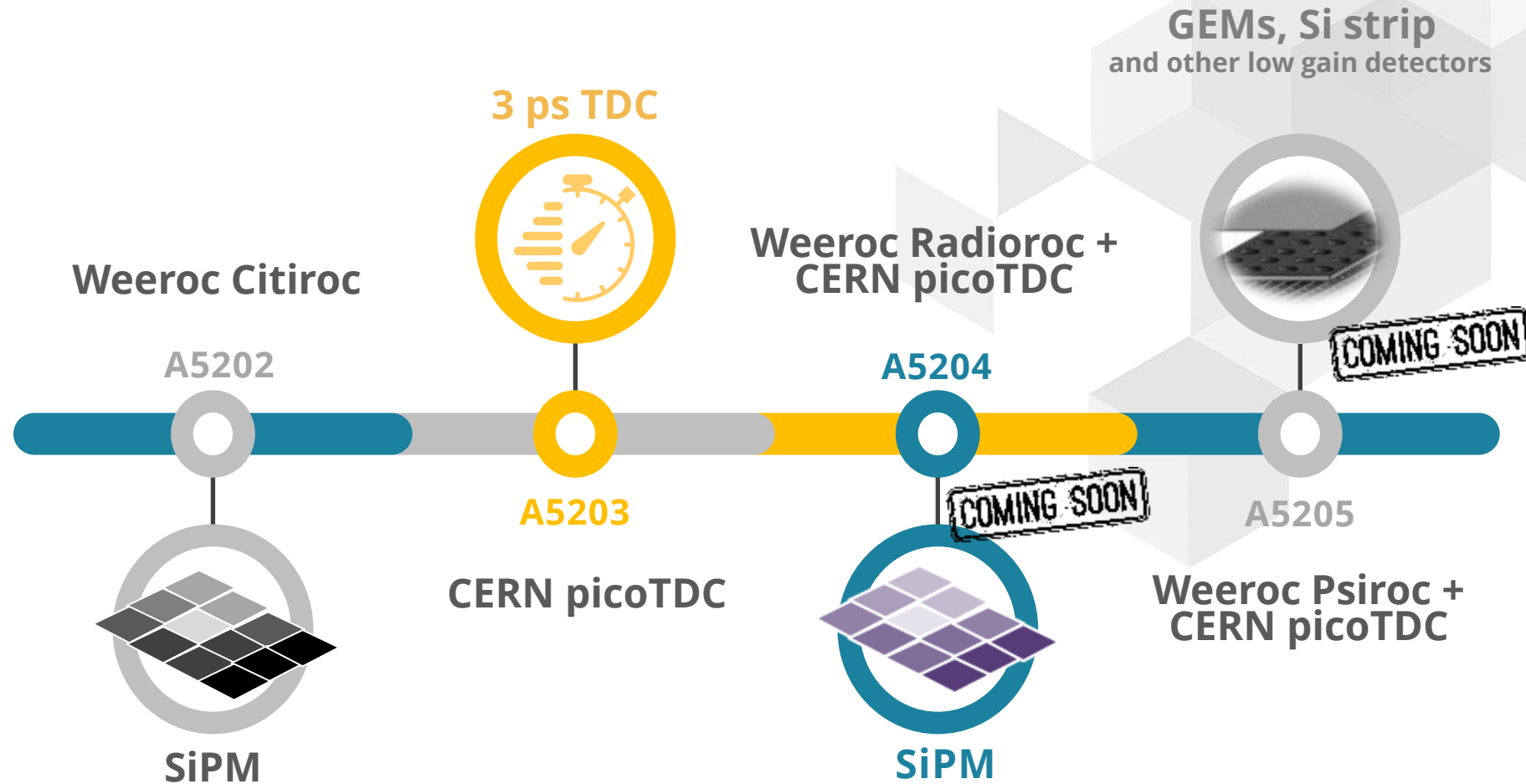
Readout + Slow Control + Synchronization

Custom Flange or Backplane

Easy ASIC integration on FERS

FERS – flavors and roadmap

**45 YEARS OF INNOVATION 1979-2024**

GEMs, Si strip
and other low gain detectors

3 ps TDC

Weeroc Citiroc

Weeroc Radioroc +
CERN picoTDC

A5202

A5204

COMING SOON

A5203

A5205

CERN picoTDC

SiPM

COMING SOON

Weeroc Psiroc +
CERN picoTDC

SiPM

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FERS – Readout modes

(*) PSD capabilities depends on ASIC type
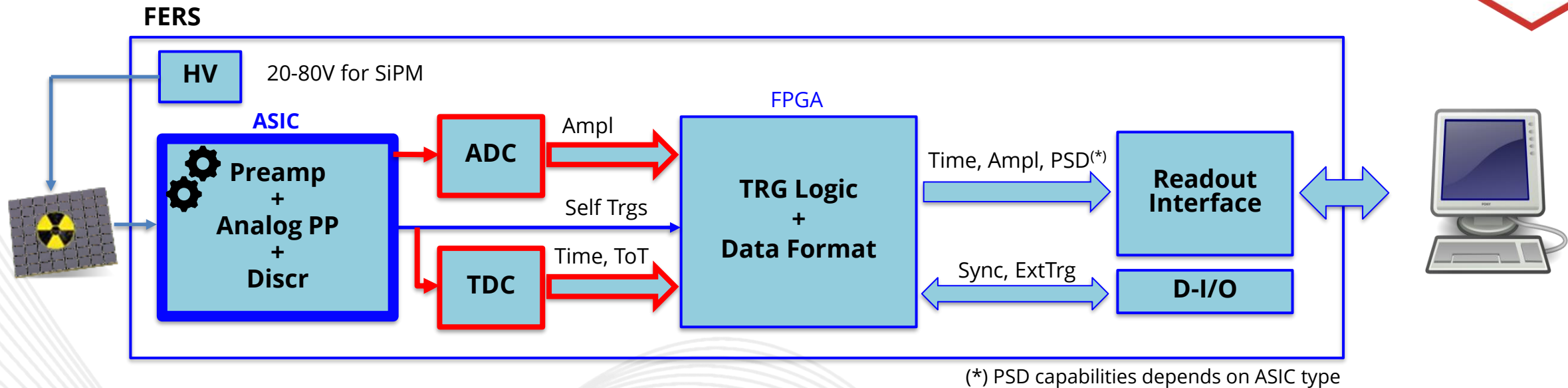
When a trigger occurs, we have a two parallel data flow:

- ASIC processes the analog input and generates a peak sensing value for each channel. Each value is converted sequentially (multiplexed output) by an ADC.

- The 64 channel self-triggers (discriminator outputs) are used to generate the board bunch trigger that starts the A/D conversion, but can be used also for counting, time stamping and to determine the Time over Threshold (ToT) information.

FERS – Converting ToT to amplitude using CERN picoTDC
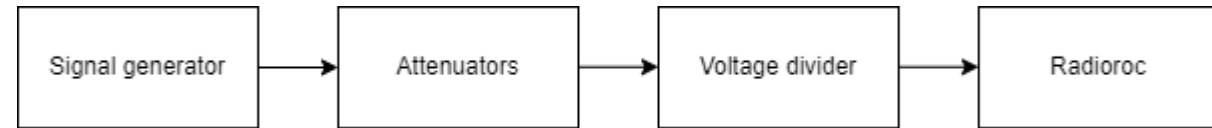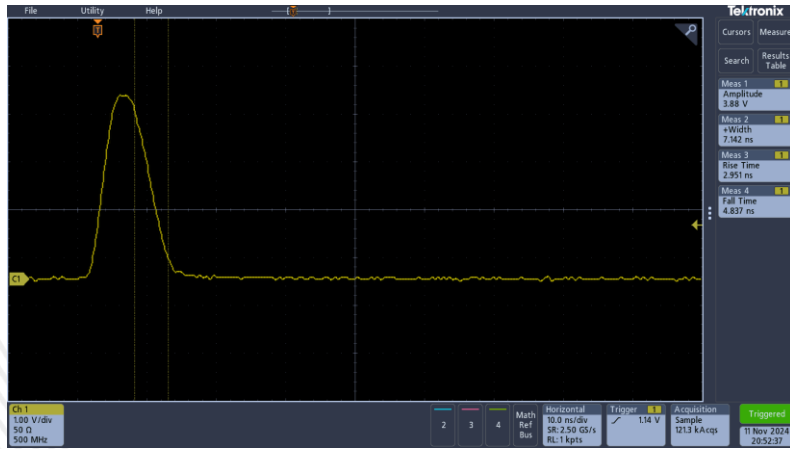
With a signal generator, we reproduce a real signal of a fast PMT with a current preamplifier.

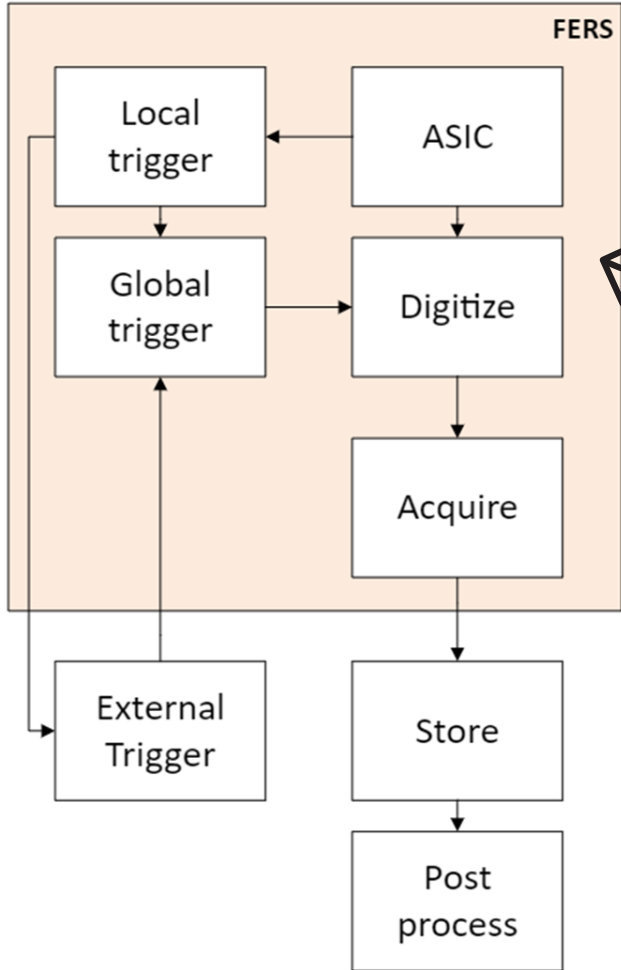The signal is then attenuated by a programmable attenuator to get the calibration curve.
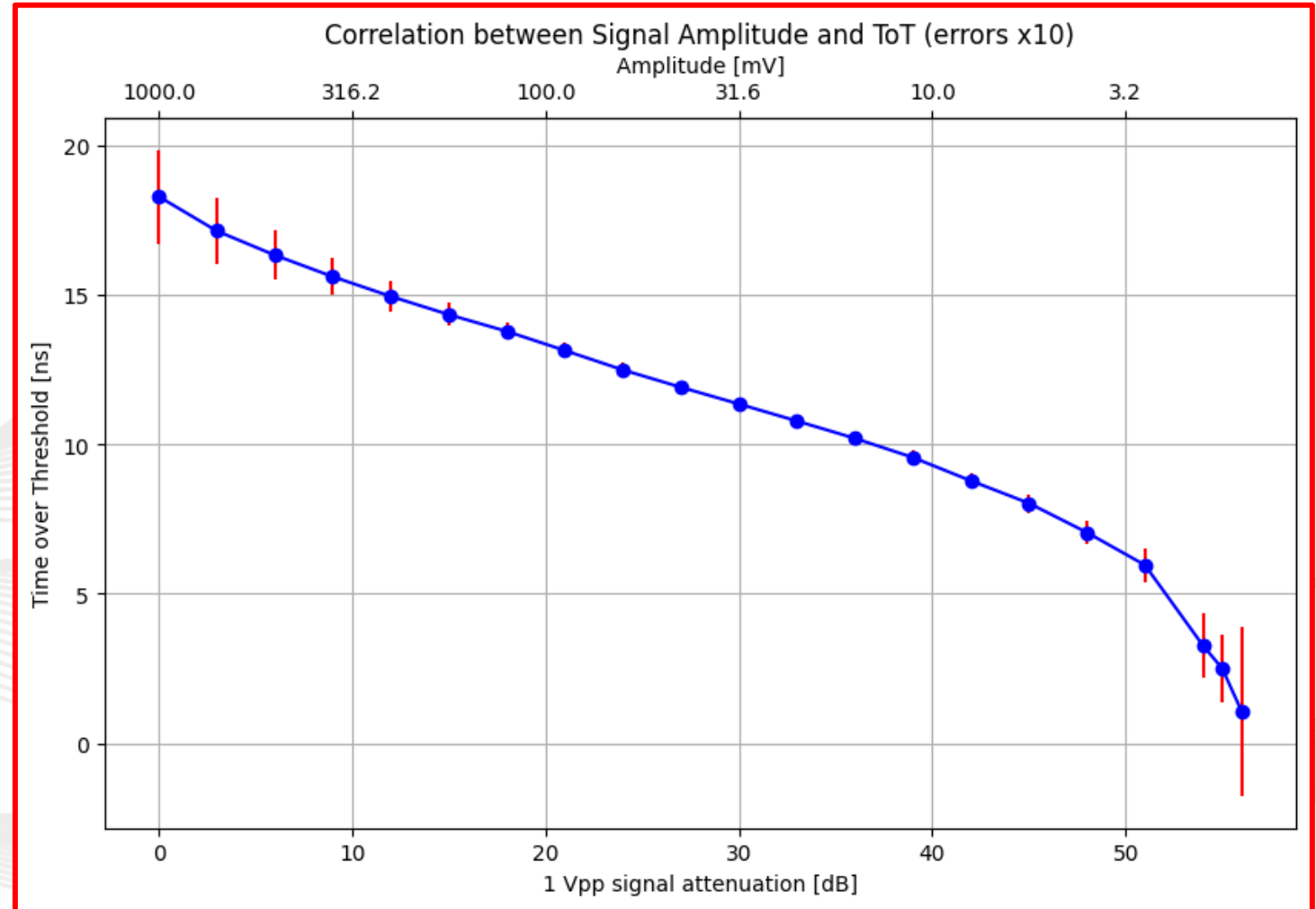
FERS – Triggered vs Streaming Readout

Triggered Readout

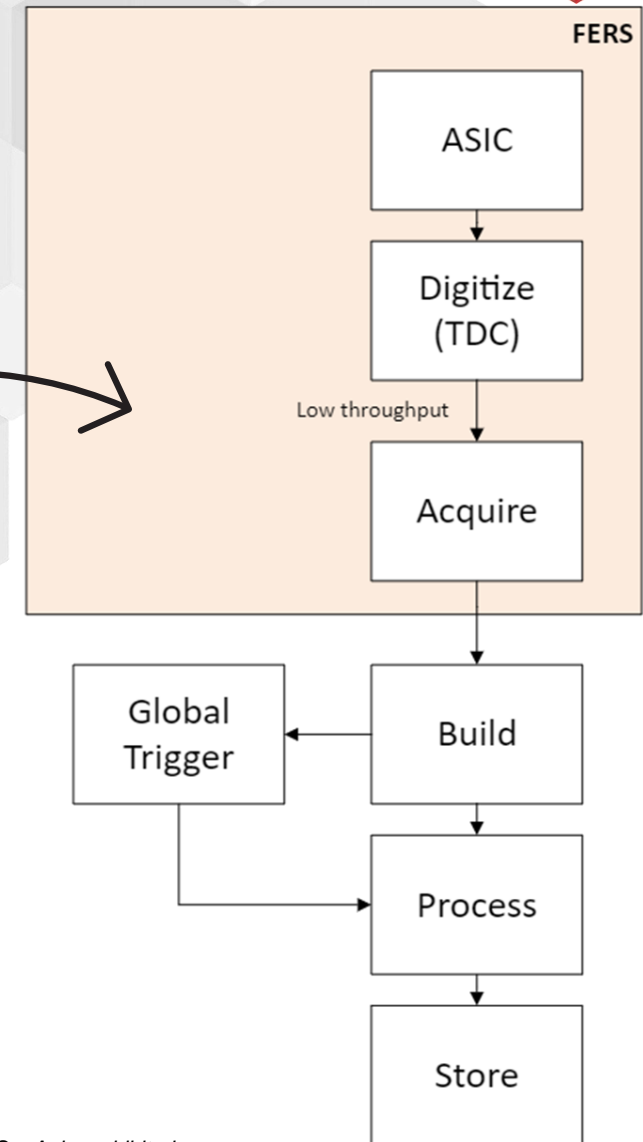**Streaming Readout**

ADC
Multiplexed A/D conversion:
- Common trigger
- High dead time

Amplitude from ToT
ToT can be converted to amplitude using a calibration, without the need of the multiplexed A/D conversion:
- Triggerless
- Individual trigger
- Very low dead time
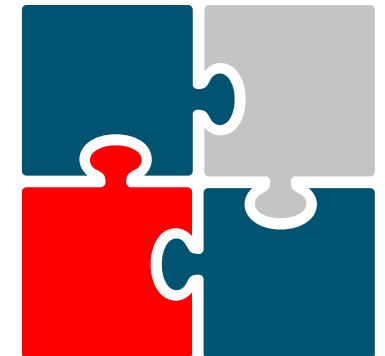- Extremely high rate

Conclusions
FERS and Waveform Digitizers: two alternative and complementary solutions

WAVEFORM DIGITIZERS

- General Purpose Instrument

- Specialized by FW and SW (high flexibility)

- Digital Pulse Processor

- High Data Throughput

- Large Memory Buffers (GB)

- Open FPGA for customization with Sci-Compiler

- DPP designed by CAEN: multi-parametric DAQ

- Need Front-End (Preamp)

- Rack-mount electronics

FERS

- Based on ASIC chips

- Specialized by HW (the ASIC makes the specs)

- Analog Pulse Processor

- Low Data Throughput

- Small Memory Buffers (kB)

- All-in-one readout chain (from detectors to PC)

- Scalability

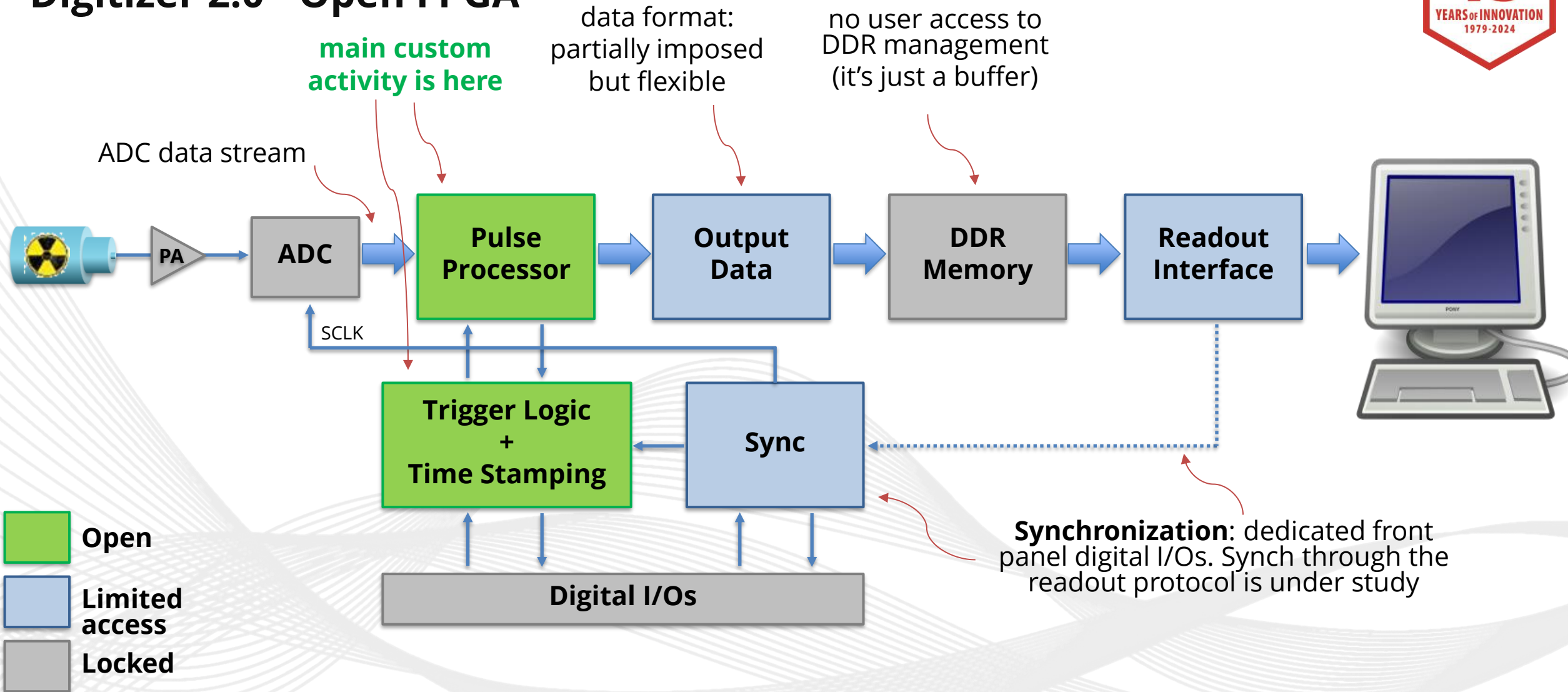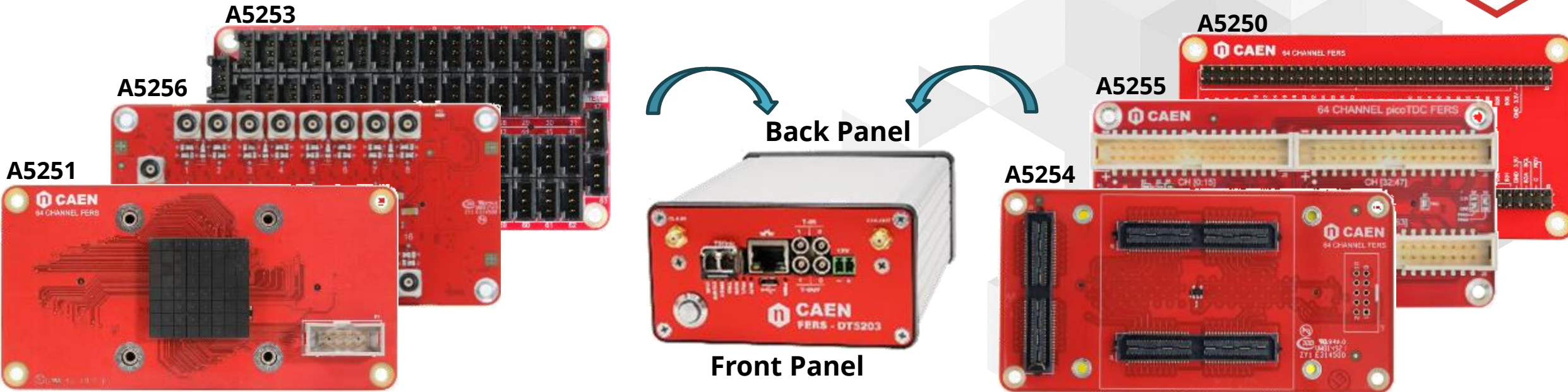- Low cost per channel

- Distributed electronics

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Thank you!

Backup Slides

Digitizer 2.0 - Open FPGA

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main custom activity is here

data format: partially imposed but flexible

no user access to DDR management (it's just a buffer)

ADC data stream

Block diagram flow: Radioactive source → PA → ADC → Pulse Processor → Output Data → DDR Memory → Readout Interface → Computer

ADC → SCLK feedback

Trigger Logic + Time Stamping ← → Sync → Digital I/Os

Synchronization: dedicated front panel digital I/Os. Synch through the readout protocol is under study

Open (green)
Limited access (blue)
Locked (gray)

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Adapters and Extensions

A5253

A5256

A5251

A5250

A5255

A5254

Back Panel

Front Panel

A5260: Remotization cable

FERS-5200: block diagram
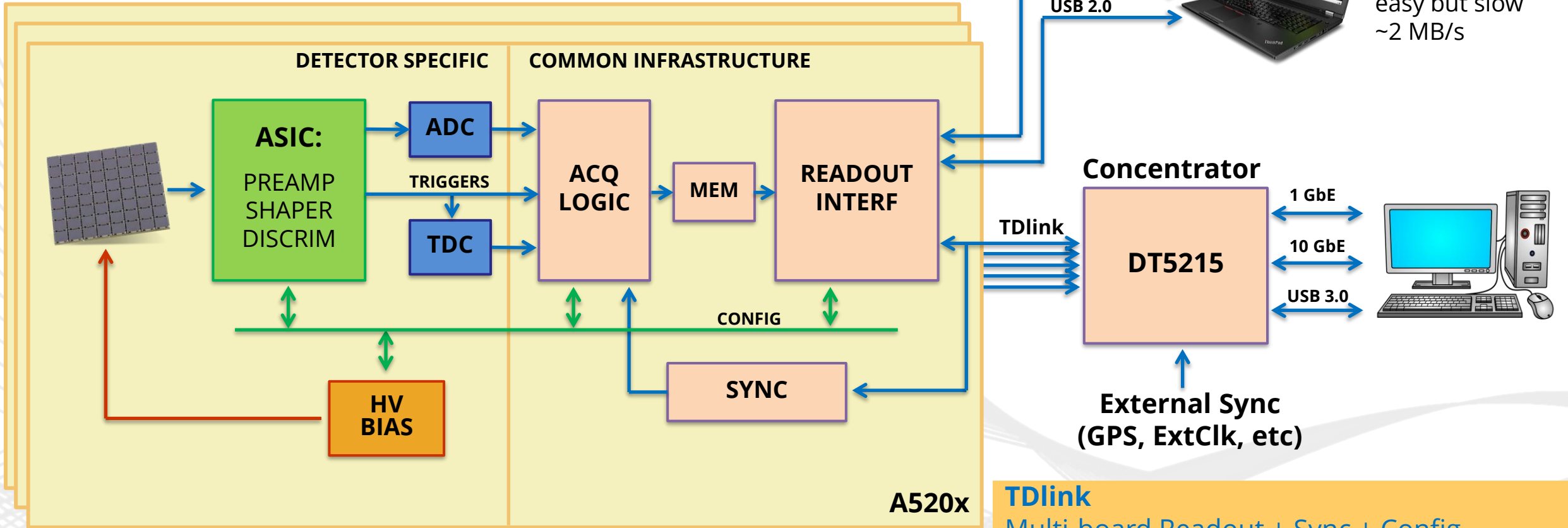
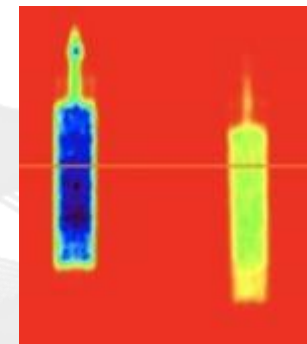# picoTech ProVision PET scanner

Poster N-01-051
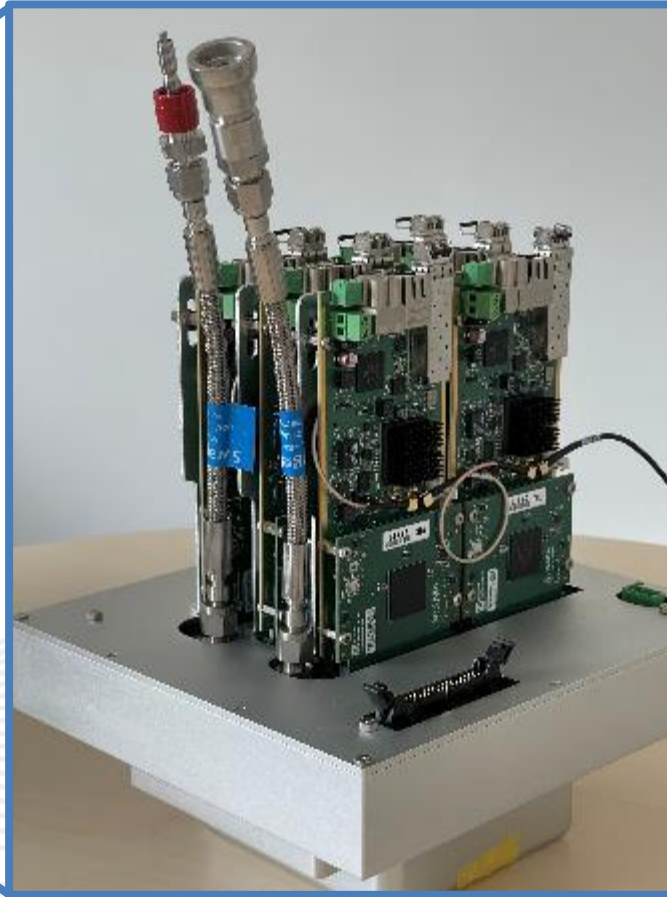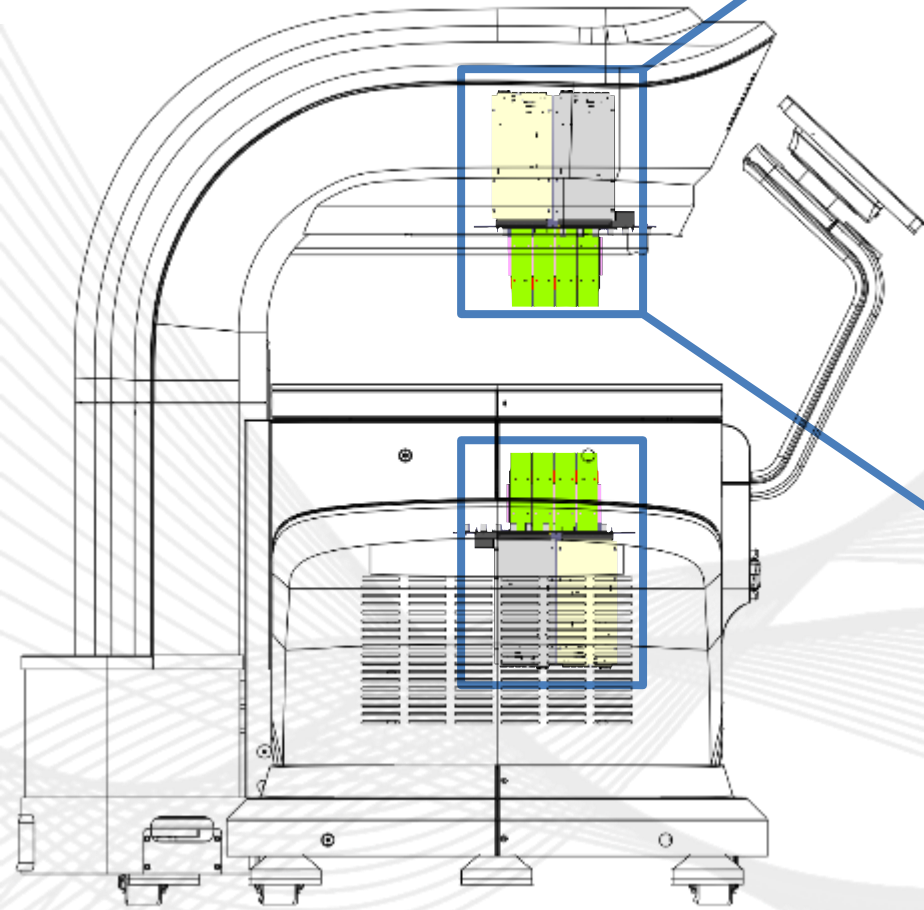
- 2x768 SiPM channels
- 2x6 A5203Bs (128 ch. TDC)
- 1 DT5215 Concentrator
- Precise timing and TOT measurement
- High throughput – almost zero deadtime
- ToT cut for Dark Count and noise suppression

Courtesy of C. Williams
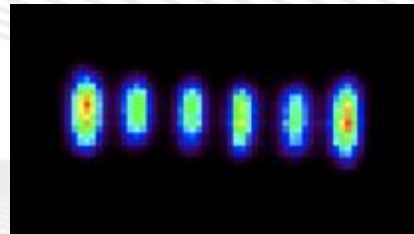
4 mm thick Sodium disks separated by 4 mm gaps

2 syringes filled with FDG radiotracer (activity ratio 3:1)

Silent Border

Cosmic Ray Tomograph for identification of hazardous and illegal goods hidden in Trucks and Sea Containers

- 221.184 Fibers + SiPMs

- 1 mux = 64 SiPMs = 4 FERS channels (X+, X-, Y+, Y-)

- 216 A5202 FERS units

- 3 DT5215 (Data Concentrator)

Mux Constellation