# SRO chips at OMEGA

**XII** Streaming Readout Workshop Tokyo
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Organization for Micro-Electronics desiGn and Applications

# Experience with SRO at OMEGA

- CATIROC (2014) : JUNO SPMT readout  (installed)
- *HARDROC3 (2014) : CALICE RPC digital calorimeter readout (prototyped)*
- HKROC (2022) : PMT readout for HyperK (prototyped)
- CALOROC (2025) : SiPM readout for EIC (in design)
- EICROC (2026) : AC-LGAD readout for EIC (in  design)
- Strong interest for SRO as a way to decrease power consumption in VFE

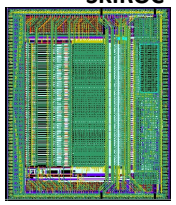
# ASICs produced and installed on detectors since 2006

Omega

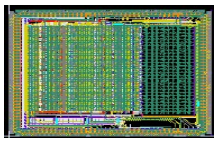




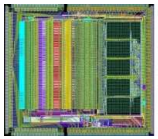

SKIROC



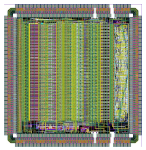
SPIROC



MICROROC

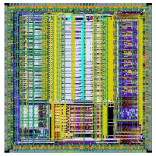


MAROC3

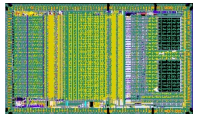


2006

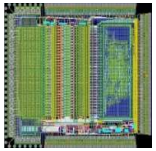
SPACIROC



HARDROC



PETIROC

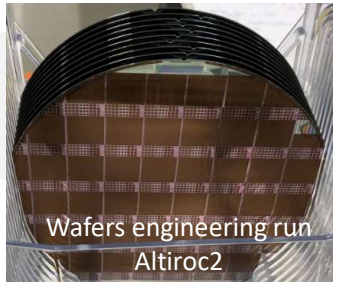




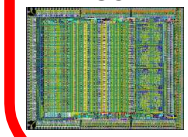
**9 engineering runs in 9 years :**

AMS SiGe 0,35um 2014, 2016, 2018

TSMC 130nm: 2019, 2020, 2021, 2022 and 2023 (x2)

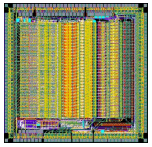



TRIROC



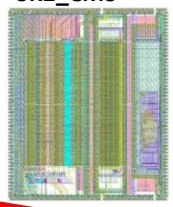


CITIROC



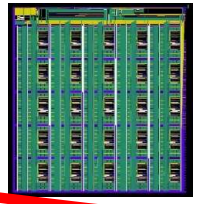
CATIROC

SK2_CMS



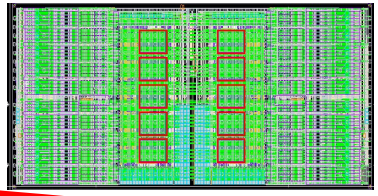
ATLAS EXPERIMENT

ALTIROC1

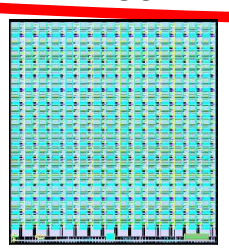



ATLAS EXPERIMENT

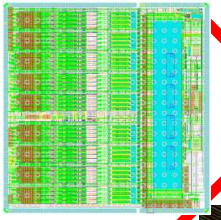
HGCROC



ALTIROC2

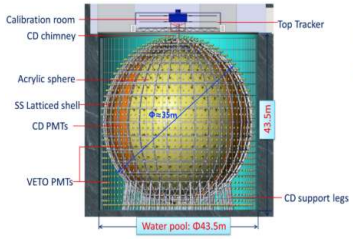


HKROC



HYPER HK

2023

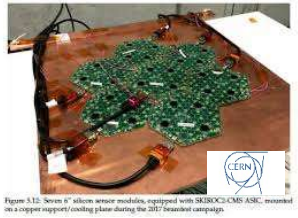
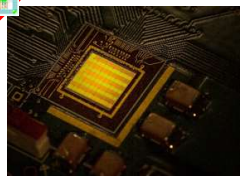



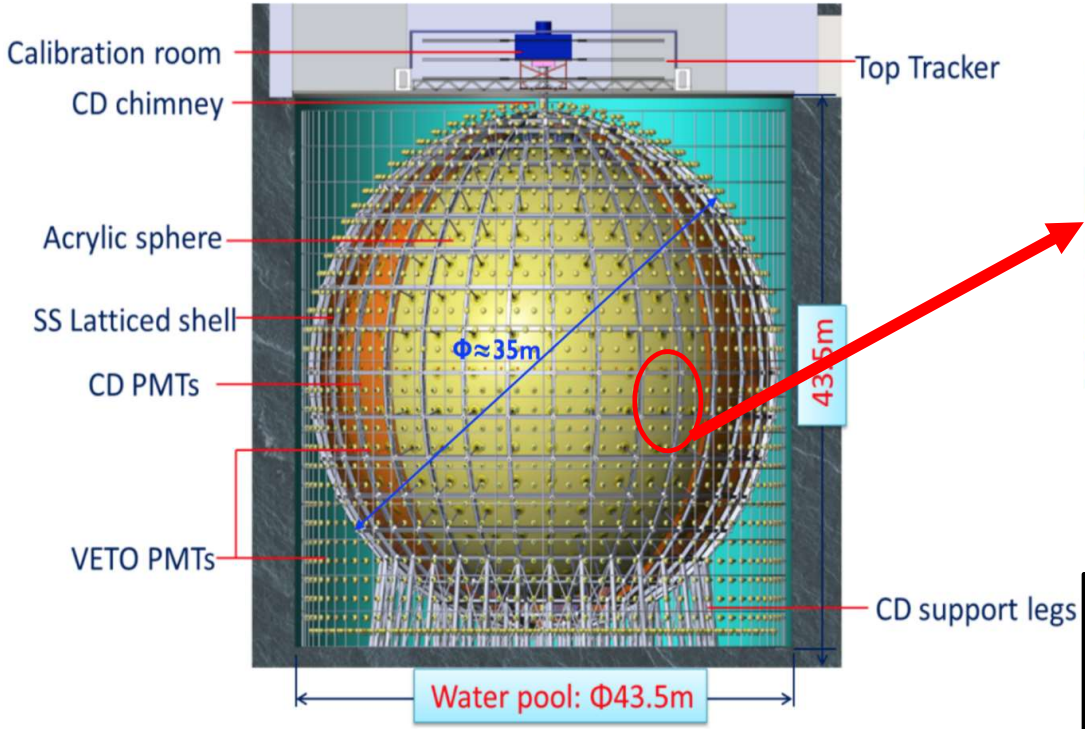

Figure 3.12: Seven 6" silicon sensor modules, equipped with SKIROC2-CMS ASIC, mounted on a copper support/cooling plane during the 2017 beamtest campaign.

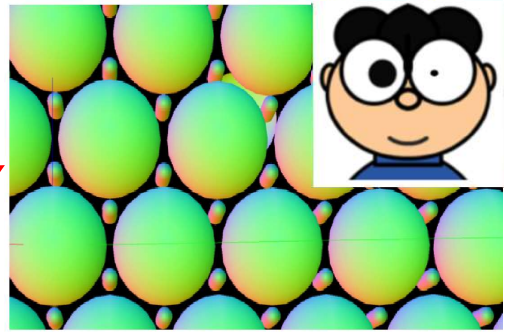


le SRO XII 3

# CATIROC : SPMT readout at JUNO

A multipurpose **neutrino experiment** designed to determine neutrino mass hierarchy with a **20,000 tons liquid scintillator detector** at 700-meter deep underground

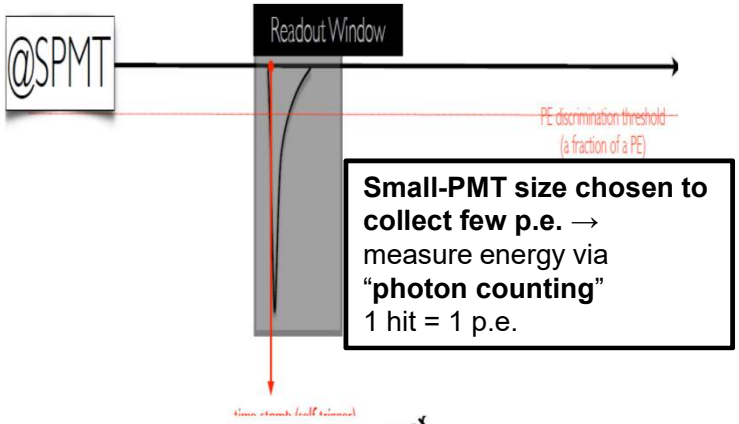



~ 18,000 PMTs (20” diameter) → Large-PMT system (LPMT)
→ **75 % of the inner surface**
~ 25,000 PMTs (3” diameter) → Small-PMT system (SPMT)
→Increase coverage of the surface → Improve energy reconstruction
- Cross calibration

# Small PMT (SPMT) system



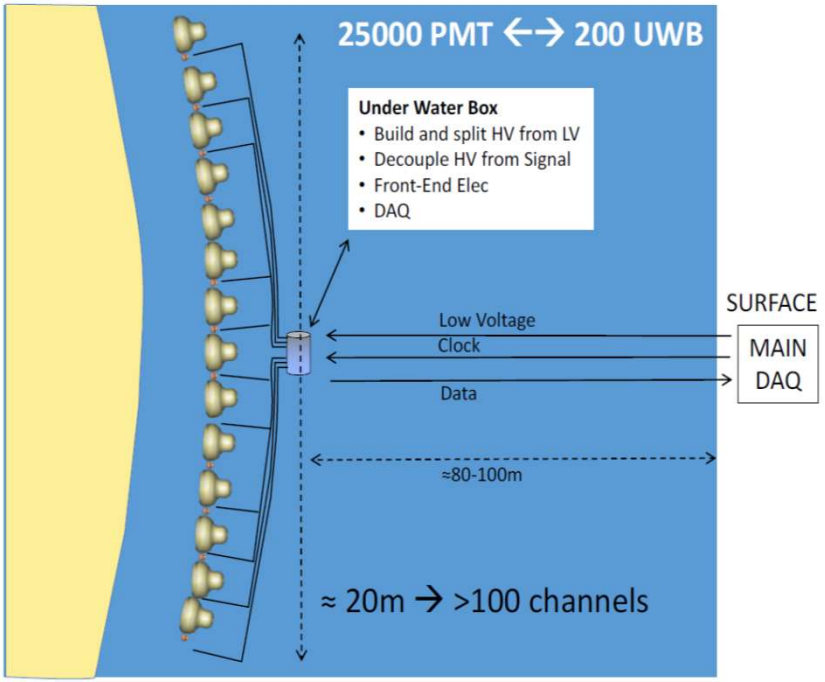


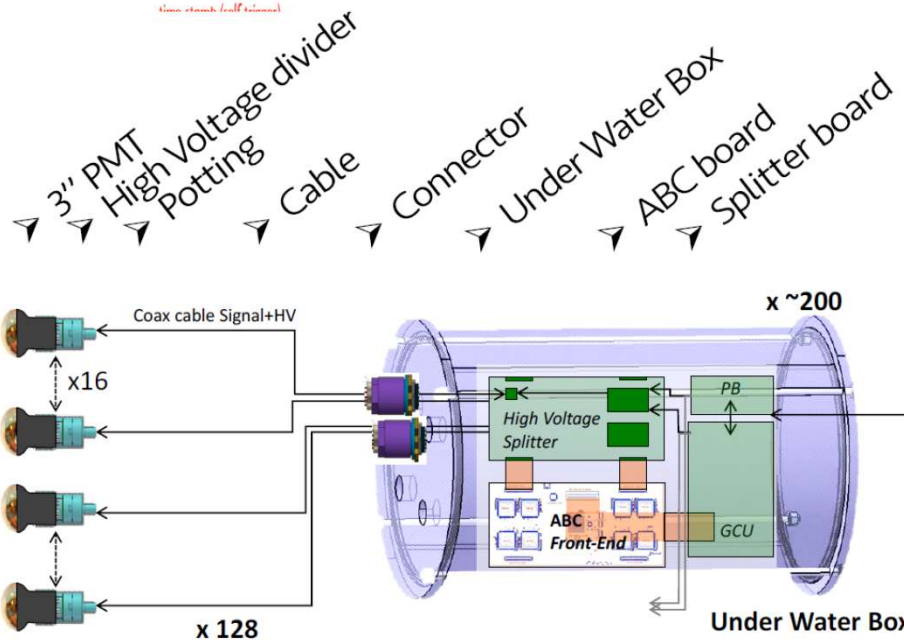

**Small-PMT size chosen to collect few p.e.** → measure energy via "**photon counting**"
1 hit = 1 p.e.

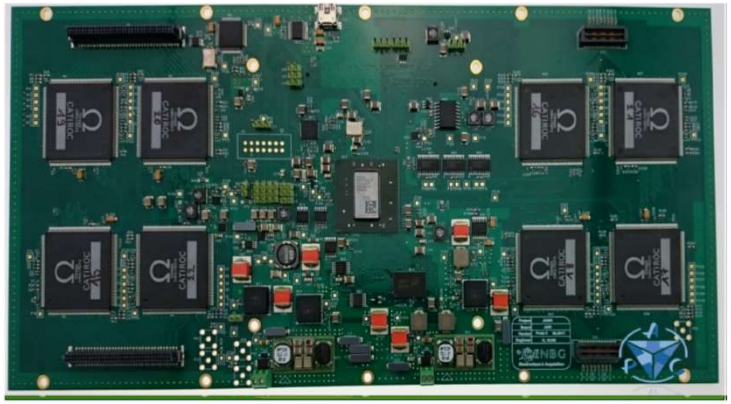
- **128 Small PMTs** with a read-out system:

**the Under Water Box (UWB)**

- A dedicated FEB based on **CATIROC**



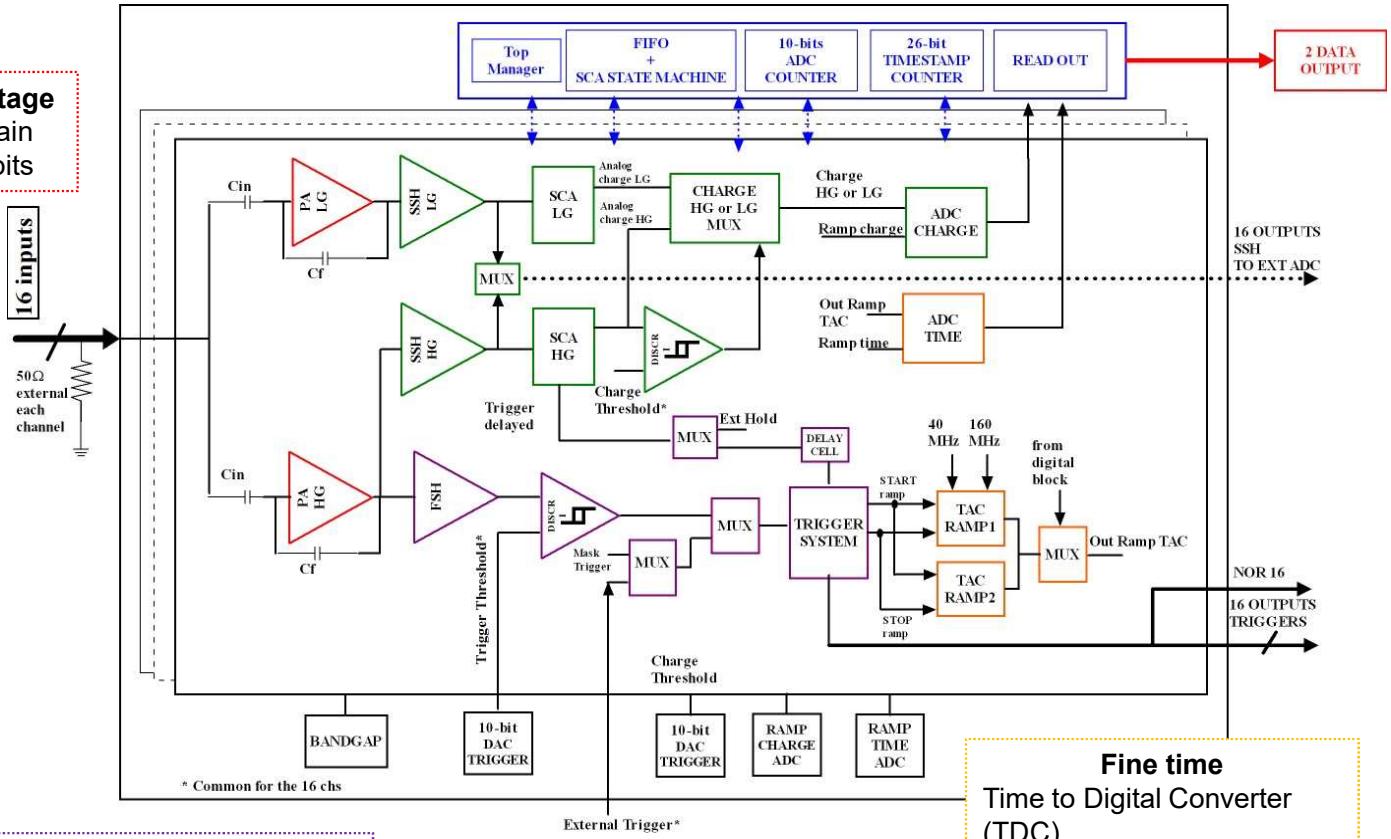
# CATIROC schematic

**Charge path**
- Shaping (variable shaping time)
- Switched capacitor array (**2 Capacitors: ping-pong mode**)
- 10 bits ADC conversion @ 160 MHz
- **50 fC ÷ 70 pC (PMT gain $10^6$)**

**Coarse time**
by 26-bit gray counter
(Digital part) 25 ns steps

**Amplification stage**
with variable gain
ch by ch on 8 bits

16 negative inputs

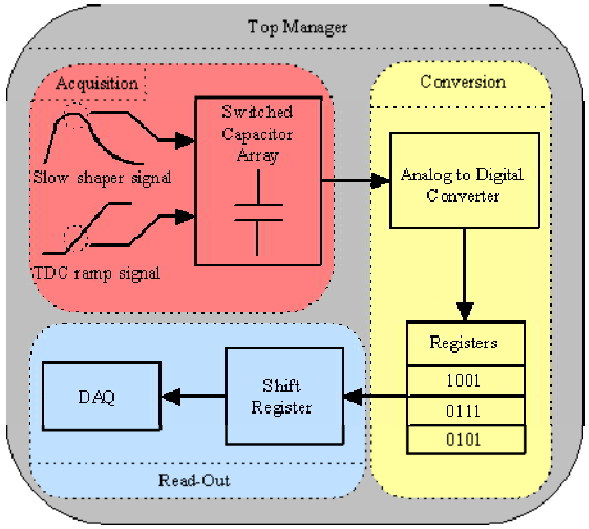



**Trigger path: AUTO TRIGGER DESIGN**

**Fine time**
Time to Digital Converter (TDC)
25 ns dynamic rang
Time resolution: 170 ps
Non linearity: +/- 500 ps

# Digital part

All channels are handled independently
by the digital part
and only channels that have created triggers
are digitized, transferred to the internal memory
and then sent-out in a data-driven way.




The **digital part** manages:

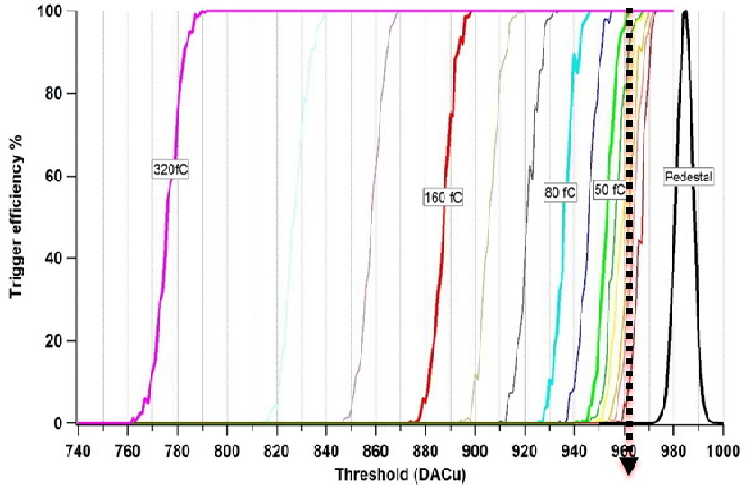
**Acquisition**: Analog memory: 2 depths for HG and LG

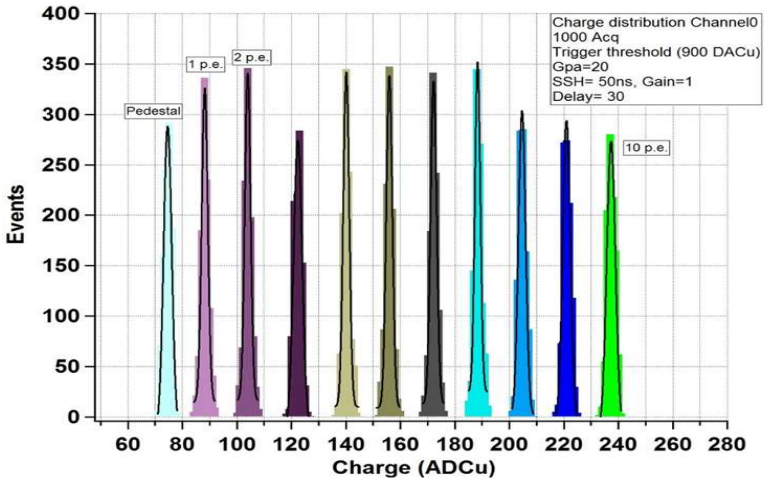
**Conversion**: Analog charge and time into 10 bits digital values saved in the register (RAM)

**Read Out**: RAM read out to an external system

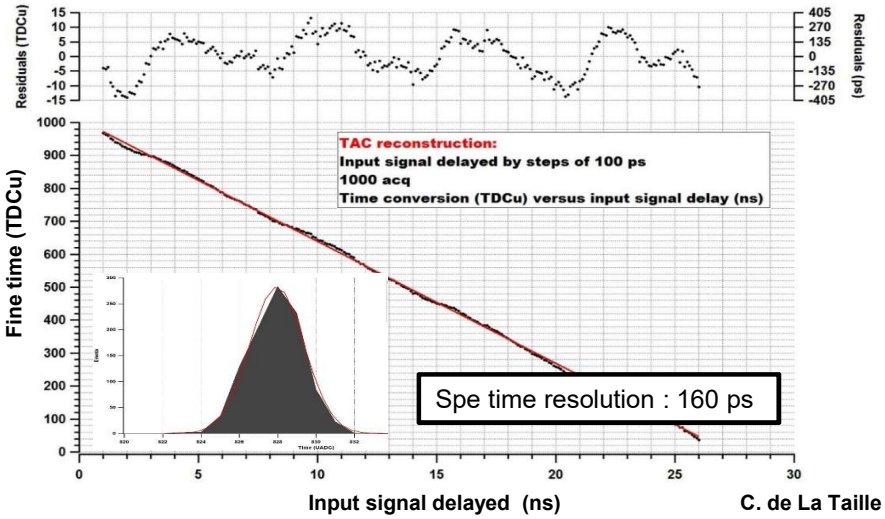
- Readout clock : **80 MHz**
- Max Readout time (16 ch hit) : **3 µs**
- **50 bits of data / hit channel**
- **Readout format** (MSB first) : **coarse time**= 26 bits ; **channel number**= 3bits; **fine time**=10 bits, **charge**=10 bits, **gain**=1 bit

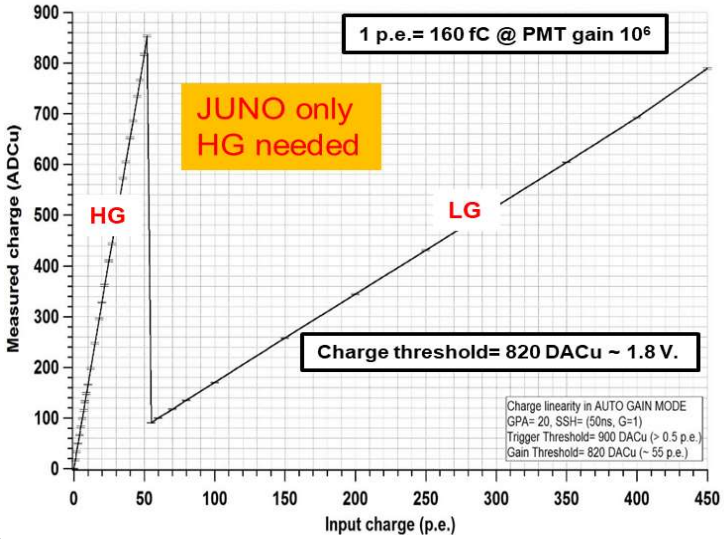
# Performance




Minimum Threshold
@ 968 DACu ~ 28 fC **< 1/3 of pe**



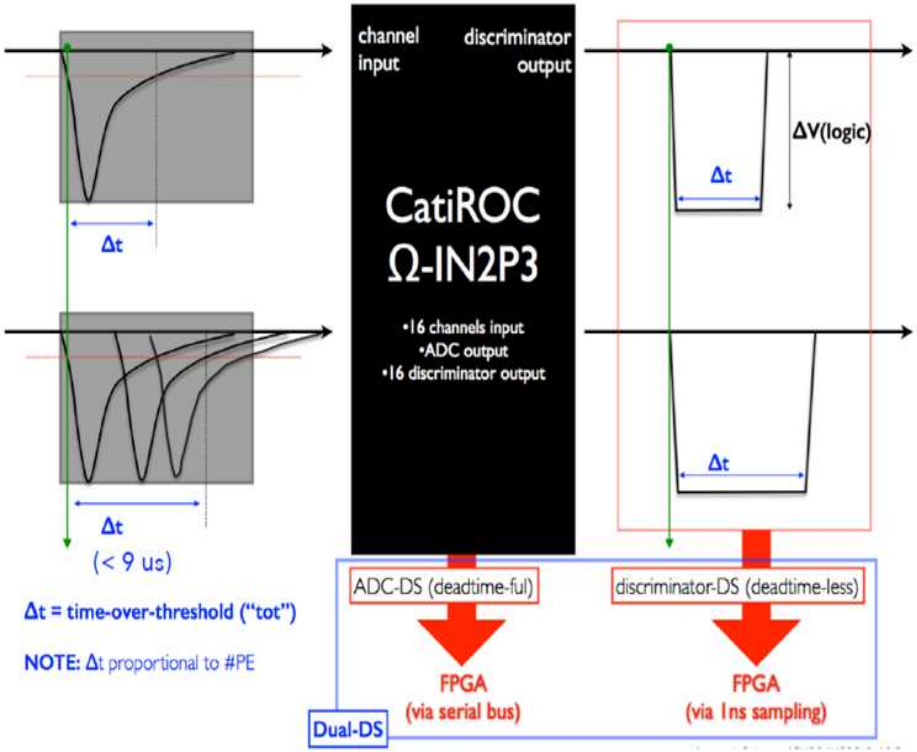
# Hit rate measurements

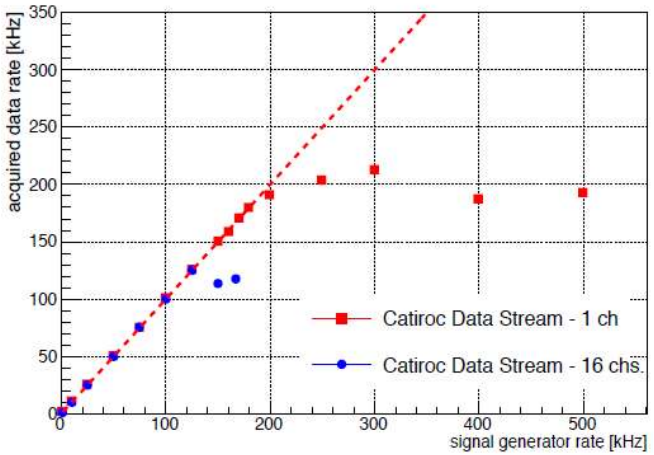
SPMT

| HIT RATE | | | |
|---|---|---|---|
| Tconv (1 ch) | 6.4 µs | Tconv (16 ch) | 6.4 µs |
| Tread-out (1 ch) | 0.36 µs | Tread-out (16 ch) | 3 µs |
| Tcycle (1 ch) | 6.8 µs | Tcycle (16 ch) | 9.4 µs |
| **Hit rate (1 ch)** | 150 kHz | **Hit rate (16 ch)** | 100 kHz |

$$Tconv = \frac{2^n}{F_{conv}} = 6.4\ \mu s$$

$$TRO = \frac{n^\circ\ of\ channels * number\ of\ bit}{F_{RO}}$$



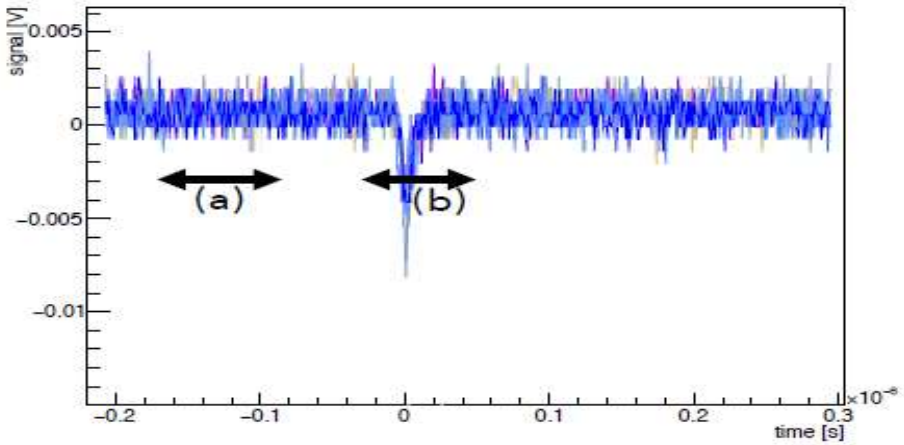




16 trigger outputs: a cross check and a Double DATA Stream (DDS):

- Photon counting
- ToT up to 6 p.e.

# Single p.e. with PMT + Catiroc

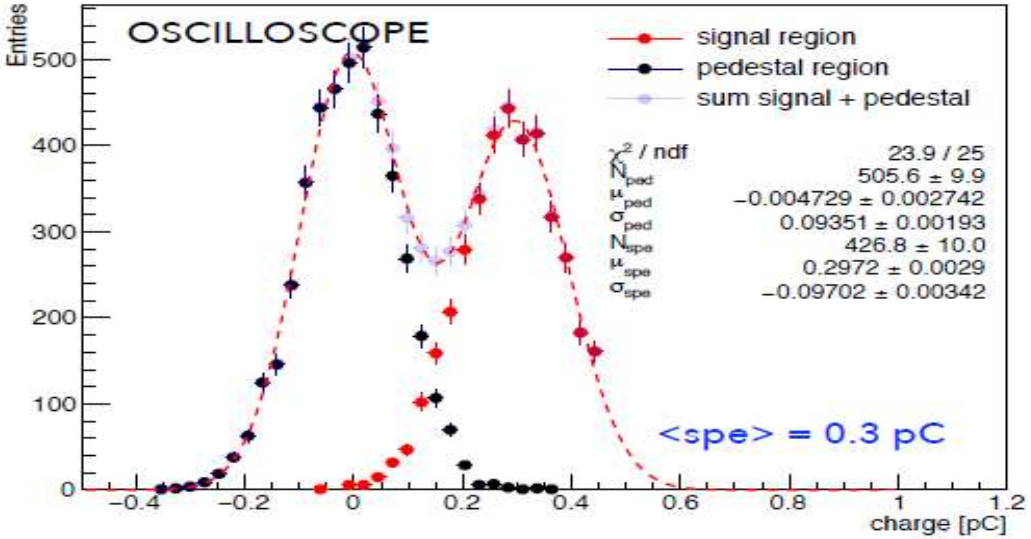


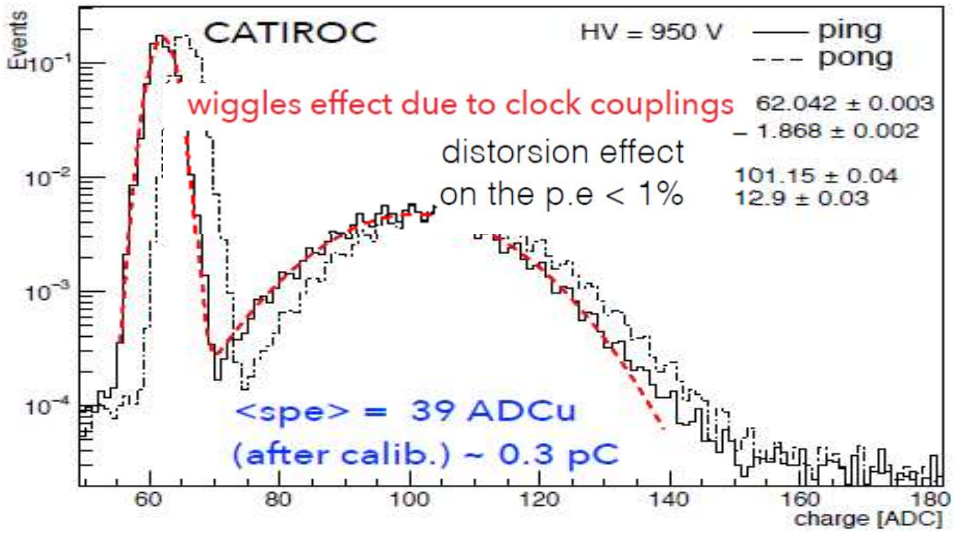



1. WITH OSCILLOSCOPE
   - Pedestal measured in the pre-trigger region (a)
   - Signal measured in the trigger region (b)

2. WITH CATIROC
   - trigger threshold sets very low (950 DACu) to allow the observation of the pedestal peak.
   - Two spectra (ping/pong) produced by CATIROC

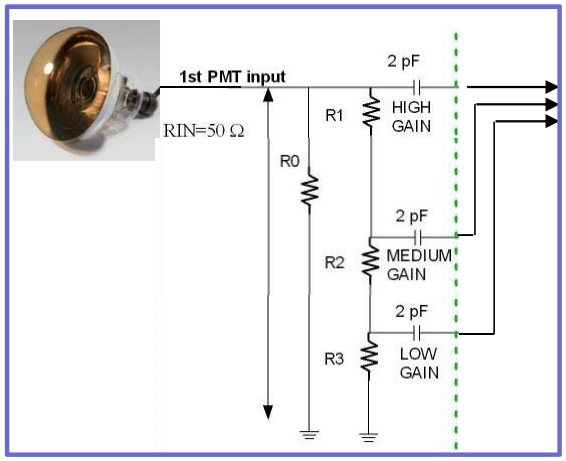
s. p.e. position measured with the two methods well compatible with the

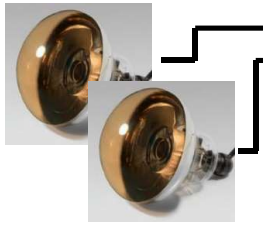


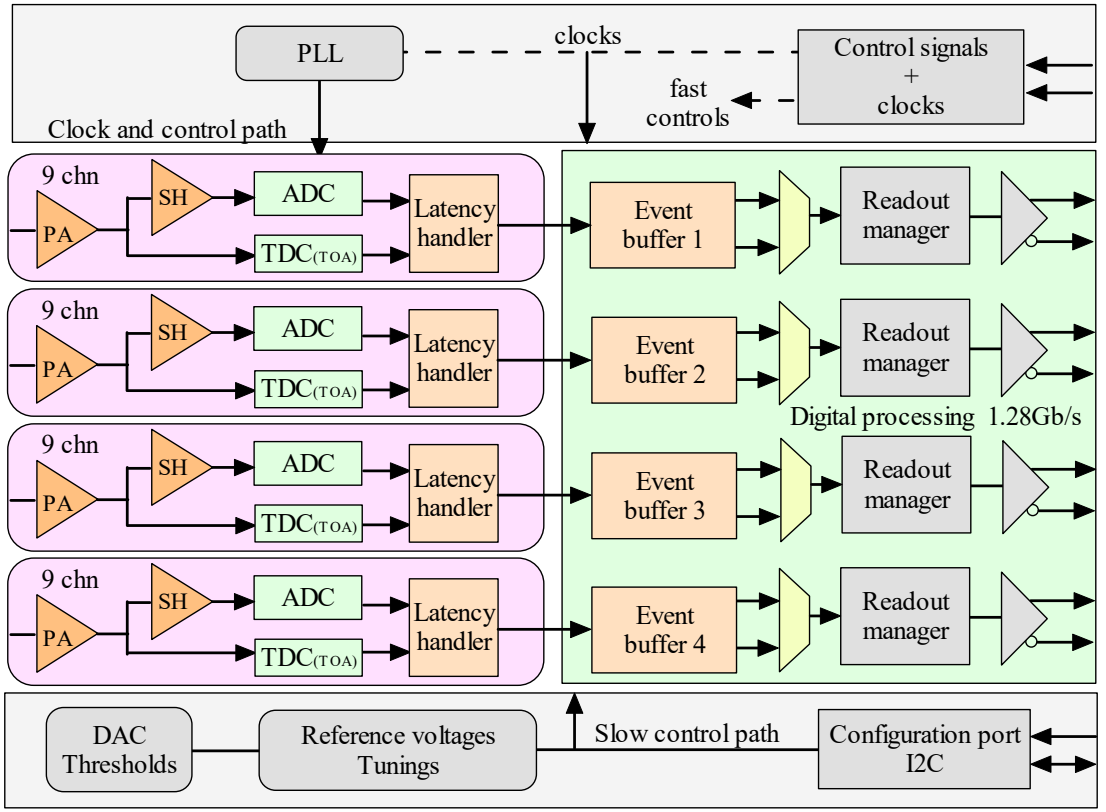



# Evolution : HKROC: waveform digitizer with TDC and auto-trigger

- HKROC is 36 channels: 12 PMTs with High, Medium and Low gain
  - Or 36 PMTs with one gain



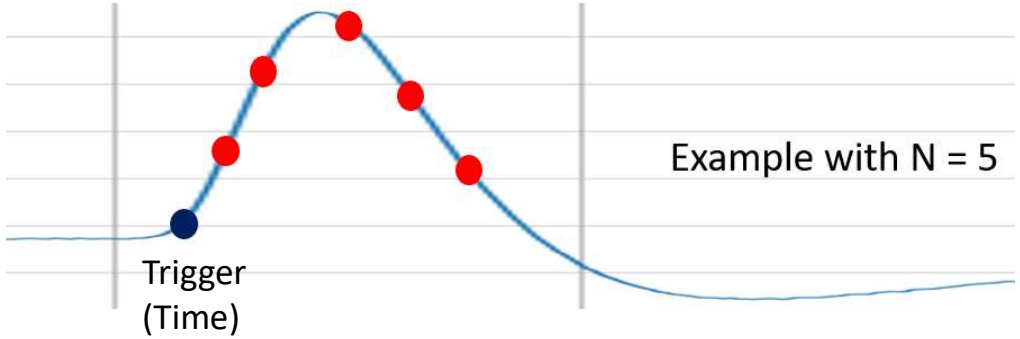




- ASIC in TSMC 130 nm node
- Low power: 10 mW per channel
- Large charge measurement with 3 gains (up to 2500 pC)
- Integrated timing measurements (25 ps binning)
- Readout with high speed links (1,28 Gb/s)
- HKROC is a waveform digitizer with auto-trigger

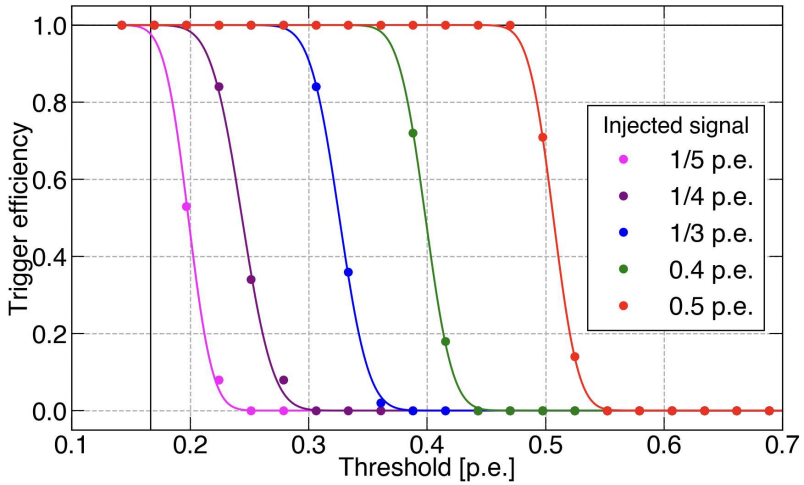
# HKROC : PMT SRO R/O

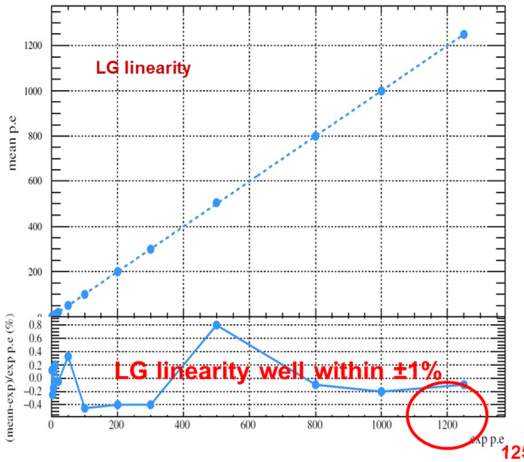
- HKROC is a charge/time measurement ASIC
  - Intended for PMTs readout at neutrino experiment
  - Slow channel (30 ns) for charge measurement
    - waveform digitizer working @ 40 MHz
    - Number of charge sampling points from 1 to 7
  - Fast channel for precise timing (25 ps binning)

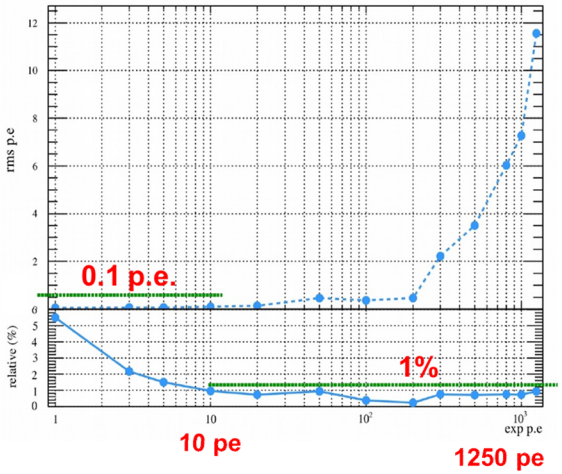



- Auto-trigger on single photoelectron
  - 4 outputs at 1.28 Gb/s
  - Data-driven readout (ch#,ADC,TDC)
  - Hit rate capability up to 0.4 MHz/PMT

# HKROC performance



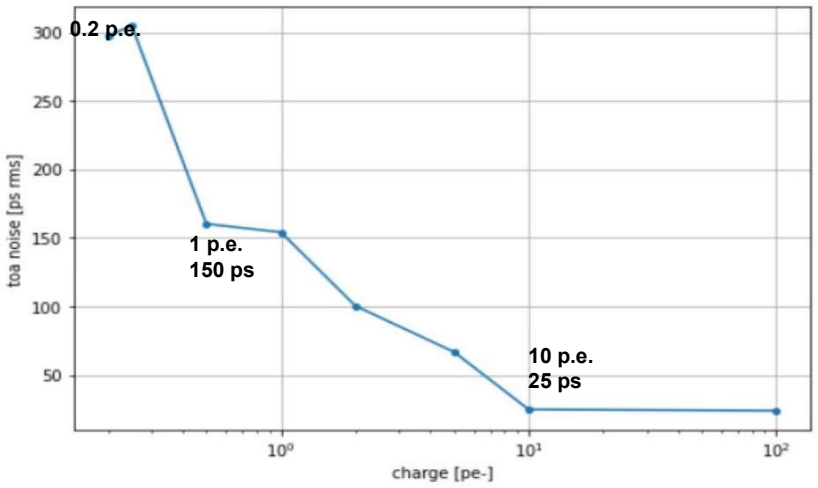

HG, MG and LG tested!!

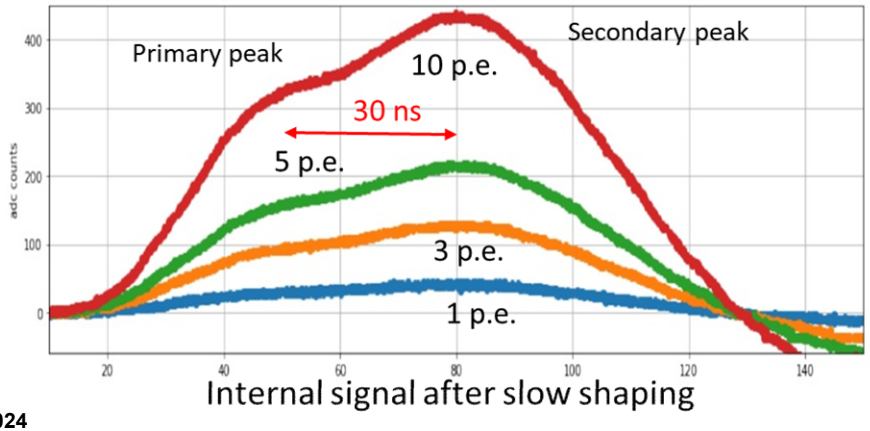
Charge linearity < **±1%** from 1 to **1250 p.e. (2500 pC)**

Charge resolution :

< **0.1 p.e (200 fC)** at ≤ 10 p.e

< 1 % otherwise

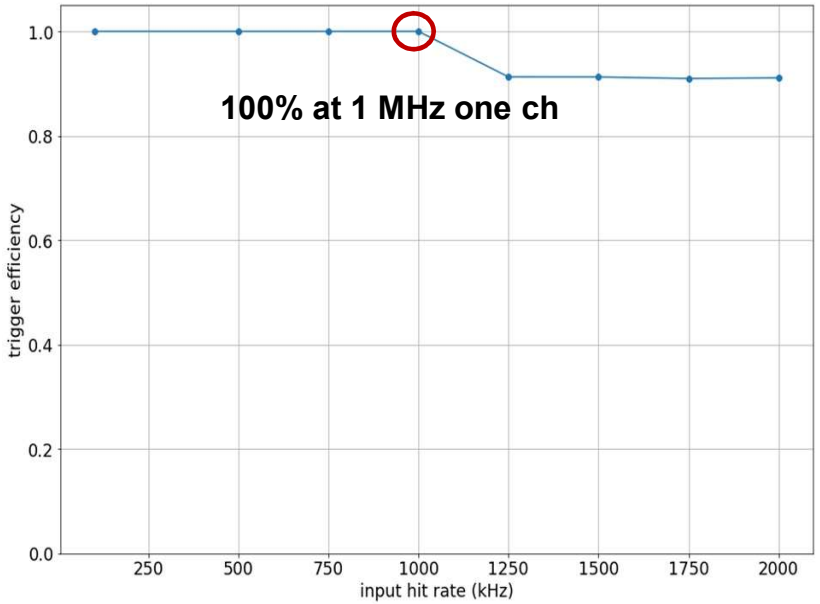


# HKROC Trigger rate measurements

**FAST hit rate (~ 1MHz) required for close Supernova signals (~ 1 p.e.)**

**Normal mode:**

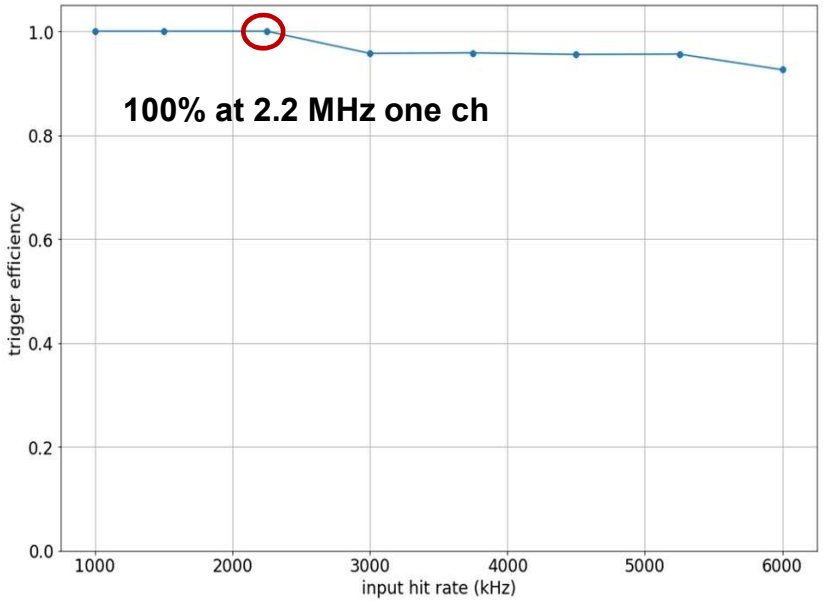



**1 PMT channel →**

**3 HKROC channels** tested in Normal Mode:

**100%** Trigger efficiency up to **415 kHz 3 chs**

**Super Nova mode**




**1 PMT channel →**

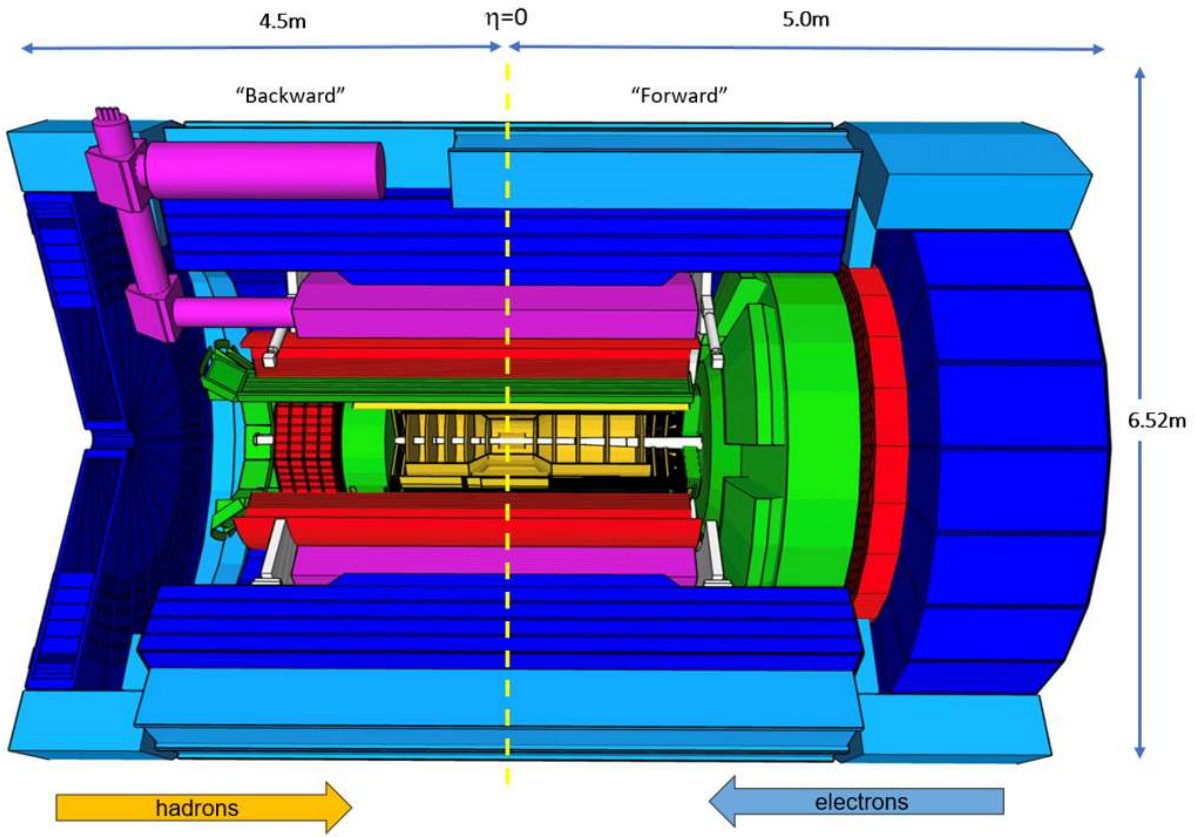
**3 HKROC channels** tested in SuperNova Mode:

**100%** Trigger efficiency up to **950 kHz 3 chs**

The HKROC saturation naturally appears when the chip internal memory is full. The chip has one independent memory for each read-out link at 1.28 Gb/s, which gather 3 PMTs.

# OMEGA chips for EIC

- HGCROC and EICROC considered for EIC calorimetry and AC-LGAD readout

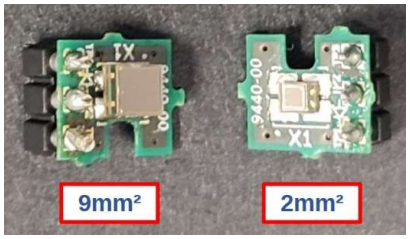


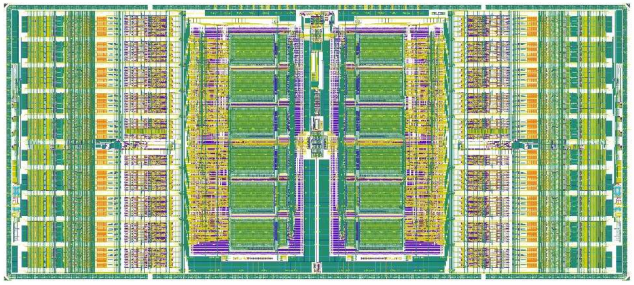

| Detector Group | Channels | | | |
|---|---|---|---|---|
| | MAPS | AC/DC-LGAD | SiPM/PMT | MPGD |
| racking | 32 B | | | 100k |
| alorimeters | 50M | | 67k | |
| ar Forward | 300M | 2.3M | 500 | |
| ar Backward | | 1.8M | 700 | |
| ID | | 3M-50M | 600k | |
| OTAL | 32 B | 7.1M-54M | 670k | 100k |
| SIC | ITS-3 | EICROC<br>FCFD<br>HPsOC<br>ASROC<br>FAST | Discrete/COTS<br>HGCROC3<br>ALCOR-EIC | SALSA |

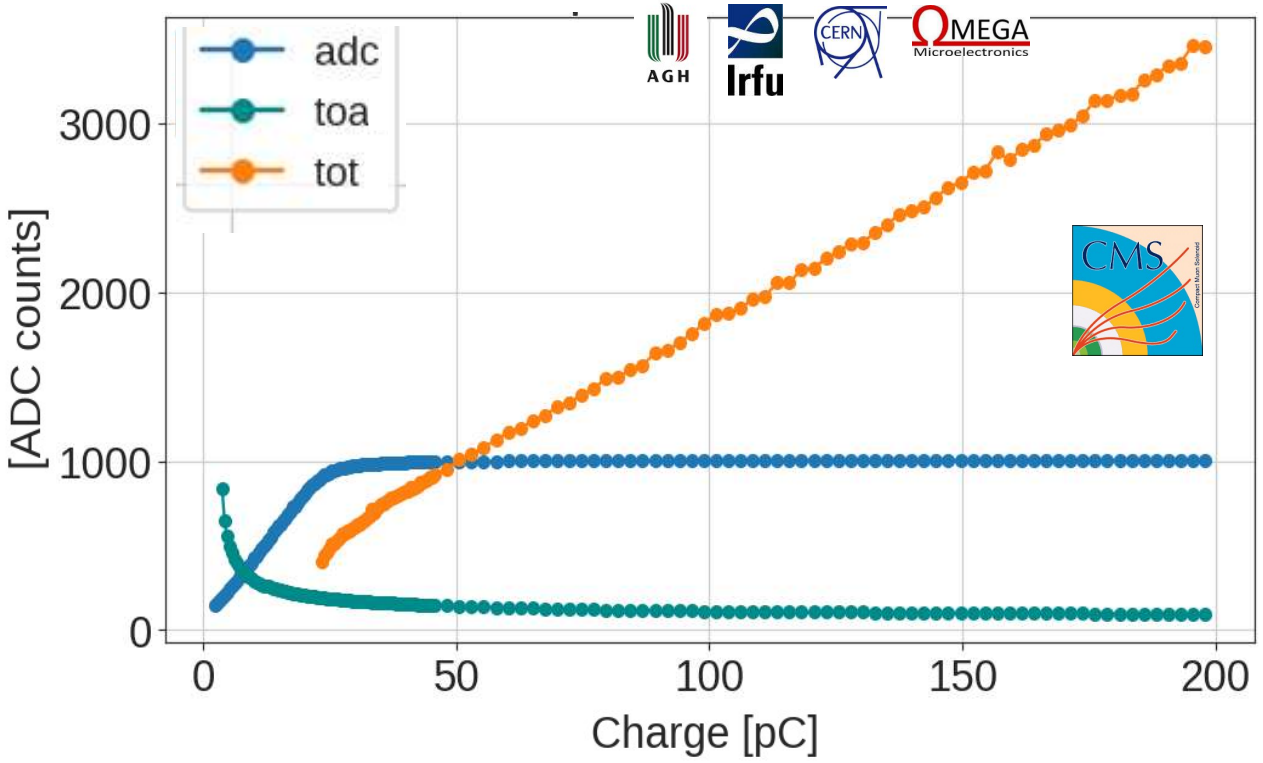
# Calorimetry : SiPM readout experience from CMS (H2GCROC)

- H2GCROC developed for CMS HGCAL is a good candidate to provide charge and time on a large dynamic range

- H2GCROC provides 72 channels with (see backup)
  - Charge measurement from 30 fC (noise) to 300 pC (MIP ~0.5 pC)
  - ToA measurement down to 15 ps
  - Optimized for Cd=500 pF
  - 15 mW/ch. Radiation hard, TMR.

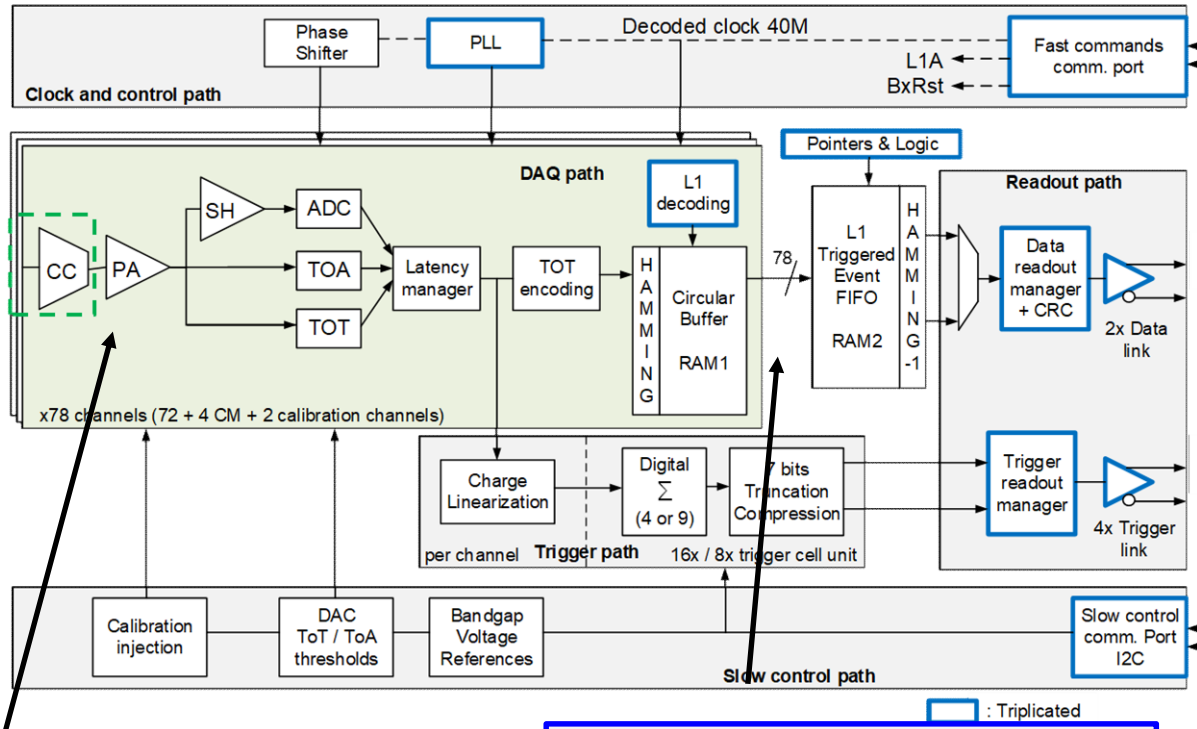




# H(2)GCROC : LHC specific

- HGCROC is designed for LHC : needs a LVL1 trigger




Dedicated fast command interface : calibration pulses, external L1 trigger.

Data and trigger serial links with CLPS signaling (LpGBT @ 1,28 Gbps)

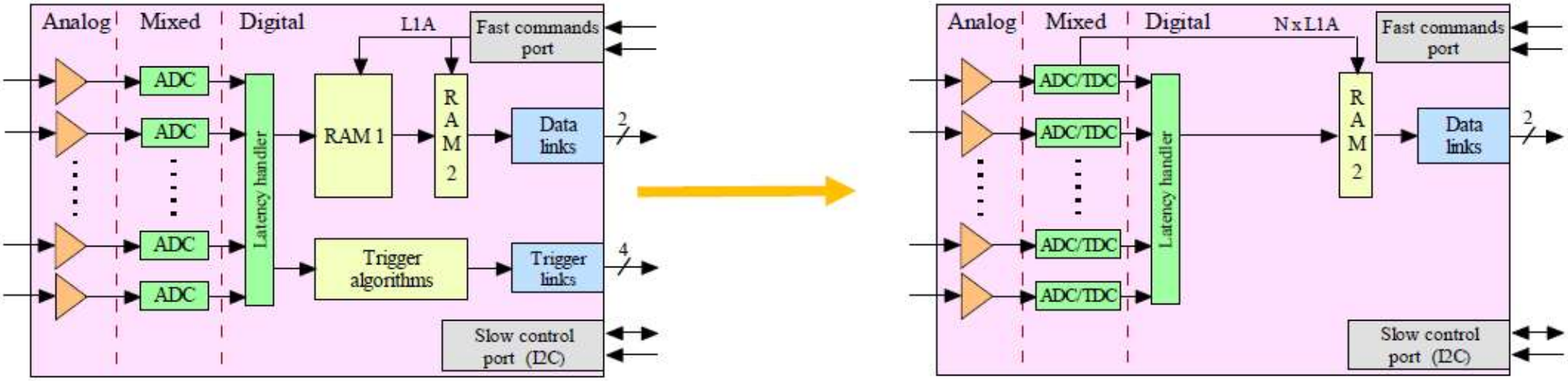
I2C interface to load the ASIC parameters (slow control interface)

Analog front-end specific to sensor

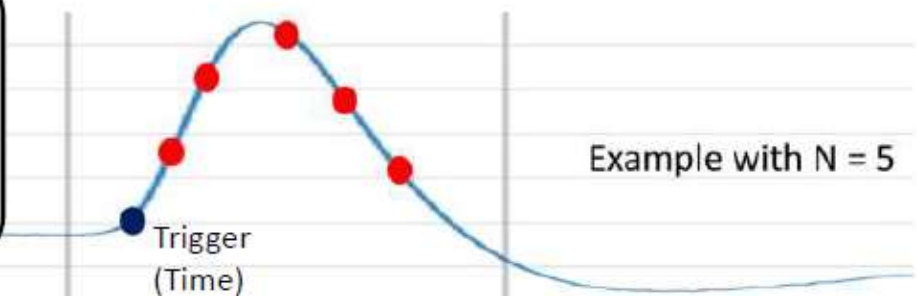
LHC-like structure :
Ram1 for data storage
Ram2 for L1 accepted events

# Evolution for EIC readout : CALOROC

- No more LVL1 : data streaming => auto-trigger and zero-suppress
  - Also very interesting for future DRD6 readout ASICs !

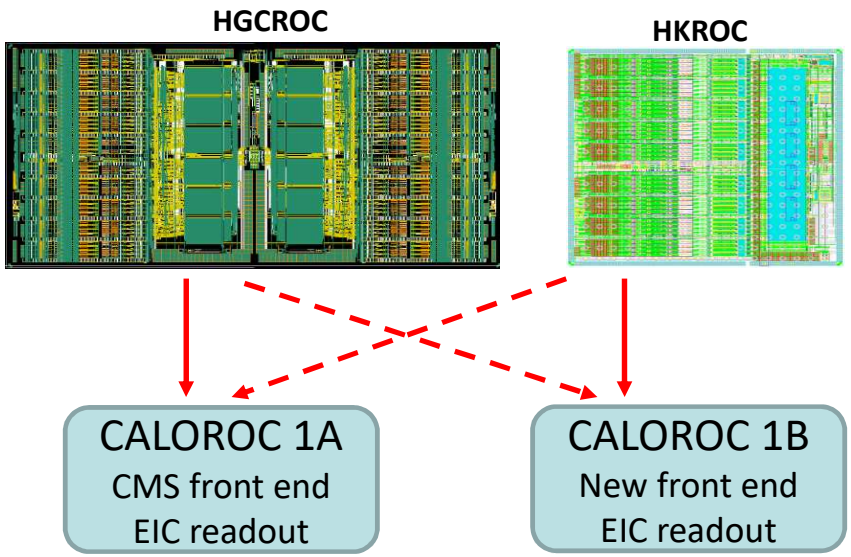



- Each event passing the threshold is readout
- Auto-trigger with N "samples" (1 to 7)
- Can be exercised with present HGCROC (multiple L1A-triggers)



# CALOROC1A/1B development plan

- CALOROC1A is H2GCROC with EIC readout (conservative)
  - Same analog front-end but new digital backend
  - Auto-trigger/zero-suppress : already exercised in HKROC (see backup)
- CALOROC1B is CALOROC1A with a new analog front end (innovative see backup)
  - Better signal to noise ratio (no current conveyor)
  - No ToT : dynamic gain switching
  - Pin-to-pin compatible
- Both chips also provide useful R&D for DRD6



# Common: Rates per channel

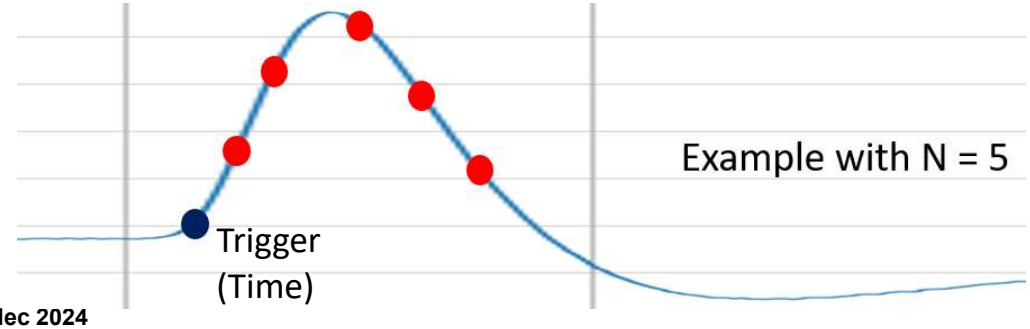
- Present HGCROC rate calculation: 1 serial link for 36 (+2) channels (HGCROC is arranged by 36 channels)

| Version | Number of points (N) | Max rate | Remarks |
|---|---|---|---|
| Present HGCROC-36ch | 1 | 976 khz / ASIC | LHC is 1 snapshot |
| Per channel (1 link/36 ch) | 4 or 3 | 7-9 kHz / chn | Divide by N and by 36 (could be exercised) |
| | | | |
| Caloroc (1 link/18 ch) | 4 or 3 | 24-32 kHz / chn | |
| Caloroc with zero suppress | 4 | 55 kHz / chn | With 6 channels triggered (over 18) |
| | | | |
| | | | |

Present HGCROC

CALOROC

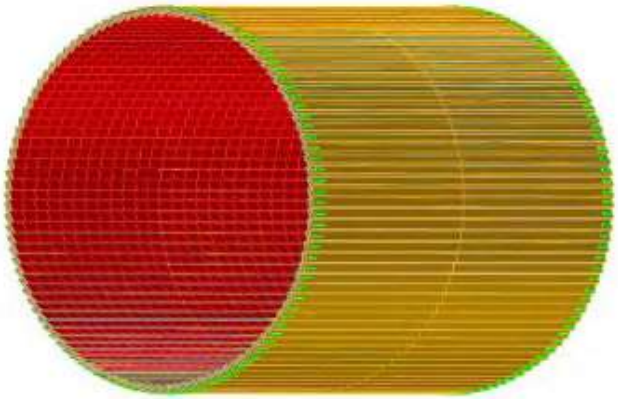
Conclusion: ZS with 2 serial links mandatory



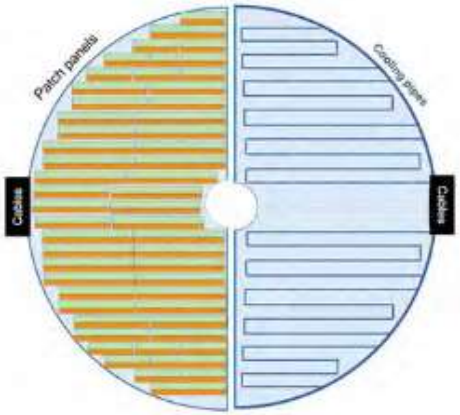
# ePIC AC-LGAD detectors

## Specifications of ePIC AC-LGAD detectors:

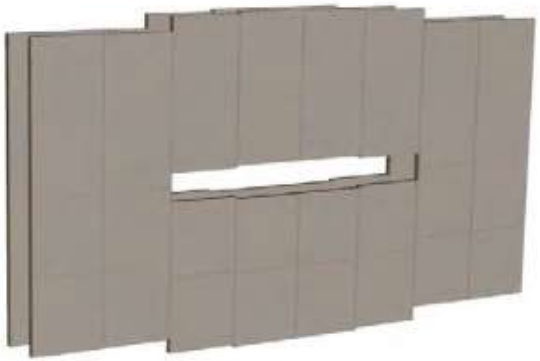
BToF



FToF




Roman Pots

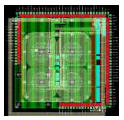


4D Trackers

| | Area ($m^2$) | Channel size ($mm^2$) | # of Channels | Timing Resolution | Spatial resolution | Material budget |
|---|---|---|---|---|---|---|
| Barrel TOF | 10.9 | 0.5*10 (strips) | 2.4M | 30 ps | 30 $\mu m$ in $\varphi$ | 0.01 X0 |
| Forward TOF | 2.22 | 0.5*0.5 (pixels) | 8.8M | 25 ps | 30 $\mu m$ in x and y | 0.08 X0 |
| B0 tracker | 0.07 | 0.5*0.5 (pixels) | 0.28M | 30 ps | 20 $\mu m$ in x and y | 0.05 X0 |
| RPs/OMD | 0.14/0.08 | 0.5*0.5 (pixels) | 0.56M/0.32M | 30 ps | 140 $\mu m$ in x and y | no strict req. |

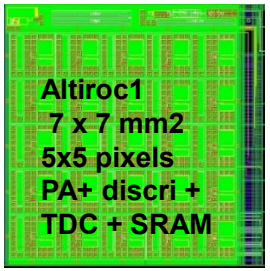
# DC-LGAD readout : experience from ATLAS : ALTIROC

2016



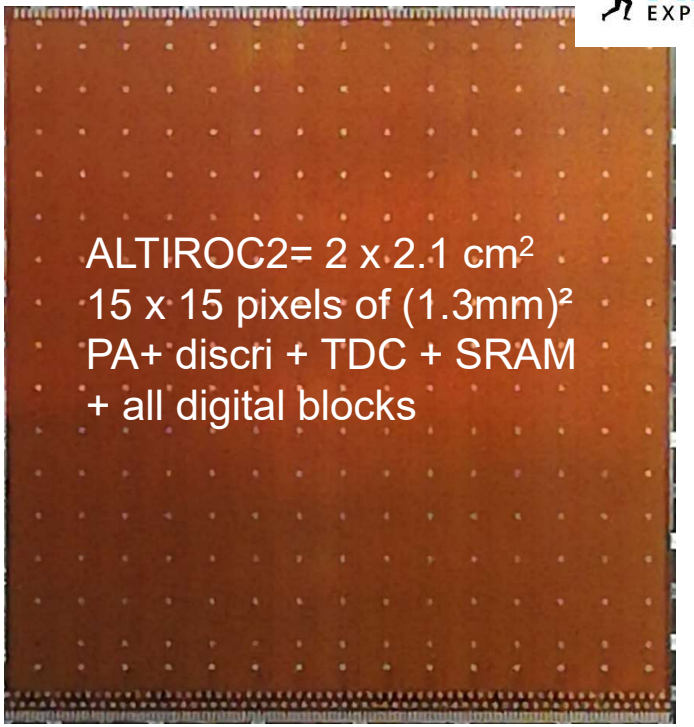
**Altiroc0**
**2 x 2 mm2**
**2 x 2 pixels**
**PA + discri**

2017

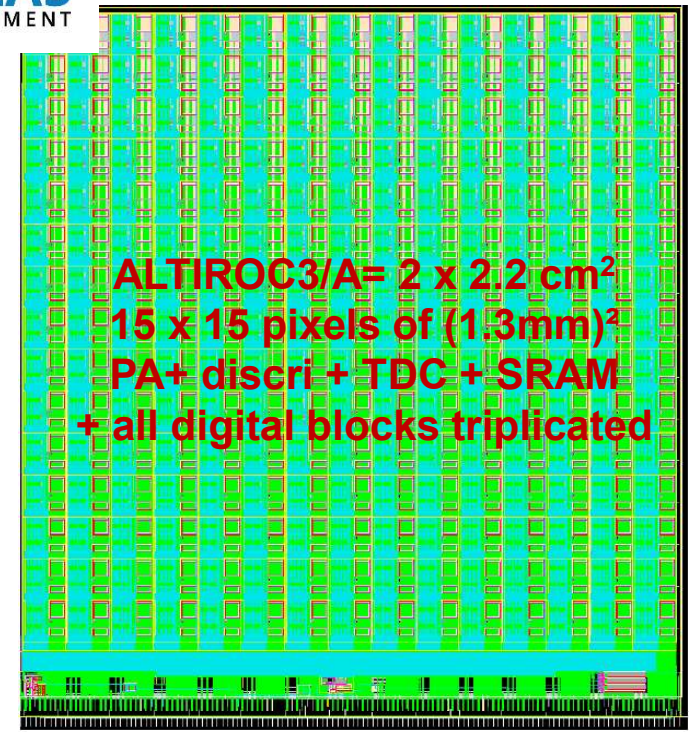



**Altiroc0 and 1:**
No digital,
To validate the FE part at system level (= ASIC bump-bonded onto a sensor)

2019

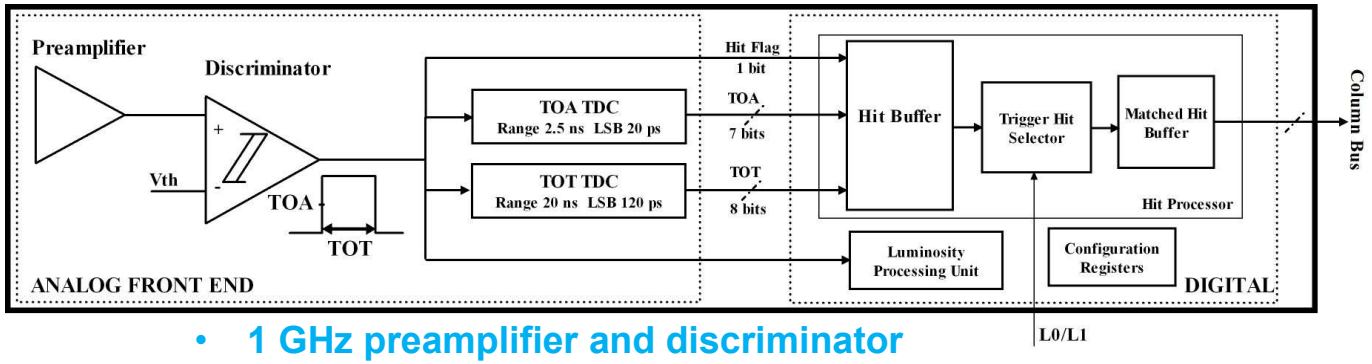



2022

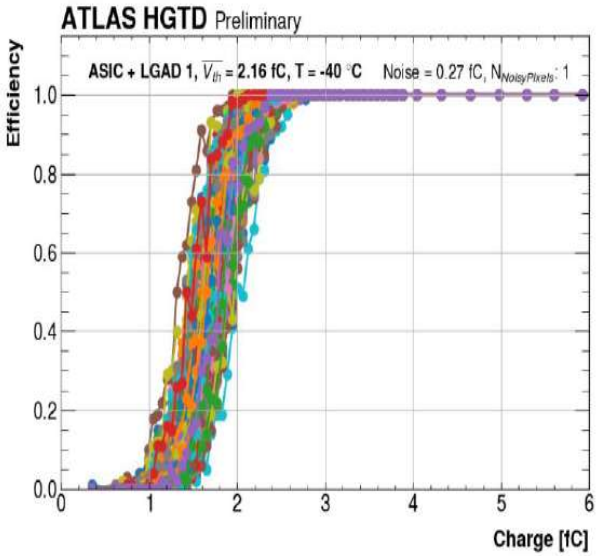


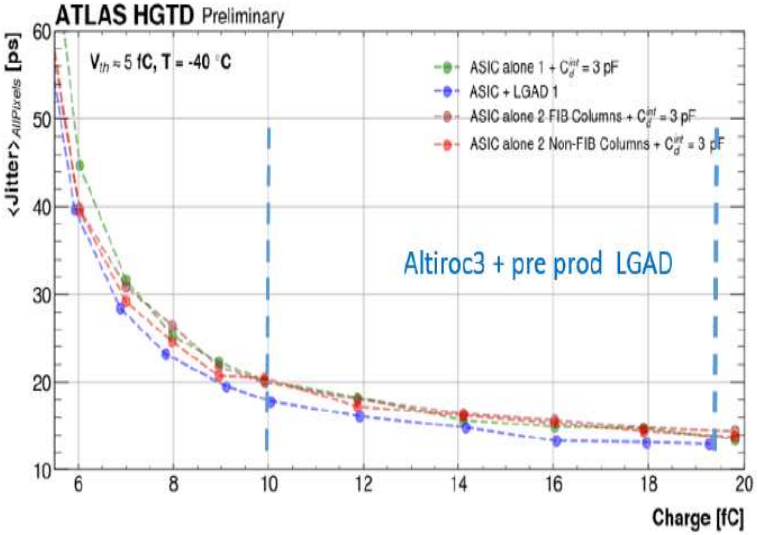

**ALTIROC2/3/A: Digital on Top design**

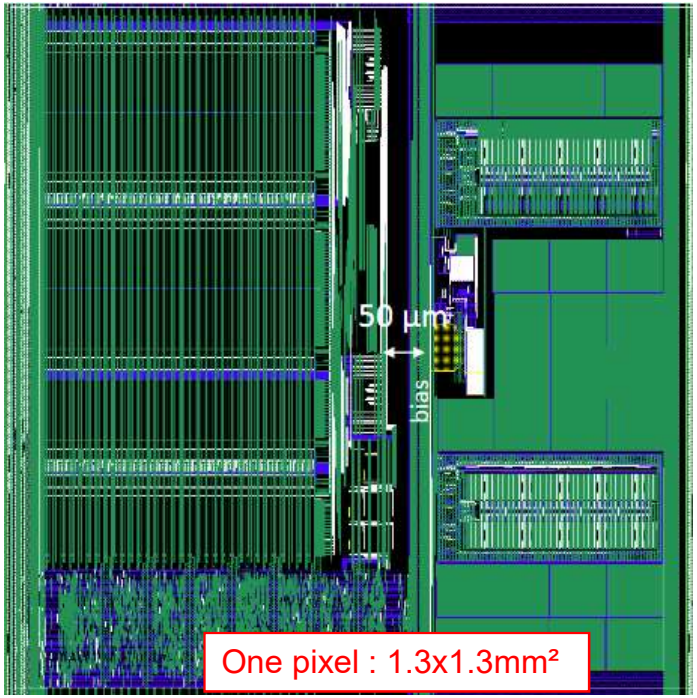
# ALTIROC pixel scheme and layout




- **1 GHz preamplifier and discriminator**
- **2 vernier TDCs for ToA and ToT**
- **Hit buffer:** SRAM 1536 x 19 bit (38 µs latenccy)

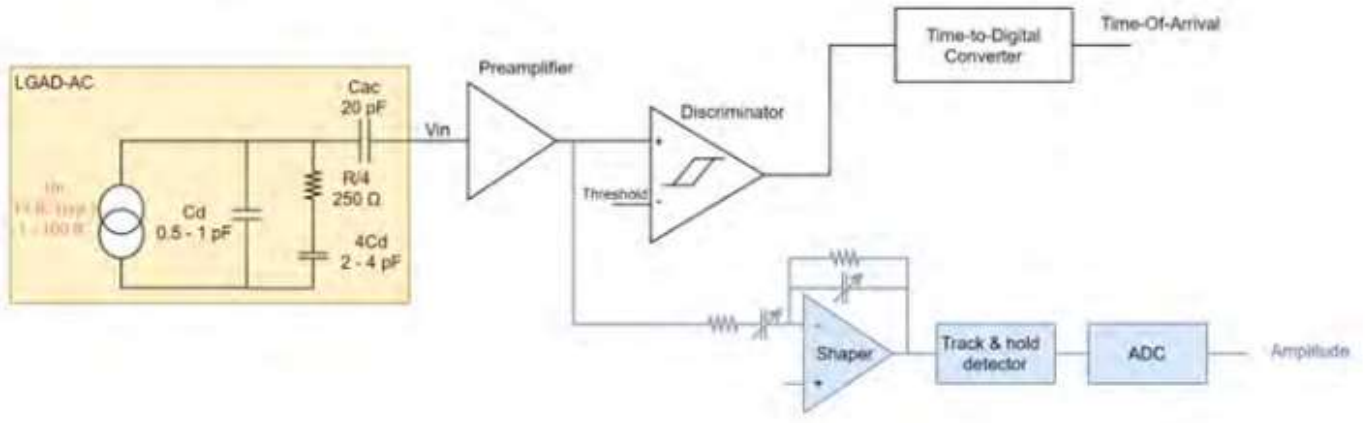


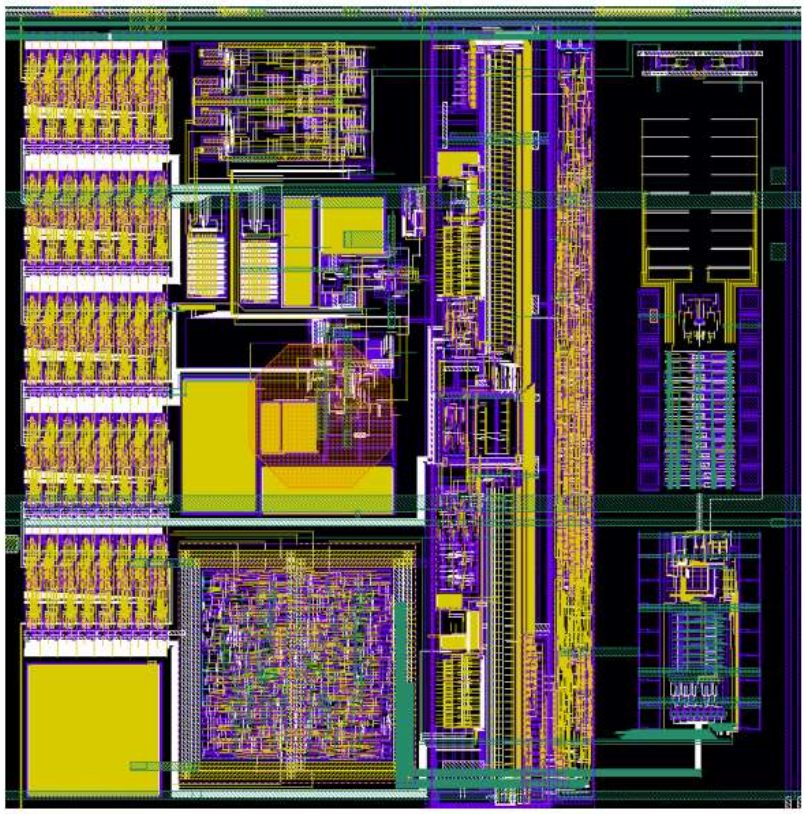



# Adaptation to EIC : EICROC

- Shrink into 500x500 µm
- Analog frontend similar to ALTIROC
- Need ADC instead of ToT for charge measurement 8bit 40 MHz from AGH Krakow
- TDC taken from HGCROC by CEA Saclay
- I²C configuration
- Simple digital readout



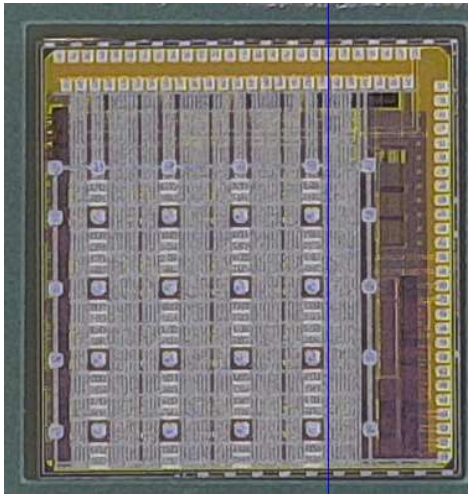



Slow control | PA +discri | TOA TDC | 8b 40M ADC

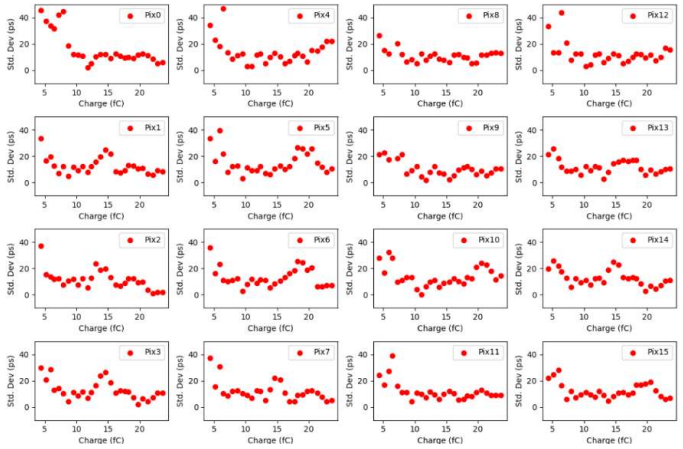
OMEGA Microelectronics | Irfu | AGH

# EICROC0 : 4x4 pixels

- EICROC0 : 4x4 test chip for (500µm)² pixels
  - Readout : TDC data and 8 ADC values
  - Performance : a few examples, more in backup



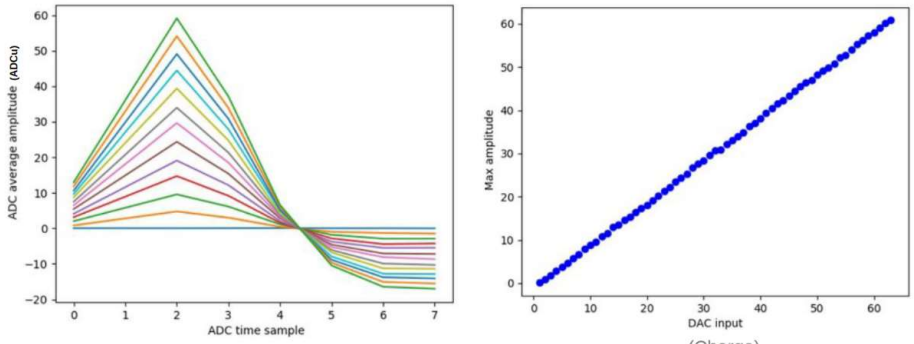
## TDC Jitter




- At 23 fC, σ ~ 10 ps

## ADC studies: Charge Scan for Pix1

Amplitudes as a function of time with pedestal subtraction (w.r.t. lower charge).

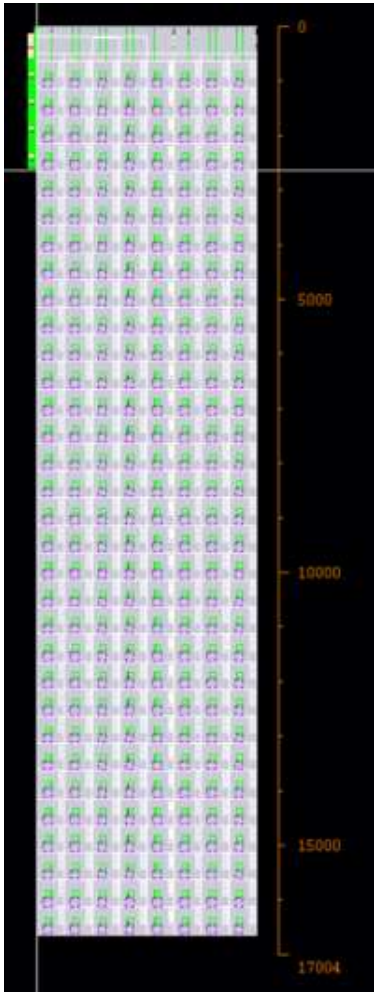


# Next steps : EICROC1 8x32 or 32x32

- EICROC1 : 8x32 = 256 pixels or 32x32 = 1024
  - Layout complete. DRC/LVS OK
  - Still EICROC0 digital architecture and Readout
  - 2/8 data outputs : 1 for 128 pixels (4x32)
  - Looking to increase R/O speed. Possibility to skip pixels by SC
  - Looking to improve testability.
  - Verifications in progress (~2 months)
  - 32x32 would allow tests with final sensor

- EICROC1 addresses floorplan issues
  - Power drops along column, threshold uniformity
  - TDC uniformity and dependance on number of channels triggering

- Variants of EICROC0 will also be submitted
  - Lower power in the ADC branch (100 µW)

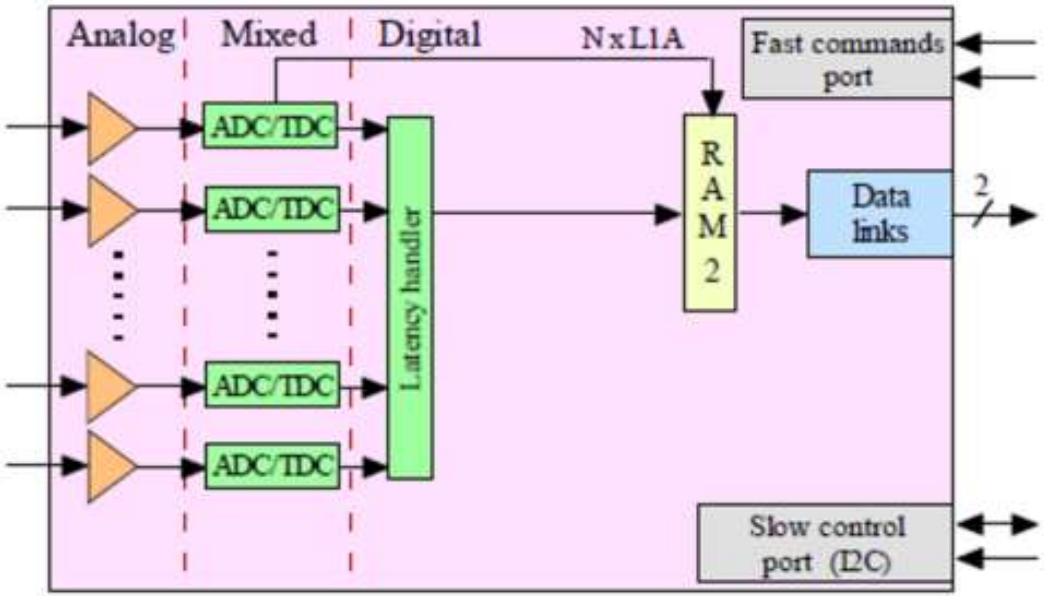


# EICROC2 : 32x32 with EIC backend

- EICROC2 needs to address EIC digital architecture
  - Auto-trigger
  - Data driven zero-suppressed readout
  - Only readout hit channels and neighbours
  - Will depend a lot on the (low?) occupancy
  - Triplication and SEE tolerance

- Several EIC functions will be tested in CALOROC
  - Sparsified readout
  - Output links 160-1280 Mb/s

- Foreseen submission mid-2026



# Comparison EICROC / HGCROC

## EICROC

- « 2D chip »  16 -> 1024 channels
- Input capacitance : Cd = 1-5 pF
- Dynamic range : 1 fC – 50 fC
- ToA and ADC
- Target power : 1 mW/ch
- Area 10 mm² (300 mm² final)

- Target DoT

## H2GCROC/CALOROC

- « 1D chip » 36/72 channels
- Input capacitance : Cd = 100-1000 pF
- Dynamic range : 30 fC – 300 pC
- ToA and ToT
- Target power : 5-10 mW/ch (now 15)
- Area 100 mm²

- AoT

# Possible issues/questions with SRO

- Bandwidth saturation with spurious noise events
  - Throttling
  - Flag buffer almost full
- Buffer depth
  - Need a good estimation of occupancy and background
- Auto-trigger stability
  - Minimize threshold drift
- Pedestal estimation
  - External trigger

# Conclusion

- CALOROC is a 36-72 channel chip to readout SiPMs for calorimetry
  - will make full use of SRO

- EICROC is a 1k-channels ASIC to readout AC-LGAD pixels
  - Very promising new family of detectors
  - Combines both good timing and position resolution (30 ps 10 µm)
  - Targeting ~1 mW/ch
  - Reuses many blocks from ATLAS HGTD and CMS HGCAL

- SRO an important feature of these next chips
  - Also paves the way for future low power calorimeter readout (DRD6)

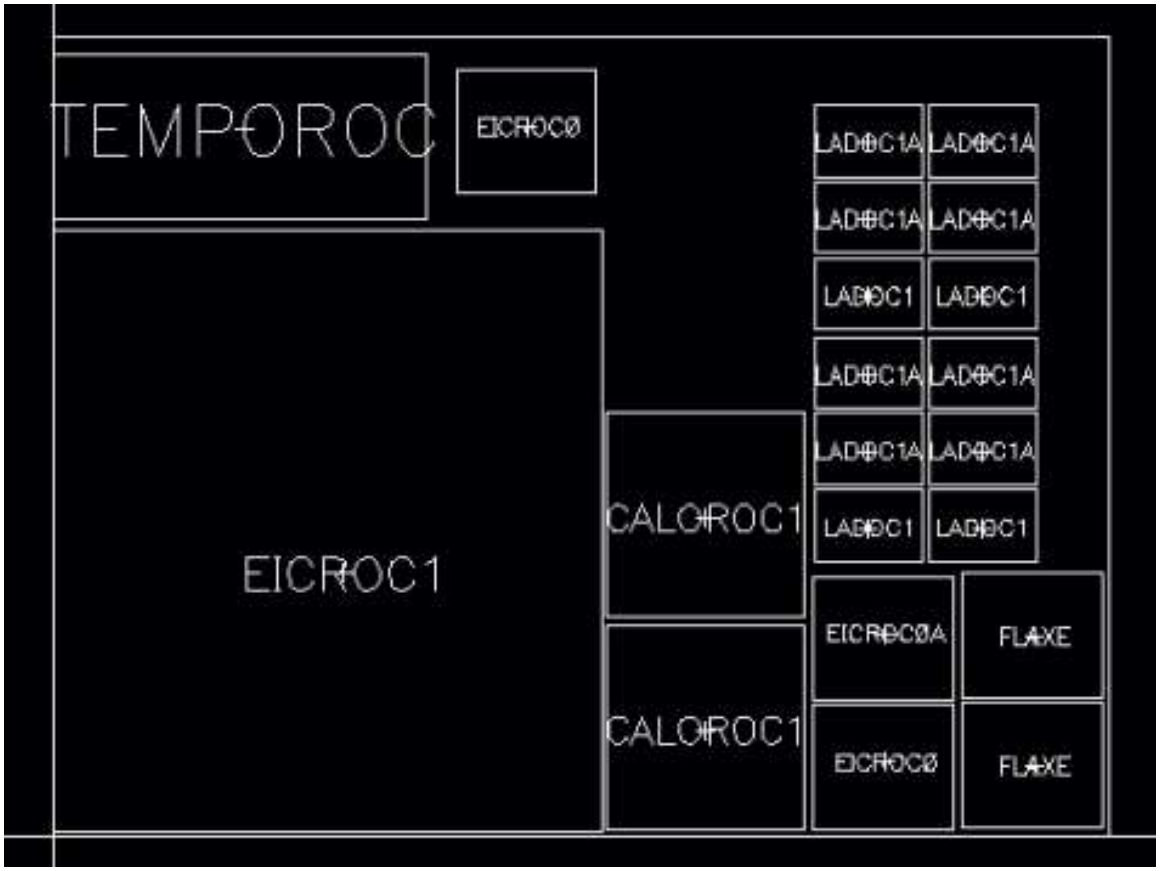
# backup

# EIC reticle 2024

- TSMC now requires to fully populate the reticle of 24x32
  - Cost ~300 k€

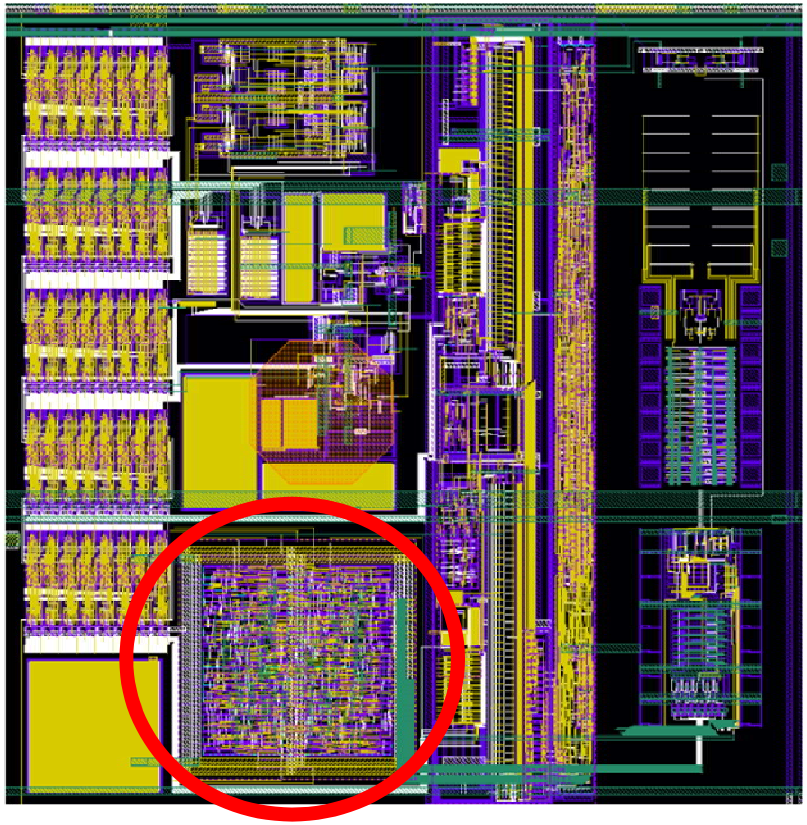
- For EIC we would have
  - EICROC1
  - 2 or 3 EICROC0/A/B
  - 2 CALOROC1A/1B
  - ~60% of reticle area

- Possible additionnal partners
  - ~20% of reticle area
  - Still space available (if ready in time !)



# Technology choice 65/130n

- Little impact on analog/digital performance
  - Analog similar in 65/130
  - Possibly more significant on TDC
  - Digital much simpler than LHC chips
- Update of digital part
  - Little space available => main reason for 65 !
- sizeable cost impact : ER 700 k$ vs 300 k$
  - But possibly more partners (but EICROC 50% of reticle)
- Prepare for design in 65 nm
  - Make an EICROC0/65n to test analog part and TDC



# AoT vs DoT

- HGCROC/CALOROC designed Analog on Top (1D chip)
  - Analog inputs on one side / digital output on the other side
  - All digital data resynchronized when transefered to digital block

- ALTIROC designed Digital on Top (2D chip)
  - Powerful tools to verify digital part functionnality/timings in all corners on all the chip area
  - But needs more manpower for digital design (RTL, P&R, IRD, TB, UVM…)
  - Possible help from colleagues at Clermont

- Choice will depend on complexity (occupancy) and manpower availability

# Chips versions

| Chip | date | Techno | size | Analog | Digital | goal |
|---|---|---|---|---|---|---|
| EICROC0 | Jun 2023 | 130n | 4x4 | Conservative | Simple | Study sensor |
| EICROC0A/B | Dec 2024 | 130n | 4x4 | Low power | same | Study analog |
| EICROC1 | Dec 2024 | 130n | 32x32 | Conservative | Same | Study power distribution |
| EICROC0_65n | end 2025 | 65n | 4x4 | final | Simple | Study analog in 65n |
| EICROC2 | End 2026 | ? | 32x32 | Low power | Final | First final prototype |

| Chip | date | Techno | size | Analog | Digital | goal |
|---|---|---|---|---|---|---|
| CALOROC1A | Dec 2024 | 130n | 36ch | Conservative | Final | Study sensor |
| CALOROC1B | Dec 2024 | 130n | 36ch | Low noise | final | Study analog |
| CALOROC2 | End 2026 | 130n | 36/72 | final | final | First final prototype |

# CATIROC for JUNO

**A complex System on Chip (SoC).** Technology: 0.35 µm SiGe AMS

| CATIROC general features | Application to JUNO |
|---|---|
| **16 independent channels** | **Reduce the number of electronic** board (only 200 boards for 25,000 SPMTs) |
| Analog F.E. with **16 trigger outputs** + **charge and time digitization** | **Photon counting** + **charge and time measurements**. Resolutions very good |
| **Autotrigger mode:** all the PMTs signals above the threshold (1/3 p.e.) generate a trigger and are converted in digital data | Simplify online-DAQ |
| **100% trigger efficiency @ 1/3 p.e.** | **Good 1 p.e. detection** photon counting mode |
| **Dual gain front-end**: HG and LG channel Charge dynamic range 0 to 400p.e. (at PMT gain $10^6$) | Only **HG** actually used (only few p.e. expected) |
| **Time stamping** ( resolution ~ 170 ps rms) | **< 1ns required** |
| Each channel has a **variable gain** | **To compensate gain vs HV spread** for the 16 PMTs |
| **One** output for **DATA** | **Less number of cables to the surface** |
| Hit rate 100 kHz/ch (all channels hit) **50 bits of data / hit channel** | **Very "light" data output** (compared to a FADC waveform) |

# Summary of the HKROC0 performances

| Item measured | Performances |
|---|---|
| Trigger efficiency at 1/6 p.e. | $> 90\%$ for 1/5 p.e signals<br>100% for $\geq 1/4$ p.e signals |
| Trigger noise at 1/6 p.e. | $< 1$ Hz (No trigger observed in 10 s) |
| TDC resolution | 150 ps at 1 p.e, 70 ps at 5 p.e, 25 ps $> 10$ p.e<br>Validated with PMT |
| Charge linearity | $< 0.5\%$ in high & medium gain channels<br>$< 1\%$ in low gain channel up to 1250 p.e<br>Validated with PMT |
| Charge resolution | $< 0.1$ p.e for signals up to 10 p.e<br>$< 1\%$ beyond 10 p.e signal<br>Validated with PMT |
| Dead-time<br>& pile-up | $\leq 30$ ns for two signals of same amplitude<br>$\leq 30$ ns for a prompt $\leq 5$ p.e and secondary of 1 p.e<br>$< 1$ $\mu$s for a prompt signal $\leq 850$ p.e and secondary 1 p.e |
| Maximal<br>hit-rate<br>w/ 100% eff. | 415 kHz in normal mode<br>950 kHz in SN-mode<br>Potential extension beyond to be studied. |
| Cross-talk | Hit probability in neighbouring channel<br>of a 1250 p.e signal is $< 0.1\%$<br>*Note that cross-talk found at ASIC level, but cut by FPGA. Identified and will be removed in ASIC v2.* |
| Maximal<br>hit-rate<br>w/ 100% eff. | 415 kHz in normal mode<br>950 kHz in SN-mode<br>Can be extended even beyond for v2. |
| Temperature<br>dependency | mean time $\Delta T = 17.5$ ps/°C<br>rms time $\Delta T \leq 1$ ps/°C<br>mean charge $\Delta Q = 0.1\%$/°C (no correction)<br>charge variation has no dependency |
| Power consumption (W) | $\leq 6.6$ W for 24 PMTs |
| Resistance to HV | Received 1,000 2000 V discharge from PMT-base<br>Unprotected ASIC received $7 \times 10^{10}$ 7V injections<br>($> 500$ yrs of HK) without any impact on performances<br>Validated protection circuit itself saturates<br>signals $> 7$ V to 7 V. |
| Failure rate / year | ASIC failure $\leq 0.03\%$ |

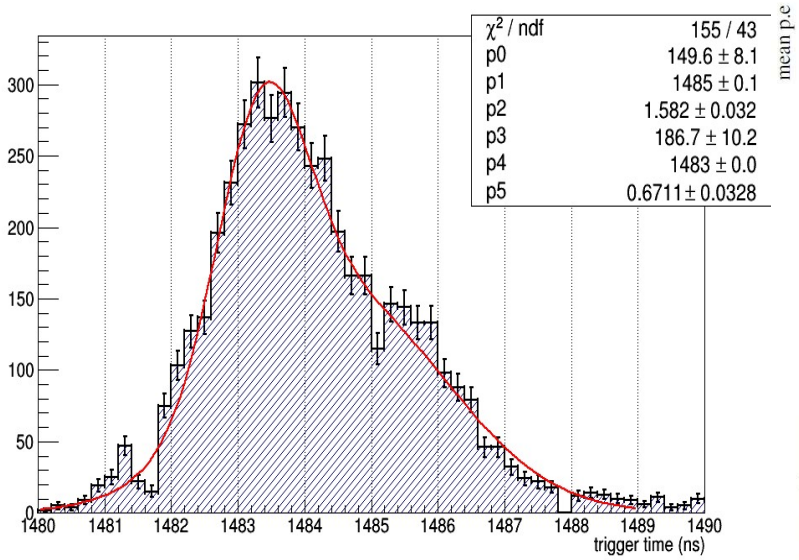
# PMT measurements

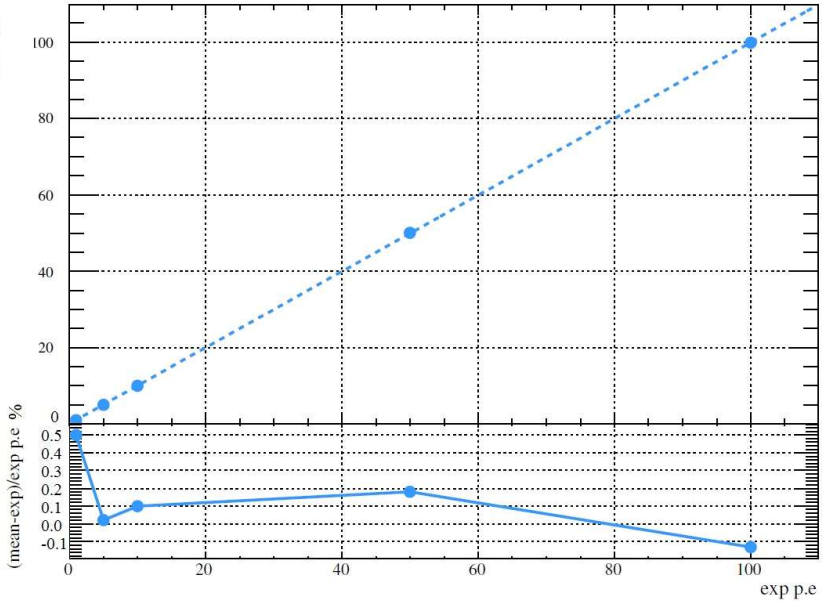
**Trigger time distribution** for events having charge ≤ 1.5 p.e : FWHM of **2.6 ns**

- **Excellent agreement with the 2.8 ns found for the PMT only**
- Digitizer does not degrade the PMT time resolution !

The charge **linearity** is **≤ ±1%**

**Exact same behavior than with the function generator.**



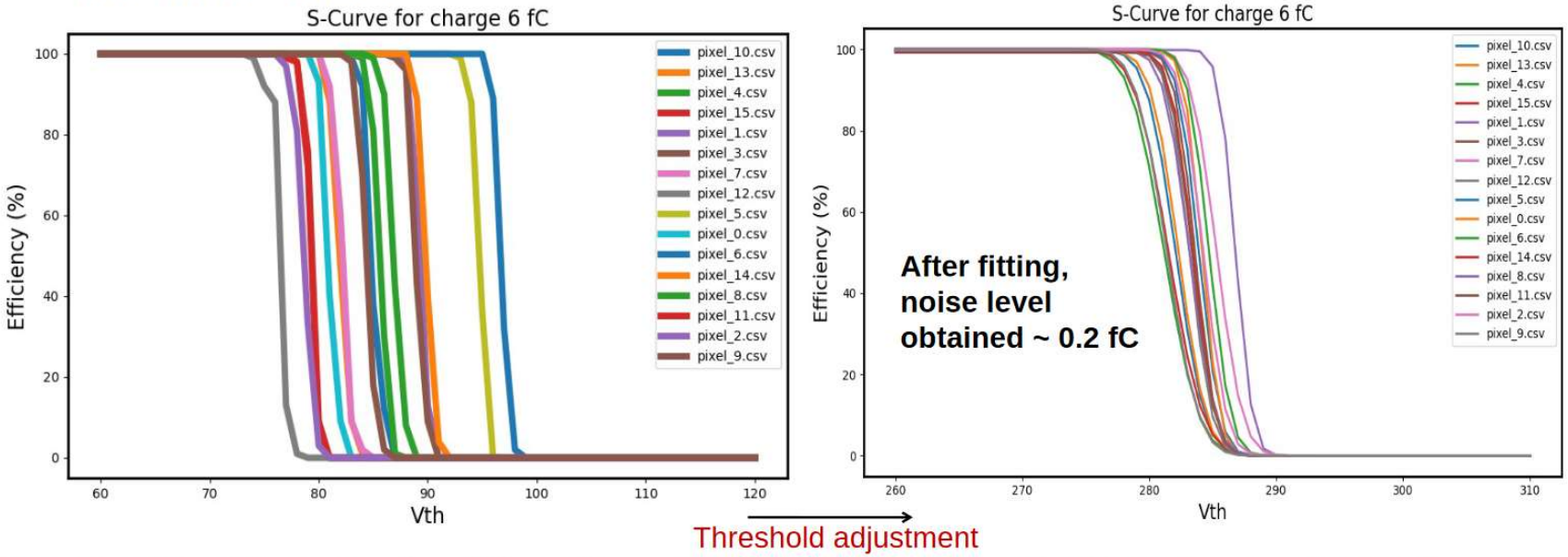



# Minimum threshold

*From A. Sharma :https://indico.in2p3.fr/event/33456/contributions/144321*

## S-curve (Efficiency vs threshold voltage)

- To correct the response of all channels towards the injected charge, discriminator threshold adjustment is done at a specific charge injection to align all channels.




Measurements performed to align all the pulses, and then obtain a minimum threshold to detect a minimum charge: for neighboring charge selection.

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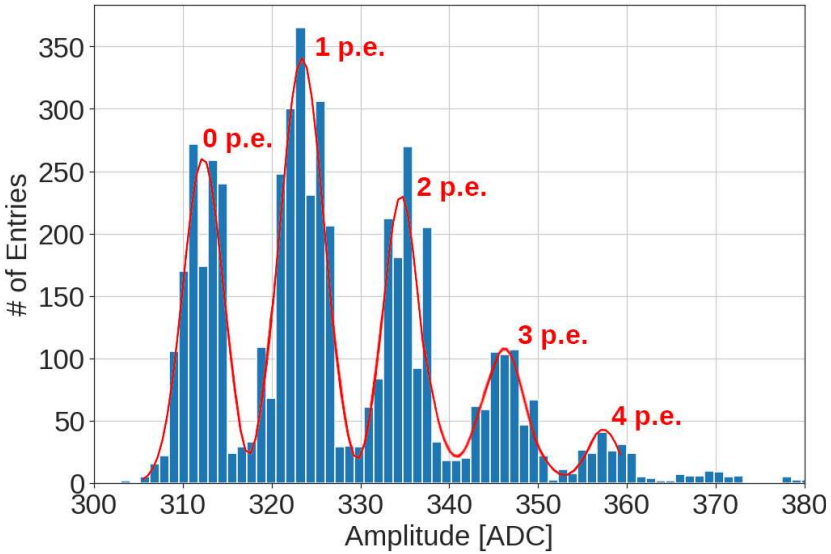
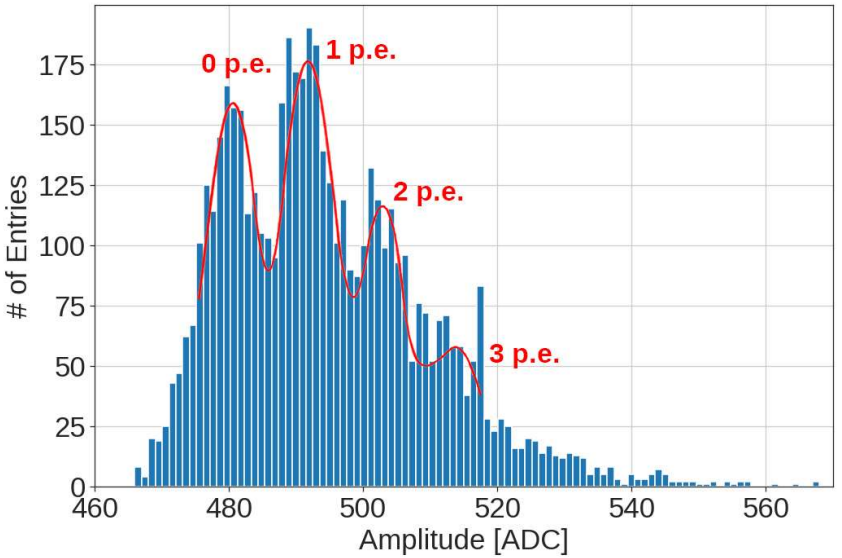
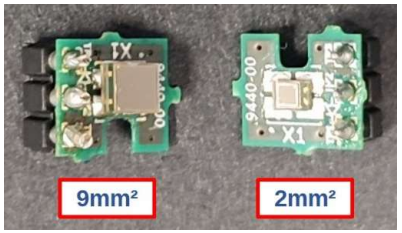
# Calibration mode: Single-photon-spectrum

- **2mm²:**




- **9mm²:**




***Extra step for 9mm² SiPM calibration:**

The large $C_{det}$ of the 9mm² SiPM produce an increment of DNL and make it harder to see the photon separation.

The DNL can be mitigated taking data with different pedestal levels using the ASIC to move the pedestals (*Trim_inv* parameter). SPS is clearer after aligning the data.

**Without DNL correction:**