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U.S. DEPARTMENT OF ENERGY

FELIX Hardware Development for Streaming Readout

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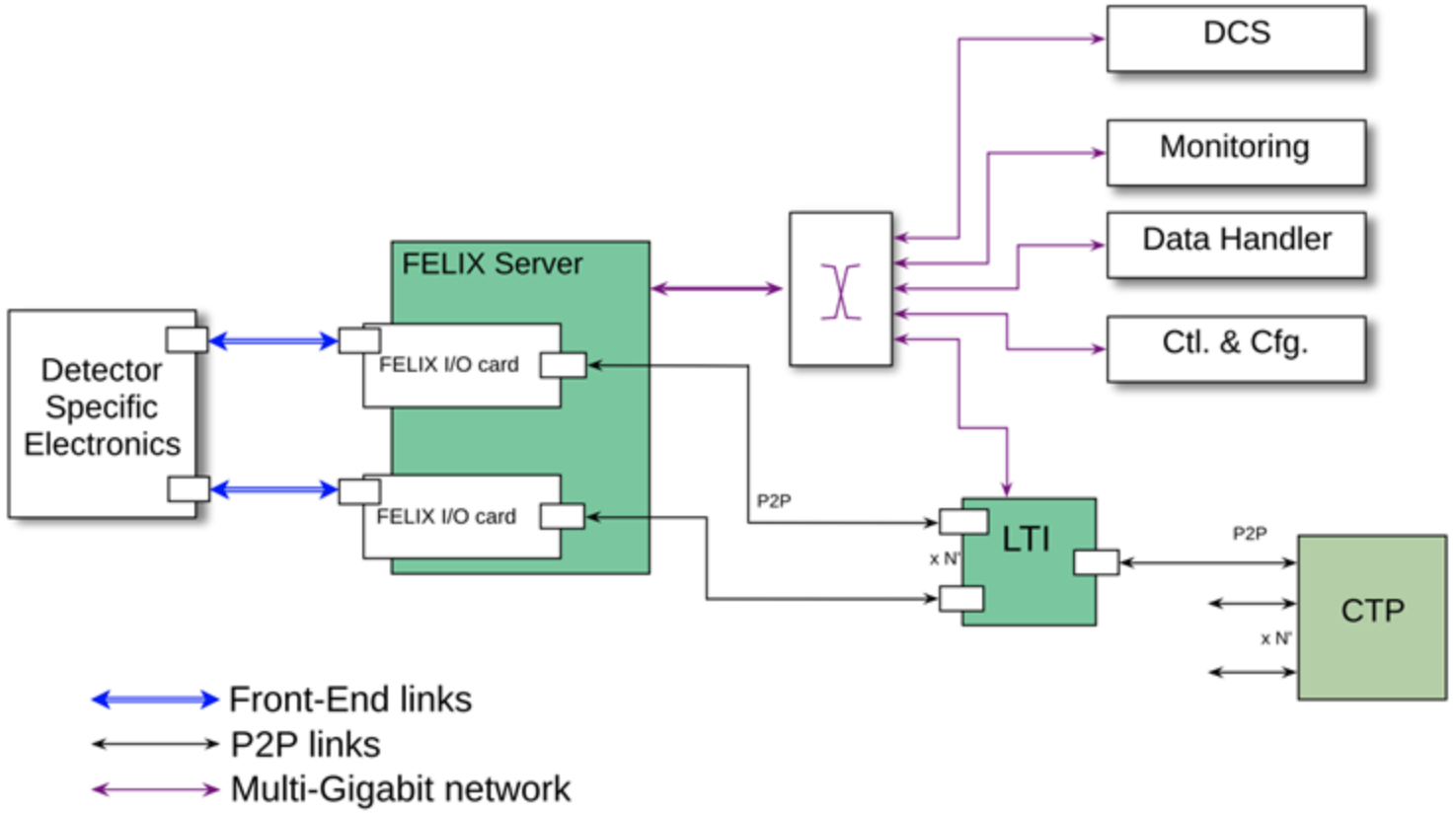
BNL

@BrookhavenLab

Streaming Readout Workshop SRO-XII, Dec 2 – 4, 2024
University of Tokyo

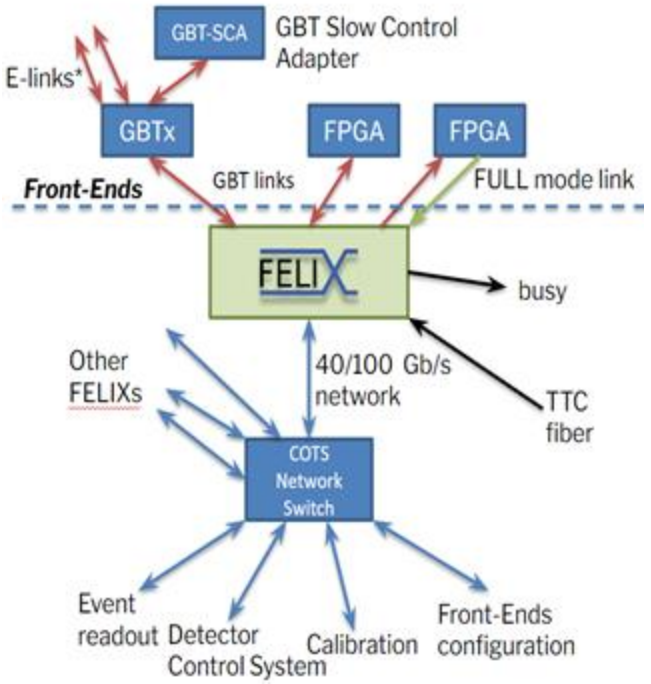
FELIX – Front End LInk eXchange



Block diagram of readout system with FELIX

FELIX

- A generic detector readout concept, proposed by ATLAS Collaboration a decade ago, between front-end serial links and a commodity network
- Open-source firmware and software
  - Collaboration of different institutes
  - ANL, BNL, Bologna, CERN, IFIN-HH Bucharest, Nikhef, RU, RHUL, UC Irvine, Weizmann and Wuppertal
- Applications in HEP and NP experiments
  - ATLAS Phase-I Upgrade, ProtoDUNE-I and NA62
  - NSLS-II & ANL Light Source, sPHENIX at RHIC, SoLID at JLab, and FAIR CBM at GSI, Fermilab Test Beam
  - Future applications: ATLAS Phase-II Upgrade, EPIC@EIC, R&D of nEXO/DarkSide, ALICE and LHCb@HL-LHC



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CERN
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Radboud University
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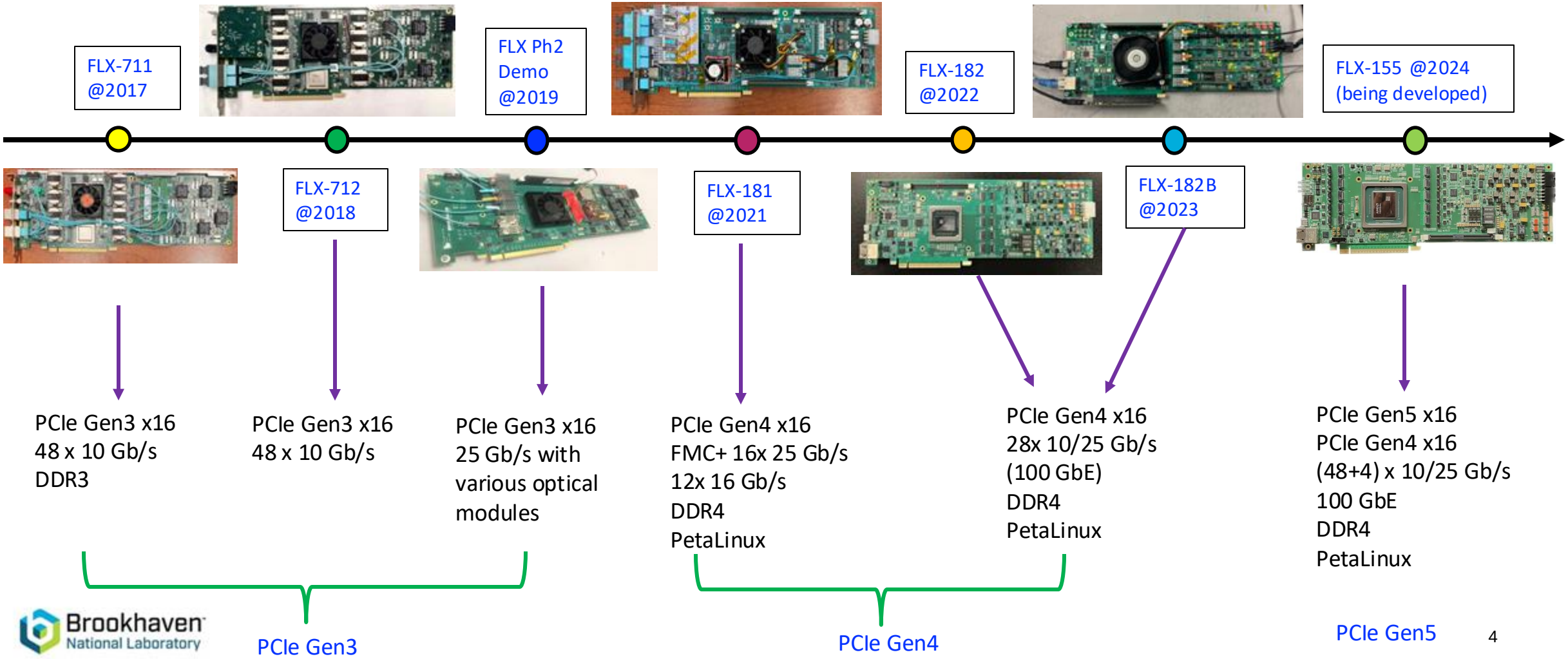
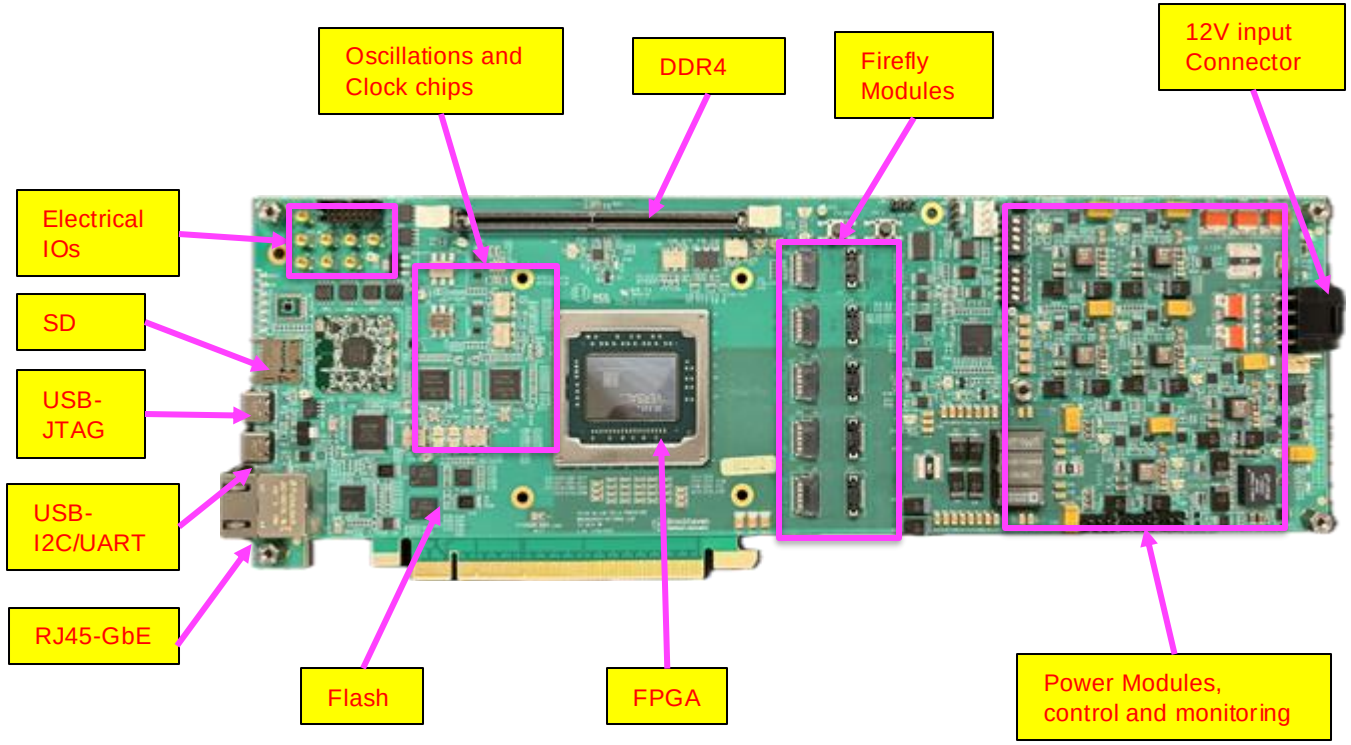
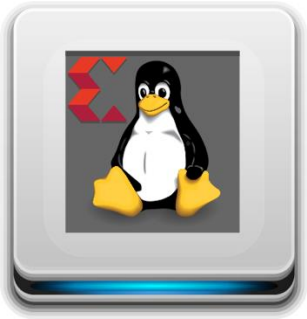
FELIX Hardware Development @BNL



FLX-182

- AMD Versal Prime FPGA XCVM1802
- PCIe Gen4 x16/2x8
- 24 FireFly links with 3 possible configurations
  - 24 links up to 25 Gb/s
  - 24 links up to 10 Gb/s (CERN-B FireFly)
  - 12 links up to 25 Gb/s + 12 links up to 10 Gb/s
- 4 FireFly links with 2 possible configurations with 14 or 25 Gb/s FireFly TRx
  - LTI interface
  - 100 GbE
- 1 DDR4 Mini-UDIMM
- USB-JTAG/USB-UART
- Boot: SD3.0/QSPI
- GbE
- White Rabbit
- PetaLinux





Picture of assembled FLX-182

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Status of FLX-182

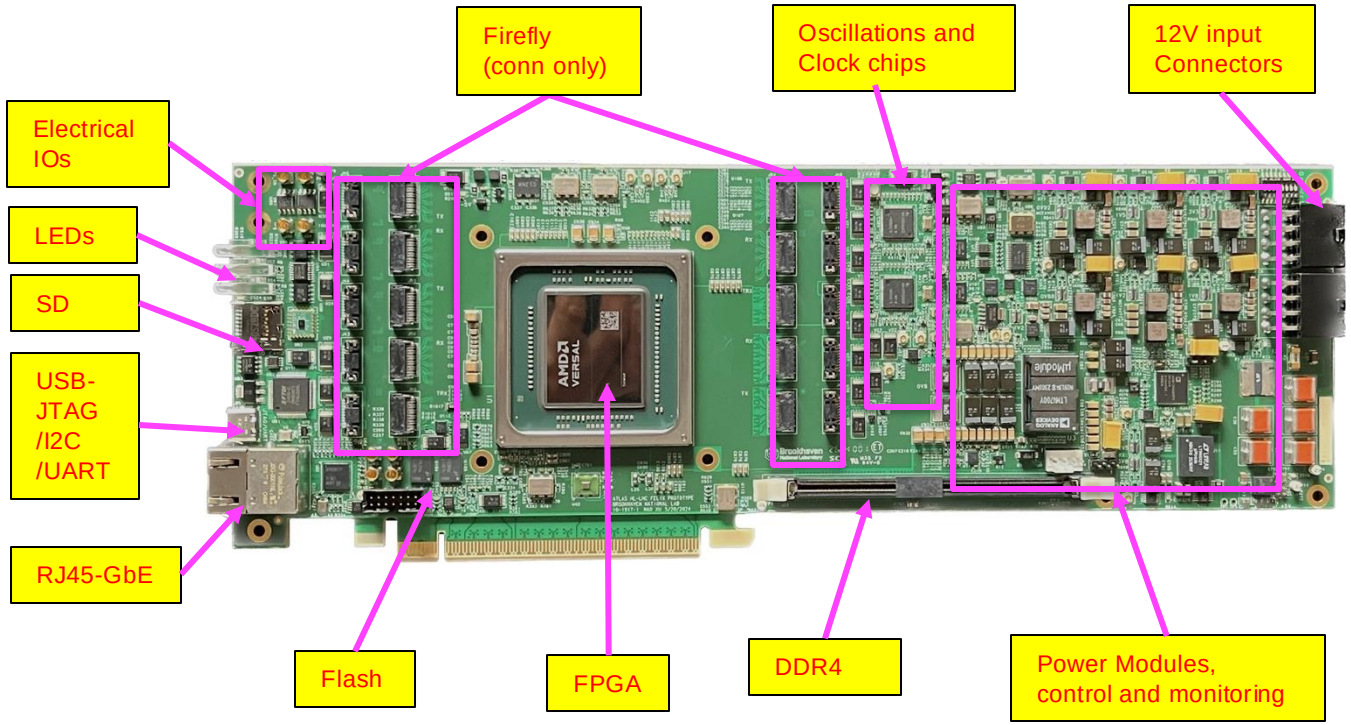
- Hardware functionalities are fully validated
  - Total 28 (24+ 4) links @ 25 Gb/s are available for data transmission
  - PCIe Gen4 performance
    - 2x Gen4x8 endpoints, theoretical payload bandwidth 120.47Gb/s for each endpoint
    - 2 x8 endpoints: 2x 113.2 Gb/s, 94% of theoretical bandwidth
    - 1 x8 endpoint: 1x 118 Gb/s, 97.9% of theoretical bandwidth
- Different flavors of FELIX firmware have been implemented, and functionality demonstrated
- 50+ FLX-182 cards have been produced for different HEP and NP experiments
  - ATLAS Phase-II Upgrade, ALICE at CERN, and CERN DRD7 hardware platform
  - ePIC at EIC
  - sPHENIX at RHIC
  - CBM/RE21 at FAIR

Picture of FLX-182 cards

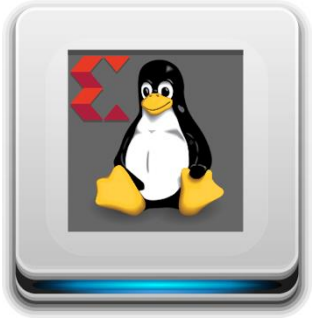
FLX-155

Main features of FLX-155

- AMD/Xilinx Versal Premium FPGA: XCVP1552-2MSEVSVA3340
- PCIe Gen4 x16 / PCIe Gen5 2x8
- 56 FireFly optical links
  - Compatible with various options
  - Default configuration for ATLAS
    - 48 data links up to 25 Gb/s
    - 4 links for LTI
  - 4 links for 100GbE
- Electrical IOs
- 1 DDR4 Mini-UDIMM
- USB-JTAG/USB-UART
- SD3.0/QSPI
- GbE
- White Rabbit

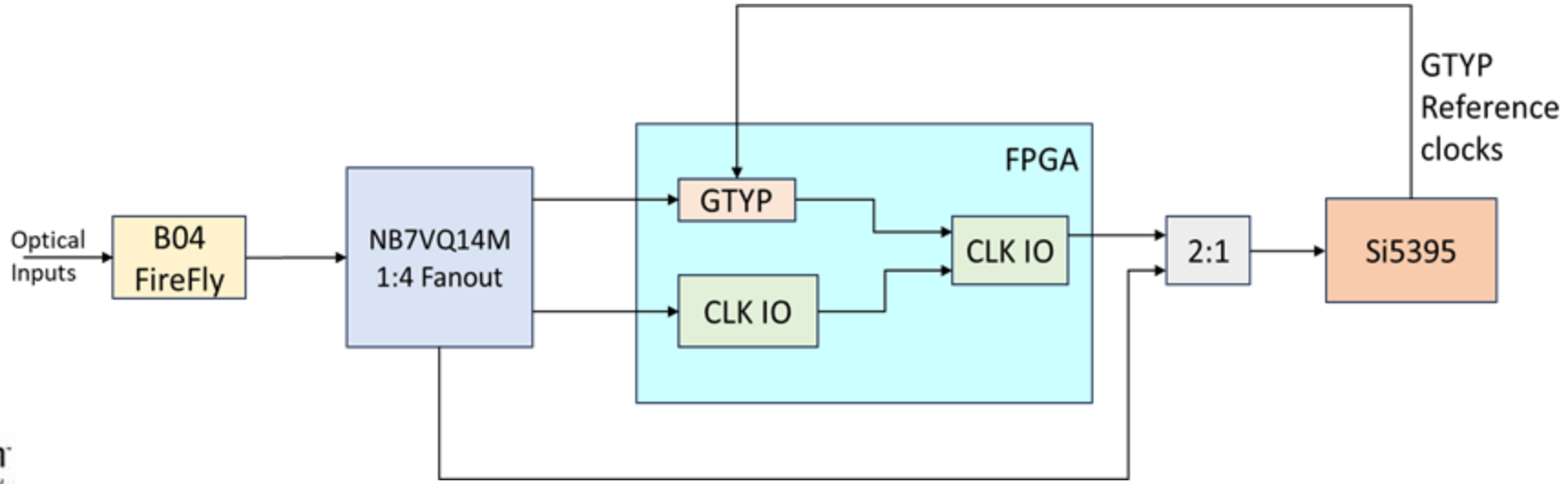


Picture of assembled FLX-155



TTC Clock Scheme

- Either recovered clock from TTC link, or clock from optical directly
- Recovered clock from TTC link
  - Connected to GTYP to get recovered clock as system clock
  - 4 TTC links on one B04
- Optional optical clock
  - To use the optical clock as system clock directly
  - One RX of B04 is connected to FPGA clock input. In this case, only 3 RX links left are connected to GTYP



Status of FLX-155

- One FLX-155 has been produced and being tested at lab
  - All functions work properly except minor issue with DDR4 memory
  - All GTYP optical links have been verified with 25Gb/s
  - PCIe Gen5 2 x8 performance have been evaluated
    - PCIe Gen5 2 x8 endpoints, theoretical payload bandwidth 256Gb/s for each endpoint
    - The throughput is 29.567 GB/s = 236.5 Gb/s, 92.4% theoretical maximum speed
    - Taking head in the test data into account, it is 98% of theoretical maximum speed

```
Consume FLX-device data while checking the data (blockheader and trailers)
Also counts chunk CRC errors.
Opened FLX-device 0, firmw FLX120-GBT-2x24CH-240306-1750-GIT:rm-5.1/191, trailer=32bit, buffer=1024MB, DMA=0
Opened FLX-device 1, firmw FLX120-GBT-2x24CH-240306-1750-GIT:rm-5.1/191, trailer=32bit, buffer=1024MB, DMA=0
**START**
** using DMA #0 polling
  Secs | d-D |  Recvd[MB/s] | File[MB/s] | Total[(M)B] | Rec[(M)B] | Buf[%] | Wraps
-------|-----|--------------|------------|-------------|-----------|--------|-------
     1   0-0        31631.6          0.0        31631.6           0       50      29
   ### @Dev-DMA=0-0 Blocks 30408704 Errors: header=30639640 trailer=0 (trunc=0 err=0 length=0 type=0 crc=0)
     1   1-0        29574.0          0.0        29574.0           0       35      27
   ### @Dev-DMA=1-0 Blocks 28547055 Errors: header=28547055 trailer=0 (trunc=0 err=0 length=0 type=0 crc=0)
     2   0-0        29567.8          0.0        61199.3           0       34      56
   ### @Dev-DMA=0-0 Blocks 59460477 Errors: header=59460477 trailer=0 (trunc=0 err=0 length=0 type=0 crc=0)
     2   1-0        29567.8          0.0        59141.8           0       24      55
   ### @Dev-DMA=1-0 Blocks 57543329 Errors: header=57543329 trailer=0 (trunc=0 err=0 length=0 type=0 crc=0)
     3   0-0        29567.6          0.0        90766.9           0       20      84
   ### @Dev-DMA=0-0 Blocks 88487291 Errors: header=88487291 trailer=0 (trunc=0 err=0 length=0 type=0 crc=0)
     3   1-0        29567.5          0.0        88709.2           0       66      82
   ### @Dev-DMA=1-0 Blocks 86983232 Errors: header=86382970 trailer=0 (trunc=0 err=0 length=0 type=0 crc=0)
```

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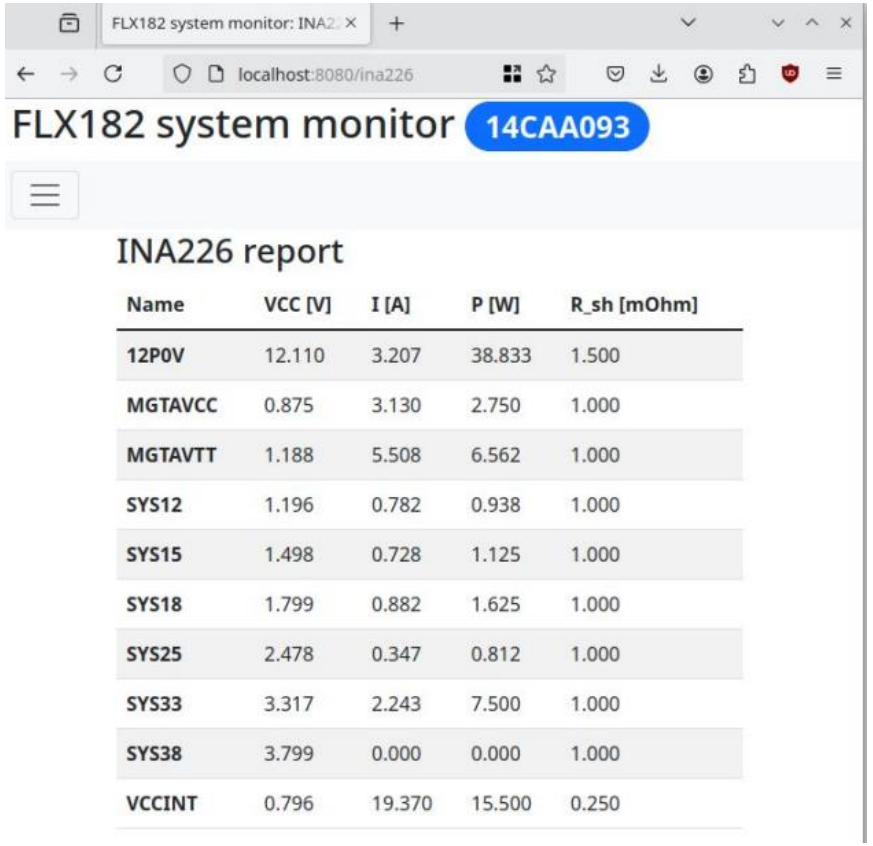
PetaLinux

- Arm cores in Versal Prime/Premium FPGA
  - Dual-core Arm Cortex-A72 Application Processor
    - Up to 1.7 GHz for 2X single-threaded performance
  - Dual-core Arm Cortex-R5 Real Processor
    - Up to 750 MHz for 1.4X greater performance
- The PetaLinux Tools offers everything necessary to customize, build and deploy Embedded Linux solutions on AMD processing systems
- PetaLinux can run successfully on Versal FPGA
  - Boot loader
  - CPU-optimized kernel
  - Linux applications & libraries
  - C & C++ application development
  - Integrated web server for easy remote management of network and firmware configurations

Petalinux 2024.1

System Monitoring and Self-test

- BIST: A Built-In Self-Test package with firmware and software for FELIX card has been developed by BNL
- ARM Cortex-A72 CPU on Versal boots Linux from SD card
  - Device drivers are already available for most peripherals
  - May use standard utilities for tests, firmware updates, remote management and more
- Web application
  - Sensor monitoring and peripheral configuration in an easy, convenient way
  - Rapid development with Python
  - Flexible configuration to support any board (requires a CPU, DRAM and storage)
- Status of key components through I2C bus
  - FireFly
  - DDR4
  - Power supply
  - Voltage and current: INA226
  - Temperature: TMP435

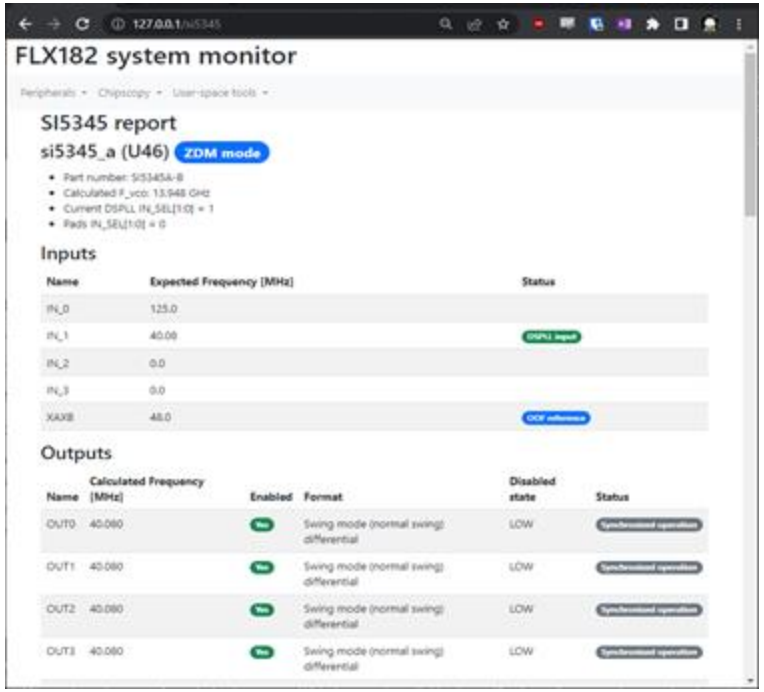


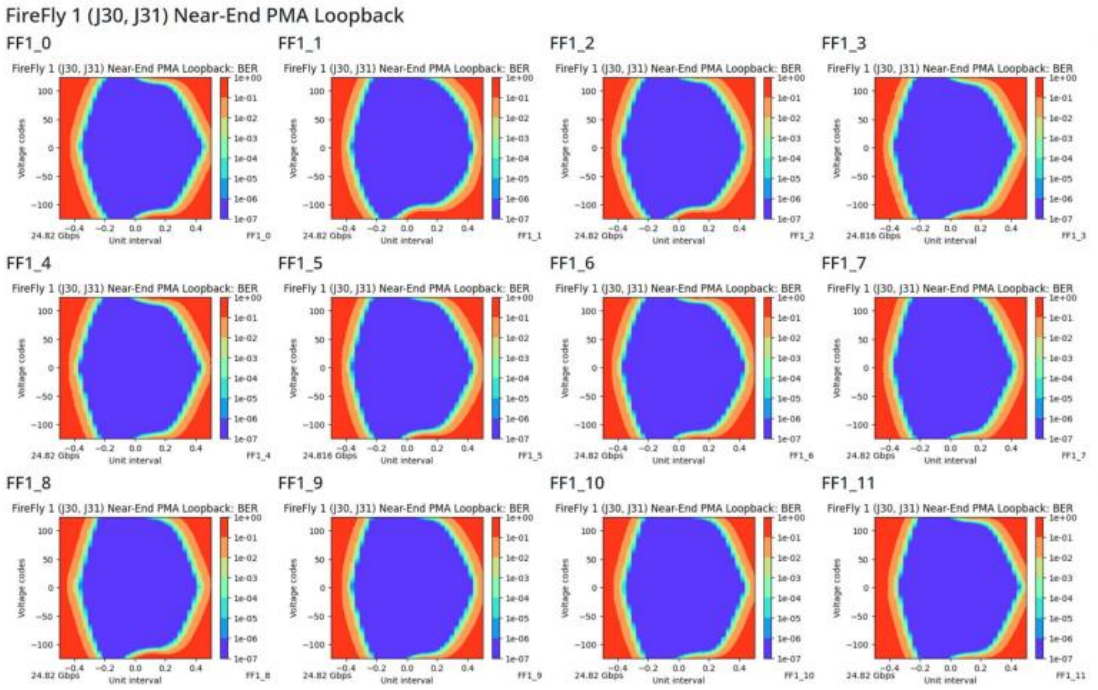
Name	VCC [V]	I [A]	P [W]	R_sh [mOhm]
12P0V	12.110	3.207	38.833	1.500
MGTAVCC	0.875	3.130	2.750	1.000
MGTAVTT	1.188	5.508	6.562	1.000
SYS12	1.196	0.782	0.938	1.000
SYS15	1.498	0.728	1.125	1.000
SYS18	1.799	0.882	1.625	1.000
SYS25	2.478	0.347	0.812	1.000
SYS33	3.317	2.243	7.500	1.000
SYS38	3.799	0.000	0.000	1.000
VCCINT	0.796	19.370	15.500	0.250

Web-based BIST for FLX-182

BIST for Production Test

- Finish production test and generate test report automatically
- Upload test results to DB once test is done





Development Plan

- FLX-155 revision is being planned
- The revision design will be finished in about 6 months, and the test will be done in 2 months once it’s delivered
- New FLX-155 cards are expected to be available for users in 2025 fall

Summary

- The FELIX is a generic platform for streaming readout, which has been and is going to be tested by several experiments - ATLAS at CERN, ePIC at EIC, sPHENIX at RHIC, LHCb at CERN, ALICE at CERN, CBM/RE21 at FAIR
- FLX-182 and FLX-155 have been developed for FELIX phase-II hardware platform. FLX-155 revision will be available for user in 2025 fall

Thanks for your attention!