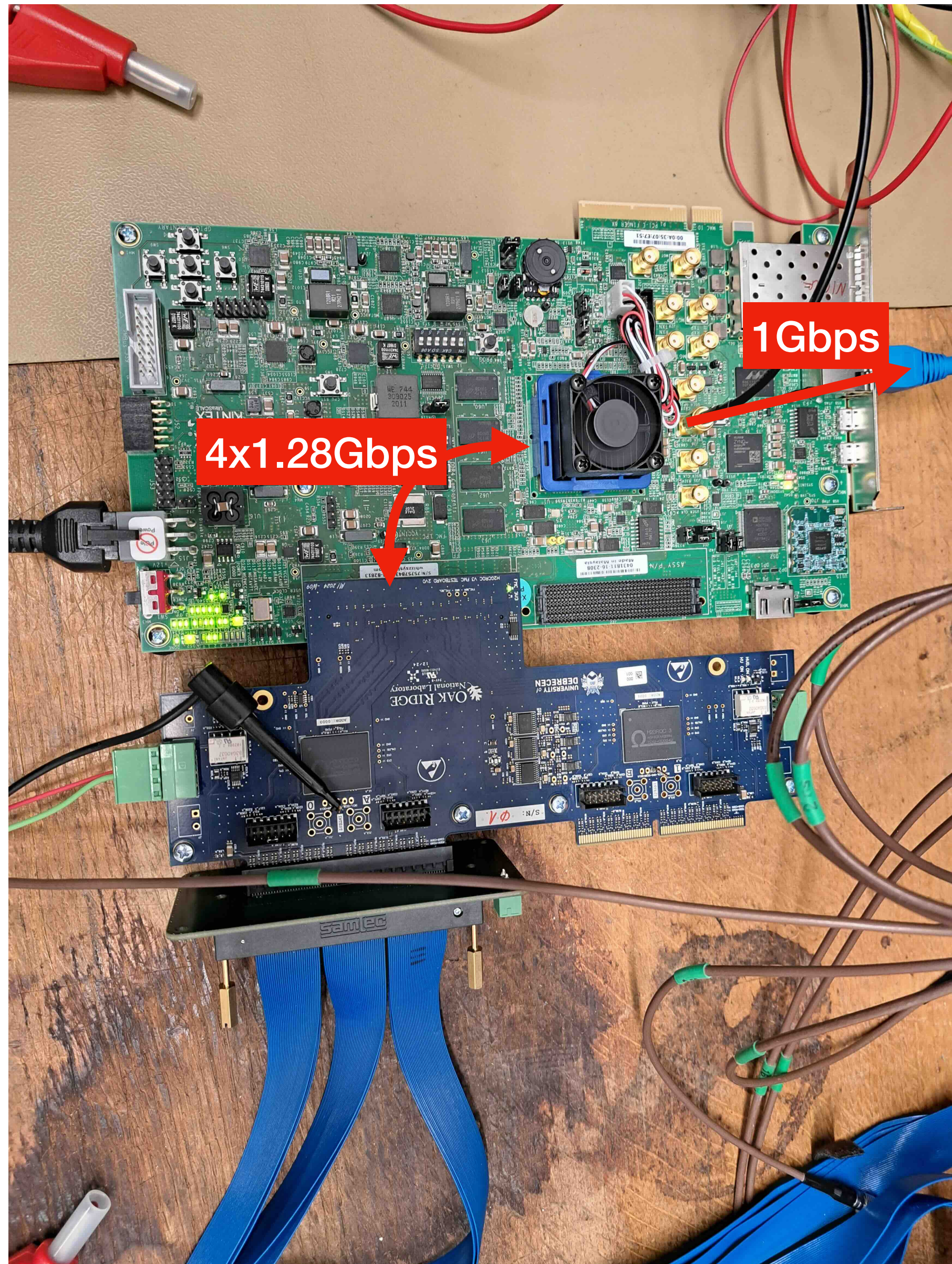


# eRD109 update - H2GCROC

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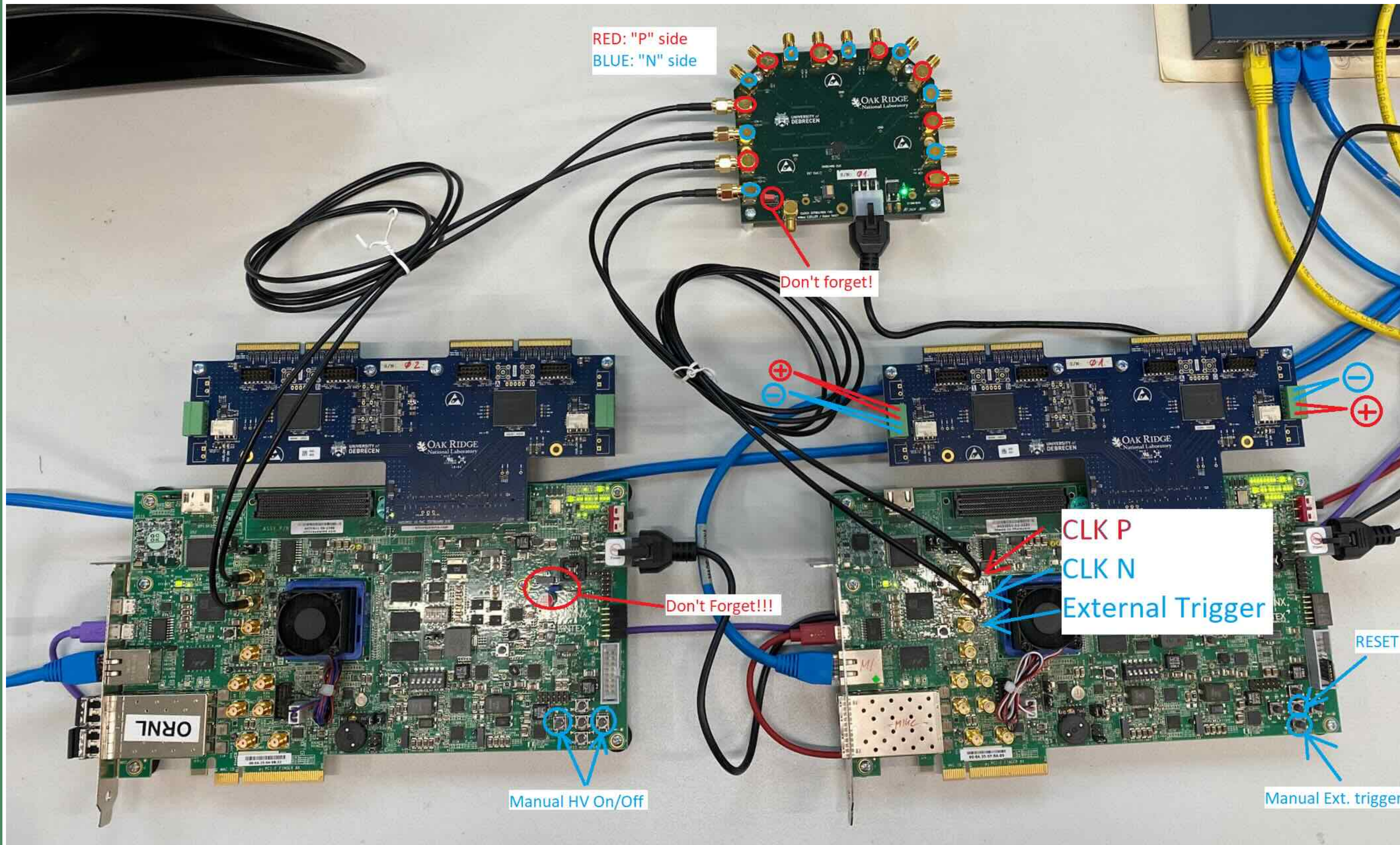
# Hardware and Firmware are ready



## Communication with the H2GCROC3:

- FPGA and H2GCROC3s:
  - DownStream:
    - 2xI2C lines for setup
    - 2xFCMD lines
    - 2x320MHz clock
  - UpStream:
    - 2x2x1.28Gbps data lines
      - 1 sample takes 80x32 bit word + idle
      - About 1.025  $\mu$ s readout
    - 2x4x1.28Gbps trigger lines (option to not include in more upstream)
- KCU105 and PC:
  - 1 Gbps UDP readout
  - Creating a bottle neck
    - Factor of 5 less speed

# External Clock - to synchronize the data



**Simple external clock is board is used for synchronization:**

- The oscillator provides 40 MHz LVDS clock via the SMA connector in KCU105
- Cable length is the same 1 meter - sufficient for our tests
- External trigger is coming in 1.8V input

# Data format

H2GCROC data

```
a0 00 24 00 05 05 28 51 50 ac 06 85 00 00 44 00 04 a0 00 00 07 a0 00 00 06 f0 00 00 06 f0 00 00 06 50 00 00 09 40 00 00
a0 00 24 01 05 05 28 51 07 60 00 00 05 f0 00 00 09 70 00 00 05 50 00 00 05 f0 00 00 05 d0 00 00 06 f0 00 00 07 50 00 00
a0 00 24 02 05 05 28 51 05 f0 00 00 05 f0 00 00 05 00 00 00 06 90 00 00 08 40 00 00 06 60 00 00 09 00 00 00 07 90 00 00
a0 00 24 03 05 05 28 51 09 00 00 00 08 20 00 00 06 f0 00 00 07 50 00 00 0a 00 00 00 08 20 00 00 08 40 00 00 07 f0 00 00
a0 00 24 04 05 05 28 51 07 70 00 00 05 b0 00 00 04 d0 00 00 08 10 00 00 07 70 00 00 04 80 00 00 06 f0 00 00 cf 98 73 60
a1 00 25 00 05 05 28 51 52 a7 05 85 00 00 00 00 05 a0 00 00 04 80 00 00 06 40 00 00 04 40 00 00 05 f0 00 00 06 f0 00 00
a1 00 25 01 05 05 28 51 05 50 00 00 05 00 00 00 05 70 00 00 05 a0 00 00 05 70 00 00 06 f0 00 00 05 b0 00 00 06 f0 00 00
a1 00 25 02 05 05 28 51 05 50 00 00 06 d0 00 00 06 d0 00 00 07 70 00 00 06 50 00 00 06 f0 00 00 06 d0 00 00 06 50 00 00
a1 00 25 03 05 05 28 51 05 a0 00 00 06 b0 00 00 08 00 00 00 05 70 00 00 05 00 00 00 06 80 00 00 06 80 00 00 05 e0 00 00
a1 00 25 04 05 05 28 51 00 30 00 00 06 80 00 00 03 90 00 00 05 f0 00 00 04 a0 00 00 06 b0 00 00 05 70 00 00 d5 a9 78 e8
a0 00 25 00 05 05 28 51 50 ac 06 85 00 00 00 00 05 a0 00 00 02 20 00 00 02 00 00 00 02 e0 00 00 02 a0 00 00 02 e0 00 00
a0 00 25 01 05 05 28 51 04 80 00 00 02 a0 00 00 02 f0 00 00 02 a0 00 00 04 80 00 00 03 60 00 00 04 20 00 00 04 90 00 00
a0 00 25 02 05 05 28 51 03 60 00 00 04 50 00 00 02 d0 00 00 04 a0 00 00 03 f0 00 00 05 a0 00 00 04 80 00 00 04 b0 00 00
a0 00 25 03 05 05 28 51 03 e0 00 00 03 a0 00 00 03 90 00 00 05 60 00 00 05 50 00 00 06 e0 00 00 05 50 00 00 05 b0 00 00
a0 00 25 04 05 05 28 51 03 70 00 00 04 80 00 00 05 f0 00 00 03 f0 00 00 03 e0 00 00 02 a0 00 00 04 40 00 00 5d d2 9a 01
a1 00 24 00 05 05 28 51 52 a7 05 85 00 00 00 00 04 a0 00 00 05 50 00 00 05 70 00 00 05 00 00 00 05 00 00 00 04 90 00 00
a1 00 24 01 05 05 28 51 04 10 00 00 03 b0 00 00 05 60 00 00 03 e0 00 00 05 00 00 00 05 70 00 00 06 e0 00 00 03 a0 00 00
a1 00 24 02 05 05 28 51 05 50 00 00 05 a0 00 00 05 50 00 00 05 f0 00 00 05 00 00 00 05 70 00 00 05 40 00 00 05 00 00
a1 00 24 03 05 05 28 51 05 60 00 00 05 50 00 00 05 20 00 00 03 d0 00 00 05 70 00 00 05 f0 00 00 05 00 00 00 02 50 00 00
a1 00 24 04 05 05 28 51 04 20 00 00 04 b0 00 00 05 20 00 00 05 00 00 00 05 50 00 00 03 e0 00 00 05 70 00 00 cc d1 3e 39
a0 00 24 00 05 05 28 7a 50 ad 0a 85 00 00 44 00 04 b0 00 00 07 a0 00 00 06 f0 00 00 06 f0 00 00 06 80 00 00 09 00 00 00
a0 00 24 01 05 05 28 7a 07 70 00 00 05 f0 00 00 09 60 00 00 05 70 00 00 05 f0 00 00 05 f0 00 00 06 f0 00 00 07 60 00 00
a0 00 24 02 05 05 28 7a 06 50 00 00 05 f0 00 00 05 00 00 00 06 80 00 00 08 40 00 00 06 50 00 00 09 00 00 00 07 70 00 00
a0 00 24 03 05 05 28 7a 09 00 00 00 08 10 00 00 06 f0 00 00 07 50 00 00 0a 00 00 00 07 f0 00 00 08 50 00 00 08 20 00 00
a0 00 24 04 05 05 28 7a 07 b0 00 00 05 b0 00 00 04 b0 00 00 08 00 00 00 07 70 00 00 04 80 00 00 06 f0 00 00 a6 72 6e 98
a1 00 25 00 05 05 28 7a 52 a8 09 85 00 00 00 00 05 a0 00 00 04 80 00 00 05 f0 00 00 04 50 00 00 05 f0 00 00 06 f0 00 00
a1 00 25 01 05 05 28 7a 05 40 00 00 05 10 00 00 05 70 00 00 05 a0 00 00 05 70 00 00 07 20 00 00 05 a0 00 00 06 f0 00 00
a1 00 25 02 05 05 28 7a 05 50 00 00 06 d0 00 00 06 b0 00 00 07 50 00 00 06 80 00 00 06 f0 00 00 06 b0 00 00 06 50 00 00
a1 00 25 03 05 05 28 7a 05 a0 00 00 06 a0 00 00 08 10 00 00 05 a0 00 00 05 00 00 00 06 80 00 00 06 80 00 00 05 d0 00 00
a1 00 25 04 05 05 28 7a 00 30 00 00 06 80 00 00 03 a0 00 00 05 f0 00 00 04 90 00 00 06 b0 00 00 05 50 00 00 5e 8a db 54
a0 00 25 00 05 05 28 7a 50 ad 0a 85 00 00 00 00 05 90 00 00 02 00 00 00 02 00 00 00 02 e0 00 00 02 a0 00 00 02 d0 00 00
a0 00 25 01 05 05 28 7a 04 60 00 00 02 60 00 00 03 10 00 00 02 a0 00 00 04 80 00 00 03 50 00 00 04 20 00 00 04 50 00 00
a0 00 25 02 05 05 28 7a 03 60 00 00 04 80 00 00 02 d0 00 00 04 b0 00 00 03 d0 00 00 05 a0 00 00 04 b0 00 00 05 00 00 00
a0 00 25 03 05 05 28 7a 03 d0 00 00 03 90 00 00 03 a0 00 00 05 70 00 00 05 40 00 00 06 d0 00 00 05 70 00 00 05 a0 00 00
a0 00 25 04 05 05 28 7a 03 70 00 00 04 80 00 00 05 f0 00 00 04 10 00 00 03 f0 00 00 02 a0 00 00 04 50 00 00 34 16 8f c2
a1 00 24 00 05 05 28 7a 52 a8 09 85 00 00 00 00 04 a0 00 00 05 40 00 00 03 90 00 00 05 00 00 00 05 00 00 00 04 90 00 00
a1 00 24 01 05 05 28 7a 04 10 00 00 03 a0 00 00 05 90 00 00 03 e0 00 00 05 00 00 00 05 70 00 00 06 e0 00 00 03 a0 00 00
```

FPGA counter

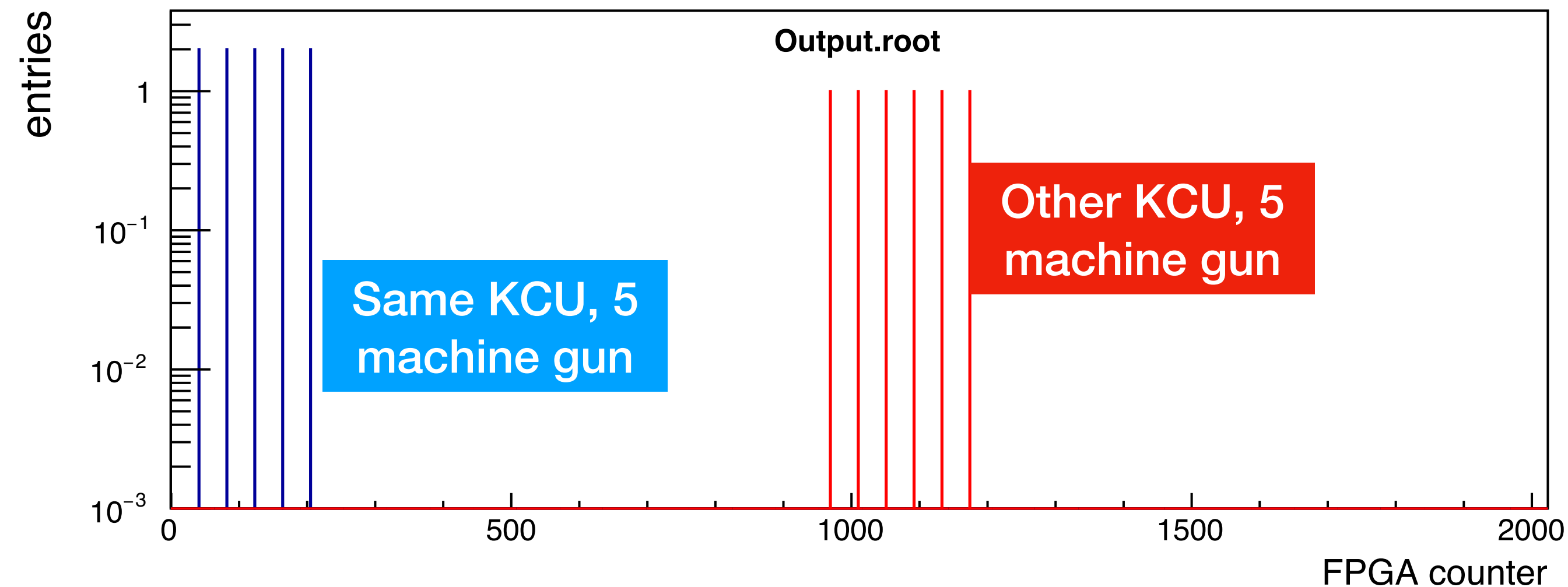
ASIC, FPGA ID

# Synchronization process offline

## Procedure for analysis:

- Collect 20 lines of KCU information:
  - Has to have the same FPGA time stamp
  - Contains all readout for 2 ASICs, both sides
  - Create root file
- Create events using full KCU information:
  - Take one FPGA counter reference
    - Compare the difference to it with the same FPGA ID:
      - This will collect the same machine guns
    - Compare the difference to it with a different FPGA ID:
      - This will collect the other KCU information
      - There is an expected offset:
        - This offset changes run-by-run, but very stable
  - Tag all the used FPGA counters

## 1 event example



# Software development

H2GConfig

Register: Channel\_54

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 1	Gain_conv<0>	Gain_conv<1>	Inputdac<5>	Inputdac<4>	Inputdac<3>	Inputdac<2>	Inputdac<1>	Inputdac<0>
0	0	0	0	0	0	0	0	0
Byte 2	trim_toa<5>	trim_toa<4>	trim_toa<3>	trim_toa<2>	trim_toa<1>	trim_toa<0>	sel_trig_toa	mask_toa
1	0	0	0	0	0	0	0	0
Byte 3	trim_tot<5>	trim_tot<4>	trim_tot<3>	trim_tot<2>	trim_tot<1>	trim_tot<0>	NA	NA
2	0	0	0	0	0	0	0	0
Byte 4	trim_inv<5>	trim_inv<4>	trim_inv<3>	trim_inv<2>	trim_inv<1>	trim_inv<0>	probe_noinv	probe_inv
3	0	0	0	0	0	0	0	0
Byte 5	probe_toa	probe_tot	mask_tot	sel_trig_toa	Channel_off	HighRange	LowRange	probe_pa
4	0	0	0	0	0	0	1	0
Byte 6	mask_adc	NA	DAC_CAL_CT DC_TOT<5>	DAC_CAL_CT DC_TOT<4>	DAC_CAL_CT DC_TOT<3>	DAC_CAL_CT DC_TOT<2>	DAC_CAL_CT DC_TOT<1>	DAC_CAL_CT DC_TOT<0>
5	0	0	0	0	0	0	0	0
Byte 7	HZ_inv	HZ_noinv	DAC_CAL_FT DC_TOA<5>	DAC_CAL_FT DC_TOA<4>	DAC_CAL_FT DC_TOA<3>	DAC_CAL_FT DC_TOA<2>	DAC_CAL_FT DC_TOA<1>	DAC_CAL_FT DC_TOA<0>
6	0	0	0	0	0	0	0	0
Byte 8	NA	NA	DAC_CAL_FT DC_TOT<5>	DAC_CAL_FT DC_TOT<4>	DAC_CAL_FT DC_TOT<3>	DAC_CAL_FT DC_TOT<2>	DAC_CAL_FT DC_TOT<1>	DAC_CAL_FT DC_TOT<0>
7	0	0	0	0	0	0	0	0
Byte 9	NA	NA	DAC_CAL_FT DC_TOA<5>	DAC_CAL_FT DC_TOA<4>	DAC_CAL_FT DC_TOA<3>	DAC_CAL_FT DC_TOA<2>	DAC_CAL_FT DC_TOA<1>	DAC_CAL_FT DC_TOA<0>
8	0	0	0	0	0	0	0	0
Byte 10	NA	NA	IN_FTDC_EN CODER_TOA<5>	IN_FTDC_EN CODER_TOA<4>	IN_FTDC_EN CODER_TOA<3>	IN_FTDC_EN CODER_TOA<2>	IN_FTDC_EN CODER_TOA<1>	IN_FTDC_EN CODER_TOA<0>
9	0	0	0	0	0	0	0	0
Byte 11	DIS_TDC	NA	IN_FTDC_EN CODER_TOT<5>	IN_FTDC_EN CODER_TOT<4>	IN_FTDC_EN CODER_TOT<3>	IN_FTDC_EN CODER_TOT<2>	IN_FTDC_EN CODER_TOT<1>	IN_FTDC_EN CODER_TOT<0>

## Slow Control for the H2GCROC:

- N FPGA with 2 H2GCROC setup (1x2 in this case)
- All registers are settable and working

## DAQ is very simple:

- File or terminal dump
- Generator settings - all in 40MHz
- External trigger
  - Ext. trigger delay - needs to avoid the UDP packet loss
- Daq push - 1 event
- HV on/off for the board
- Adjustment if there is a misalignment, debugging

H2GDAQ

Working Folder: /home/epical/PythonCodes/NewGit/H2GDAQ

DAQ Settings

- event: 100
- time [sec]: 1
- manual:

Run Number: 35

Data Count: 8.46 MB

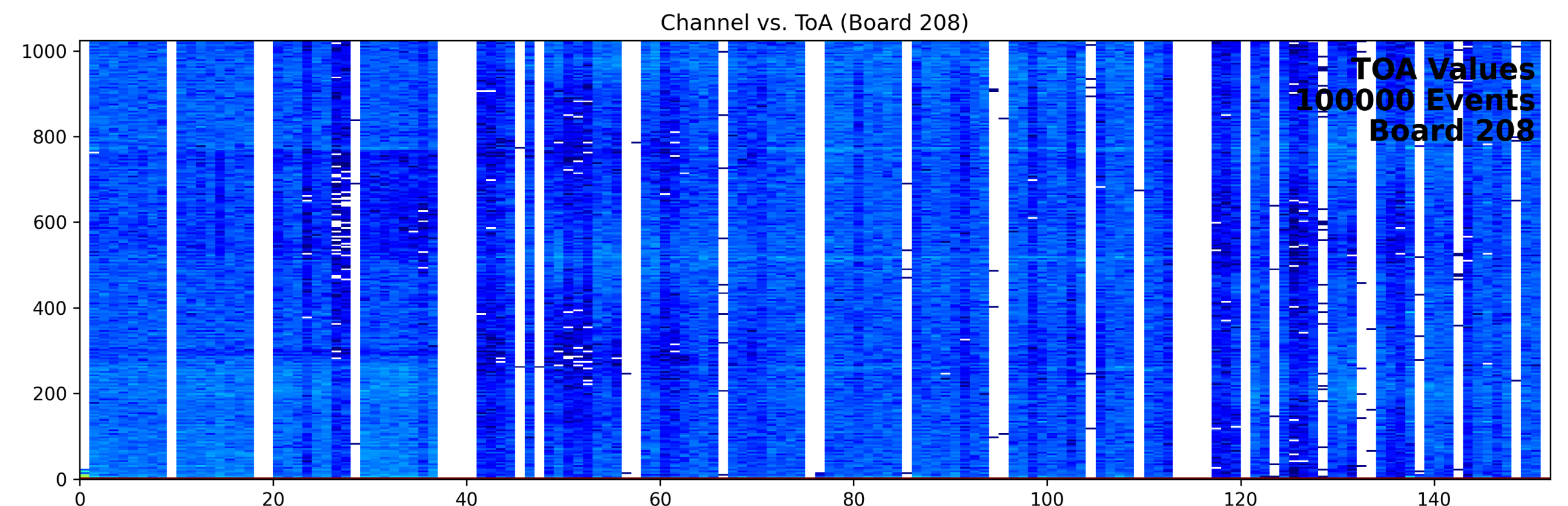
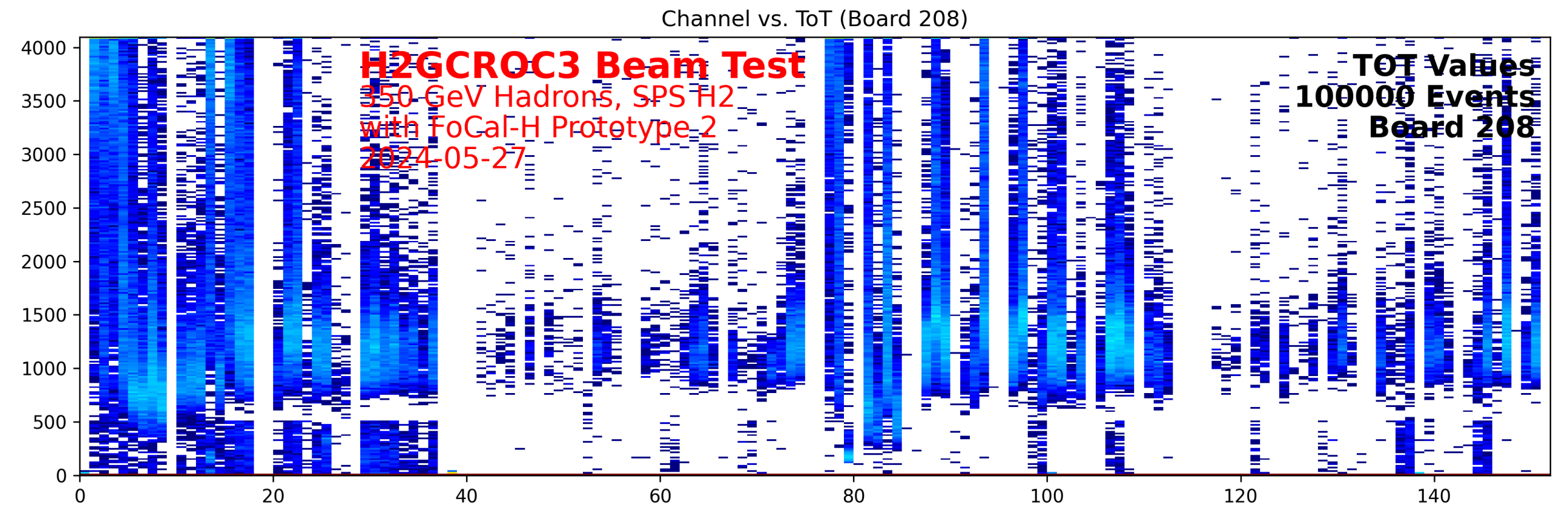
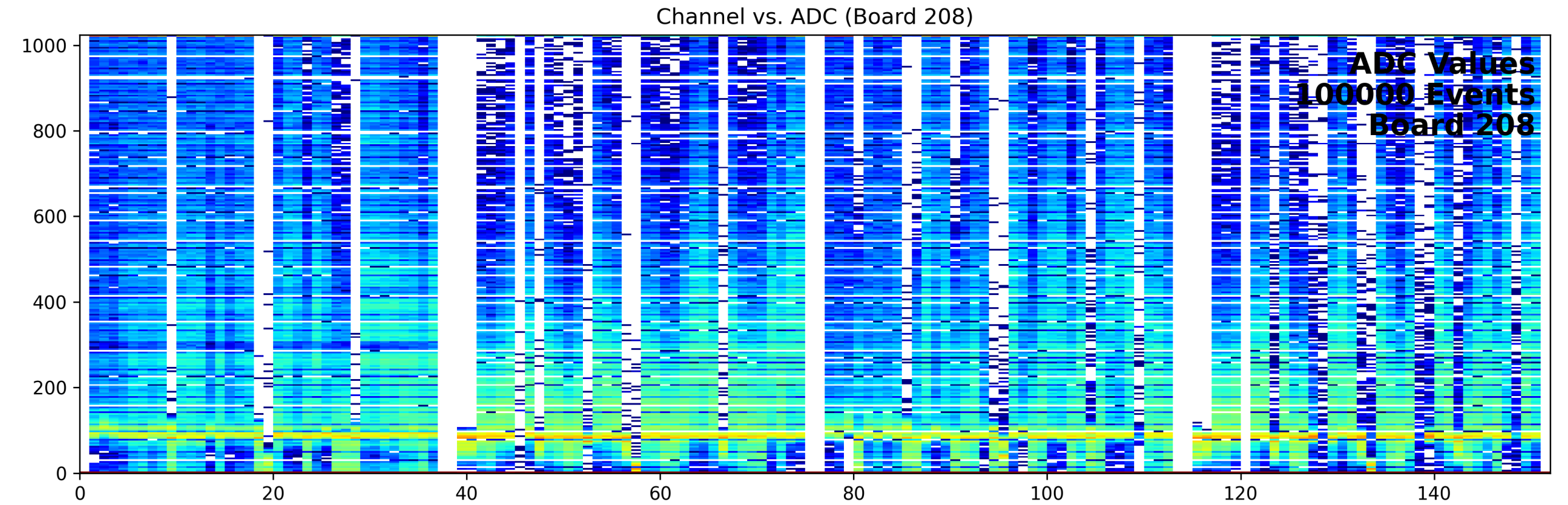
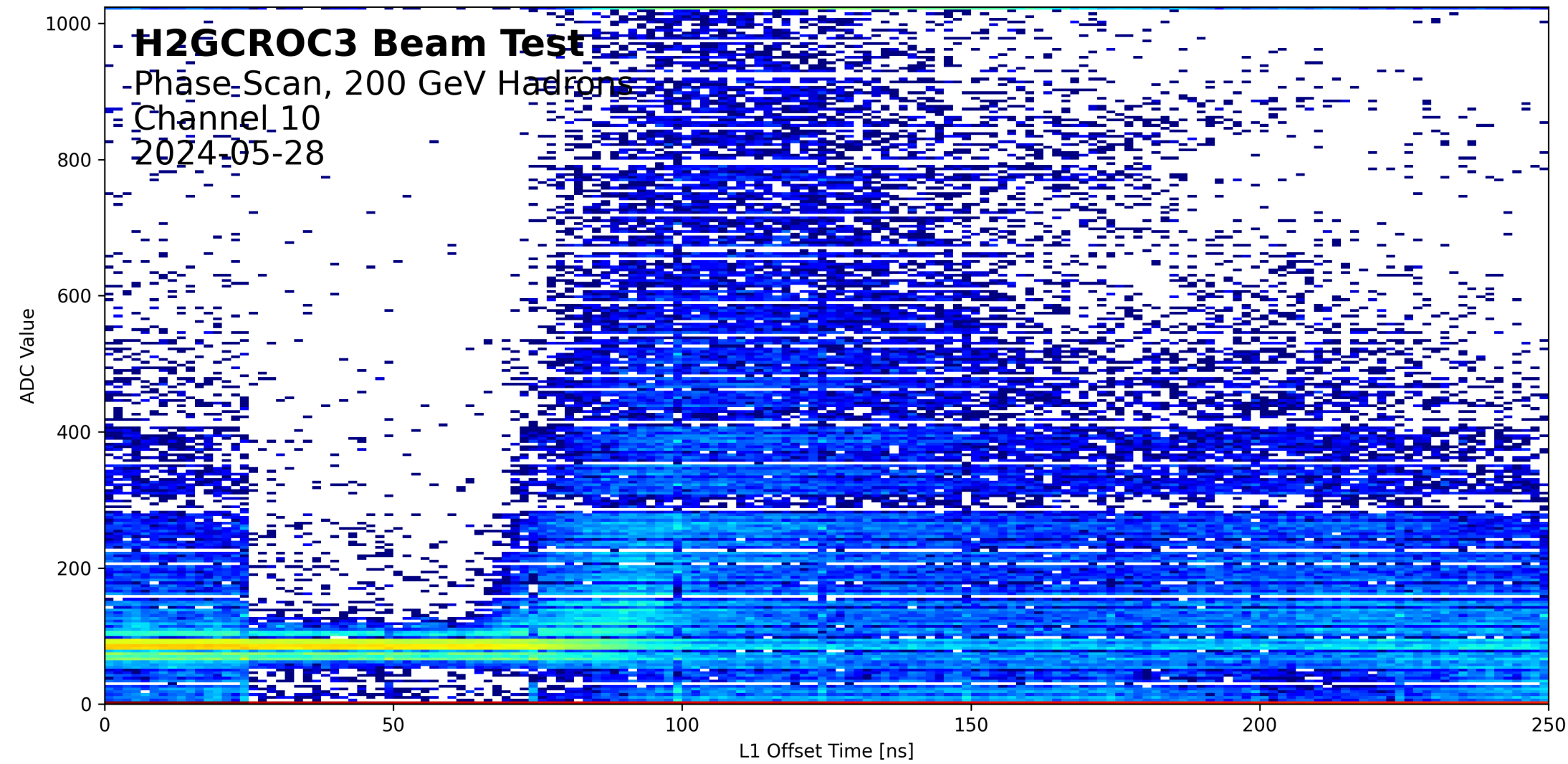
Generator Settings

- Gen PreImp En:
- Gen Pre Int: 16
- Gen Nr Cycles: 1000
- Gen Interval: 100000
- Ext Trg En:
- Ext Trg Delay: 0
- Ext Trg DeadT: 255
- DAQ FCMD: 75
- DAQ Push FCMD: 75
- Gen Pre FCMD: 45
- Gen FCMD: 75
- Machine Gun: 10

High Voltage:  F0  A0  A1

Buttons: DAQ Push, Start Generator, Stop Generator, Start DAQ, Stop DAQ, Send Gen Config, Send HV Settings

# Some very early results



## Some very early results:

- 60-350 GeV hadron scan
- 60-200 GeV electron scan
- 200 GeV hadron and positron position scan
- Phase scan to see the whole SiPM signal

Two KCU's were synced throughout the run, no issue to combine them so far

TOA and TOT are responding, need to do a good QC of the data

# Summary

## **Hardware:**

- Done, 6 boards (1 France, 5 with me)

## **Firmware:**

- Done

## **Software:**

- Work in progress:
  - I2C GUI interface - done
  - I2C terminal setup - work-in-progress - needed for fast calibration
  - DAQ GUI interface - done
  - DAQ terminal setup - work-in-progress - again, calibration

## **More to come:**

- Production and testing of summing boards
- Testing of the Samtec cables (firmware ready)
- LED testing