





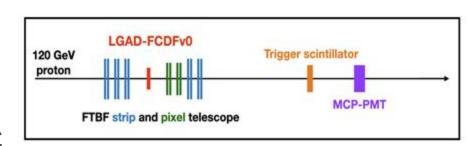
FCFD - AC-LGAD Strip Readout

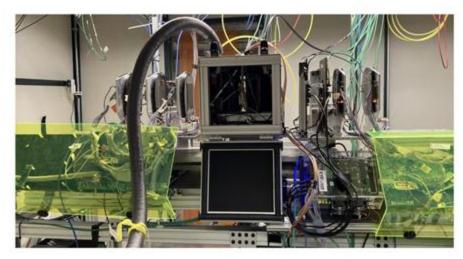
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eRD109 Monthly Progress Reports Aug 1, 2024

Proton Beam Measurements

- Use Fermilab Testbeam Facility to test CFD chip with 120 GeV protons
- MCP-PMT used as time reference detector
- Temperature maintained at 20C
- Tracking telescope used to measure hit positions and efficiency

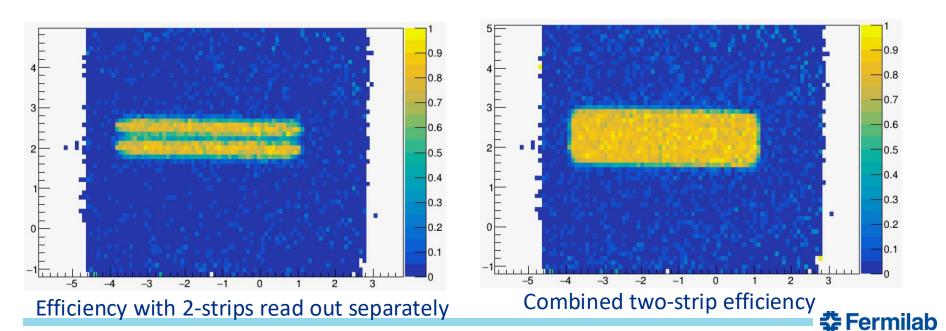






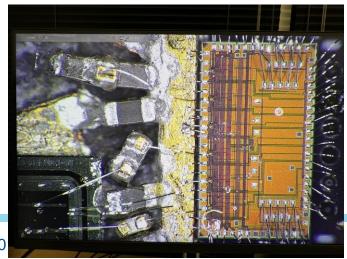
FCFDv1 test beam in May

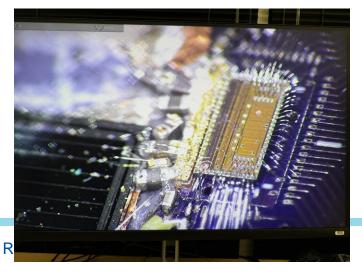
- Testing in the Fermilab beam in May 2024
 - Connected to a 5 mm strip AC-LGAD sensor, 500 μm pitch, 50 μm thick
- Optimizing the readout board grounding, power supplies, noise
 - Two-strip efficiency demonstrated to be 100%
 - The noise was observed to be too high, causing the comparator to fire too frequently, causing fake hits



FCFDv1 test beam in June

- Modified the board for test beam in June
 - Mounted on a specially designed low-noise readout board, improved layout and optimized components
 - Added a 7-pF capacitor in series to the AC-LGAD sensor, to reduce the noise and avoid fake hits, and reduce input capacitance
 - Fake hits are reduced, at the cost of ~1/2 of signal size to the chip input
- Mounted a DC-LGAD with 2 pixels (1.3x1.3 mm²) connected
 - The DC-LGAD sensors would allow to test and characterize the performance of the chip, without the RC-network effects

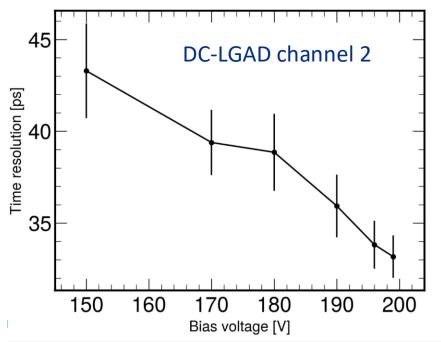


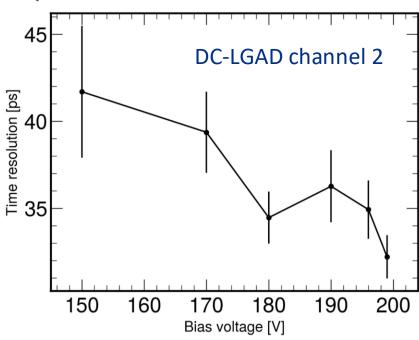




FCFDv1 test beam in June: DC-LGAD results

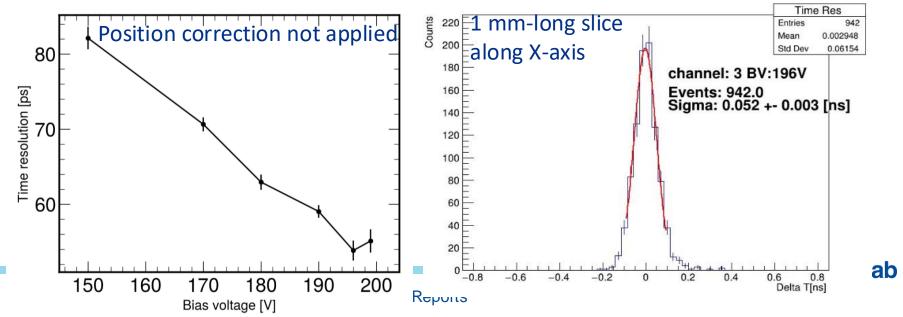
- Performed bias scan BV = 150V, 170V, 180V, 190V, 196V and 199V (breakdown above 200 V)
- Achieve time resolution around 32 ps
 - No time-walk observed, no time-walk correction applied
 - Signal amplitudes around 300 mV
 - Chip performs well for sensors with expected characteristics





FCFDv1 test beam in June: AC-LGAD results

- Time resolution on the AC-LGAD channel achieves around 55 ps
 - Due to series capacitor, MPV signal size of strip reduced by more than half: ~130 mV (AC-LGAD) compared to 300 mV (DC-LGAD)
 - Time resolution for the whole strip 55 ps (without correcting for position)
 - Time resolution in 1mm slices along strip: 52 ps (will implement correction)
- σ_T for DC-LGADs with 130 mV signals ~ 50 ps
 - Indicates that AC-LGAD should get σ_T ~35 ps with improved comparator



Development plans in 2024 and 2025

- Finalize testing of FCFDv1
 - Test with IR-laser to study the effect of increased signal from AC-LGADs on time resolution
 - Re-optimize the chip with the final-spec AC-LGAD parameters as tested with FCFDv1 version, for a minor revision FCFDv1.1
- Next focus on the full chip: full-size FCFD v2 end of 2025
 - Finalize the geometry and sensor key parameters (strip length, sheet resistance and thickness)
 - Complete ASIC with readout that would interface with the EIC experimental DAQ
 - Implement the interfaces with RDO
- The final ASIC (v3) to be produced end of 2026

