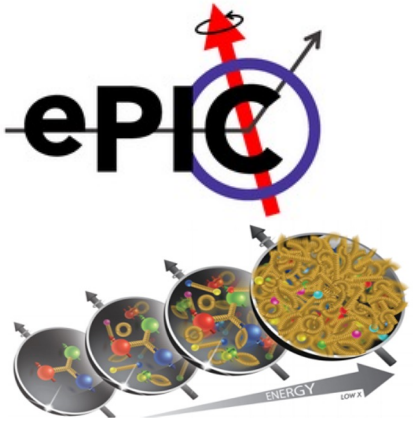


Support from DOE/eRD109

The EICROC Project

Objective: **Development** and **Characterization** of an **ASIC EICROC (32 x 32)**
able to read out the new generation of pixelated (500 x 500 μm^2) silicon sensors: **AC-LGAD**
(**L**ow-**G**ain **A**valanche **D**iode) coupled **AC**
for the **Electron Ion Collider** (EIC)

1st intention: optimized for Far Forward detectors: **Roman Pots**

Perspectives: to read out **AC-LGAD** sensors implemented in other ePIC detectors, e.g. OMD, Forward TOF, …

Stepping up through succesive ASIC iterations
to control performances fulfilling ePIC detector requirements

- **EICROC0 prototype** (16 channels; 4 x 4): under characterization since mid '23

EICROC Project: last progress reports

- ePIC « Electronics & DAQ Review », Christophe de La Taille, July 10-11, 2024
- eRD109 FY24 report & FY25 proposal:

Institution	Resource	FTE (%)	Budget (k$)
IJCLab	Senior associate scientist	70	0 (in-kind)
	Senior scientist	35	0 (in-kind)
	Senior scientist	20	0 (in-kind)
	Research engineer	25	0 (in-kind)
	Post-Doc	100	0 (in-kind)
	Fabrication of testboards and associated components	-	25
OMEGA	Senior research engineer	25	0 (in-kind)
	Senior research engineer	20	0 (in-kind)
	Research engineer	15	0 (in-kind)
	Research engineer	50	0 (in-kind)
	Assistant engineer	20	0 (in-kind)
	contribution to EICROC/CALOROC engineering run	-	70
	BGA substrate tooling for CALOROC	-	30
CEA/Irfu	Senior research engineer	30	0 (in-kind)
Total	-	-	**125**

- EICROC0 testing meeting, Adrien Verplancke (OMEGA), Arzoo Sharma (IJCLab), July 19th, 2024
- EICUG/ePIC collaboration meeting/AC-LGAD Workfest, Adrien Verplancke (OMEGA), July 26th, 2024

EICROC Project: EICROC0 Testing Update

- EICROC0 testing meeting, Adrien Verplancke (OMEGA), Arzoo Sharma (IJCLab), July 19th, 2024
- EICUG/ePIC collaboration meeting/AC-LGAD Workfest, Adrien Verplancke (OMEGA), July 26th, 2024

Main Update: Issue preventing TDC & ADC measurements **FIXED** mid-July. 😀

The EICROC0 chip receives a 160MHz clock from the FPGA. This 160 MHz colcks gets converted internally to a 40MHz. An issue with optional clock delay blocks on the FPGA was found mid-July that was adding a significant jitter to the clock, which disturbed all TDC & ADC measurements.

This issue was fixed updating the firmware.

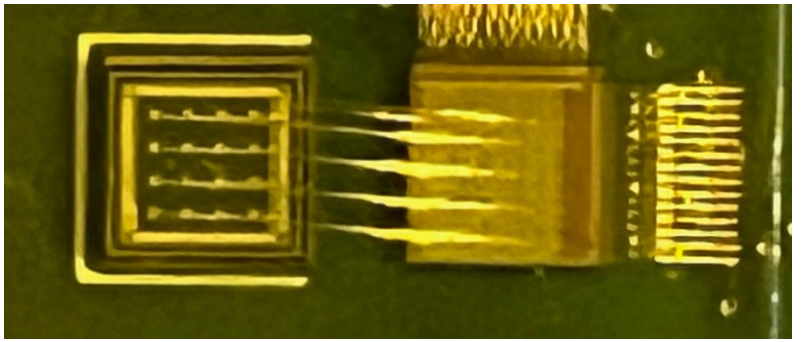
(«2023» & «2024» EICROC0 PCBs can be equally exploited with the updated firmware)

- **TDC & ADC measurements:**
  no more show stopper, ramping up on fine tuning investigations

EICROC Project: EICROC0 boards under test (OMEGA, IJLab)

- Boards without an AC-LGAD sensor: **#2.1** and **#2.2** (updated «2024» PCB)
  c_D = 11 (additional 750 fF @ preamp input), c_P = 1

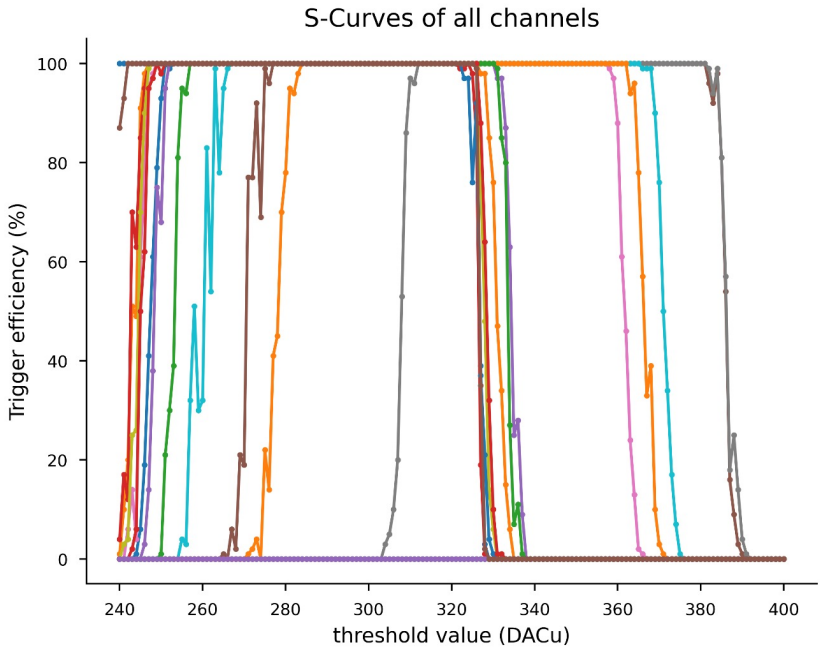
- Boards with an AC-LGAD sensor wire-bonded by IPHC Strasbourg (France): **#2.3A** and **#2.3B** (updated «2024» PCB)
  c_D = 00 (no additional capacitance @ preamp input), c_P = 1



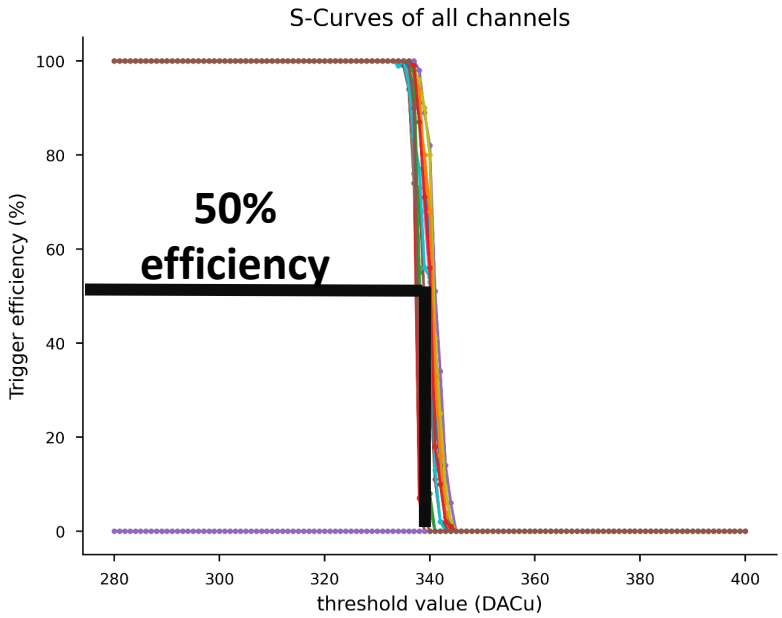
+ boards without AC-LGADs («2023» PCB)
+ 1 boards with an AC-LGAD sensor wire-bonded by BNL («2023» PCB)

EICROC Project: EICROC0 recent results (OMEGA, IJLab)

Board #2.2 (with sensor depleted, HV = -100V ; 1 µA) @ 5 fC

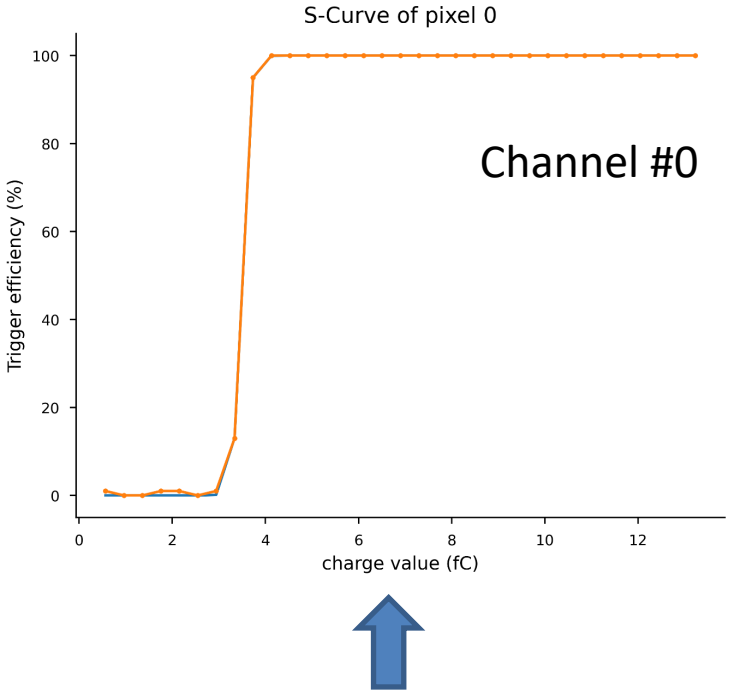


S-Curve corrected by means of individual pixel DACs

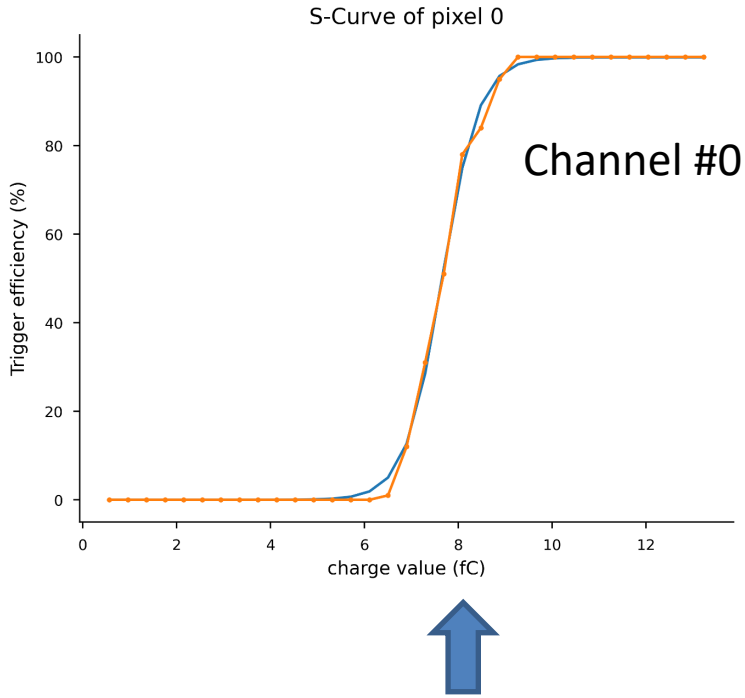


A. Verplancke et al. (OMEGA)

Minimum charge detected



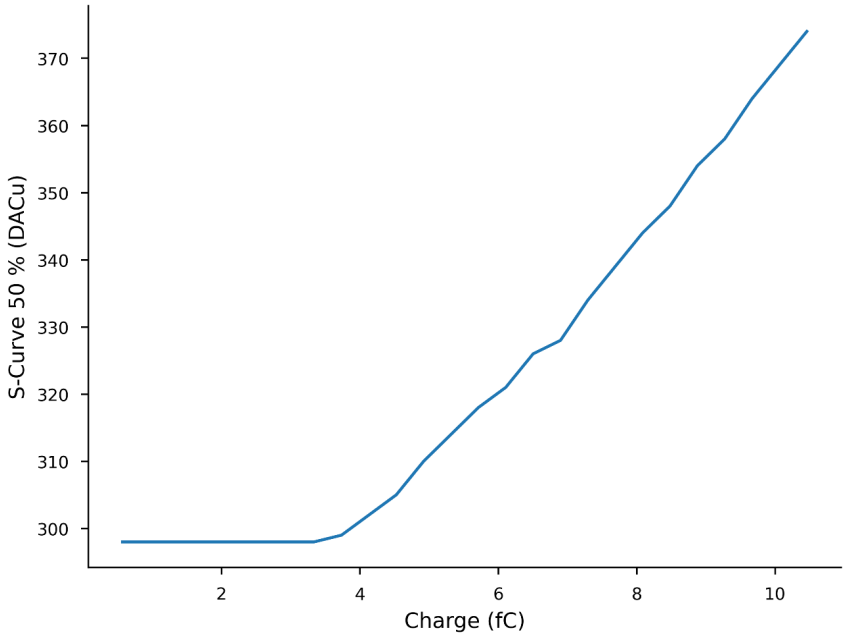
Without Sensor : 3.5 fC
Noise = 0.25 fC
Threshold = 300 DACu



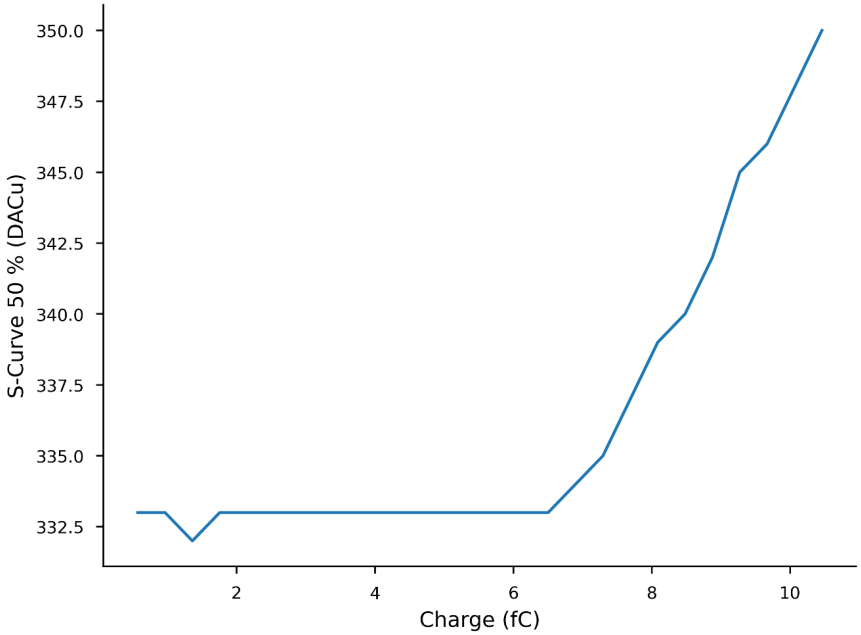
With Sensor (depleted, HV = -100 V): 7.65 fC
Noise = 0.66 fC
Threshold = 340 DACu

A. Verplancke et al. (OMEGA)

S-Curve 50% versus injected charge (channel #0)



Without Sensor

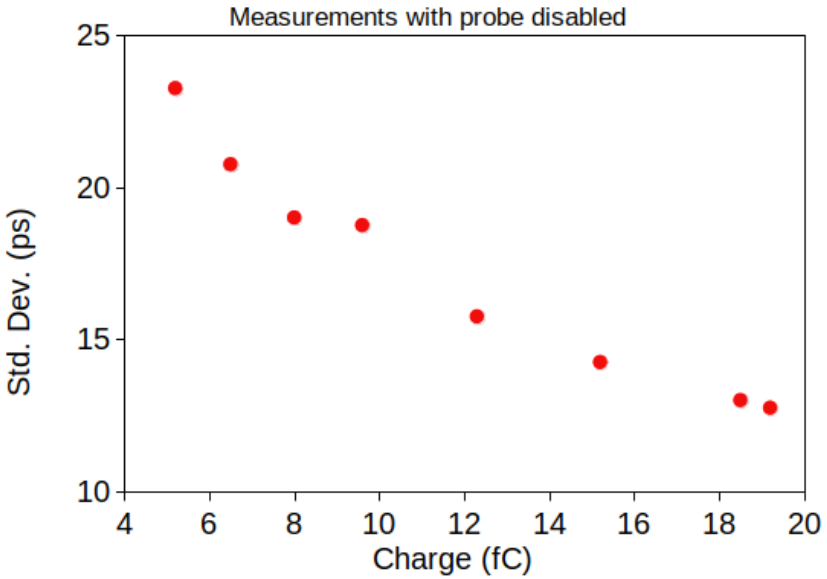


With Sensor

A. Verplancke et al. (OMEGA)

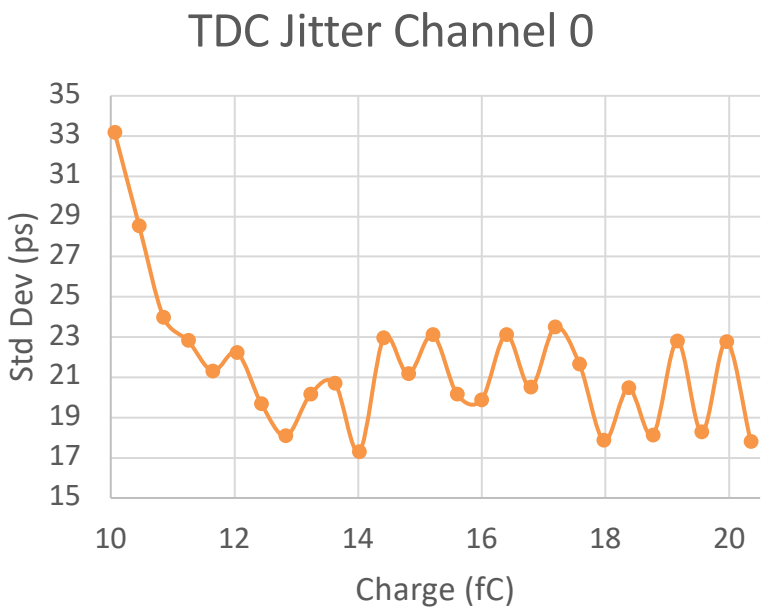
EICROC Project: EICROC0 recent results (OMEGA, IJLab)

TDC Jitter versus injected charge



Without Sensor
(board #2.1 - no sensor , channel #1)
Jitter ~17 ps @ 10 fC
~12.5 ps @ 20 fC
(Threshold = 135 DACu)

A. Sharma et al. (IJCLab)



With Sensor (#2.3B)
Jitter ~33 ps @ 10 fC
~20 ps @ 20 fC
(Threshold = 340 DACu)

A. Verplancke et al. (OMEGA)

EICROC Project: EICROC0 recent results (OMEGA, IJLab)

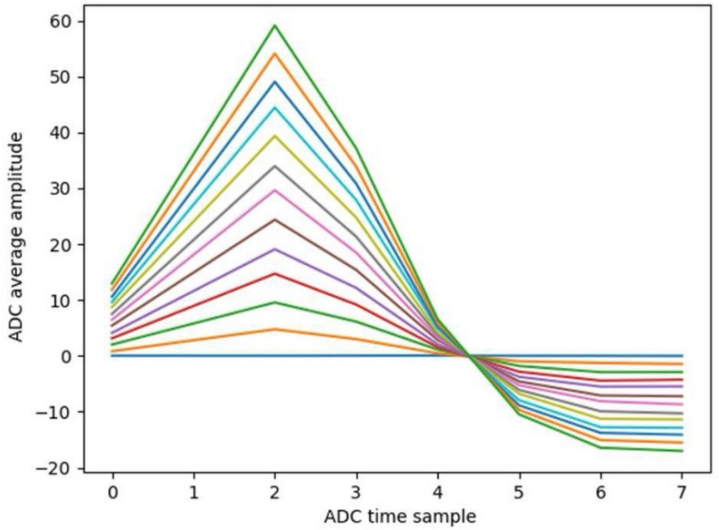
Measurement	ASIC Without Sensor	ASIC With Sensor
Min. detected charge	3.5 fC	7.65 fC
Noise value	0.26 fC	0.66 fC
TDC Jitter @ 10 fC	17.5 ps	33 ps
TDC Jitter @ 20 fC	12.5 ps	20 ps

Impact of the sensor will be further investigated

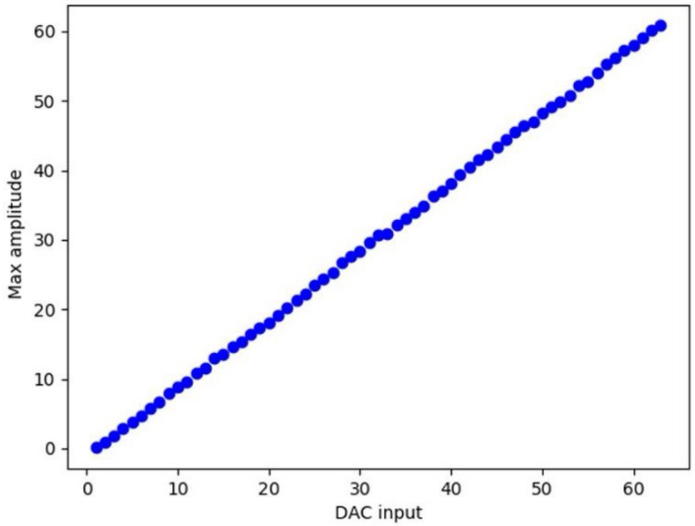
ADC studies (preliminary)

Board #2.1 (no sensor, channel #1)

No clock gating, pedestal subtraction of DAC = 1



Different amplitude from 1 to 61 (step = 4)



ADC response linearity

Cross-talk measurements underway: two neighbors investigated (2 and 5)

For very small signal: no clear xtalk but going to the largest charge, a negative signal appears.

If the minimum of the amplitude of the ADC scales linearly with the injected charge as expected for XTalk,

Typically 1 ADC amplitude of Xtalk for a signal of 60 ADC => between 1 and 2 % Xtalk,

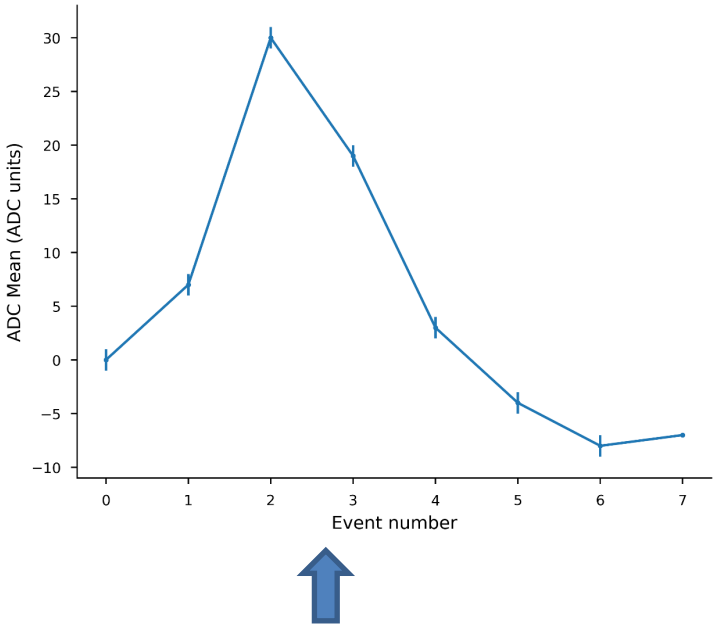
quite in agreement with previous Probe Preamp. measurements (2023)

L. Serin et al. (IJCLab)

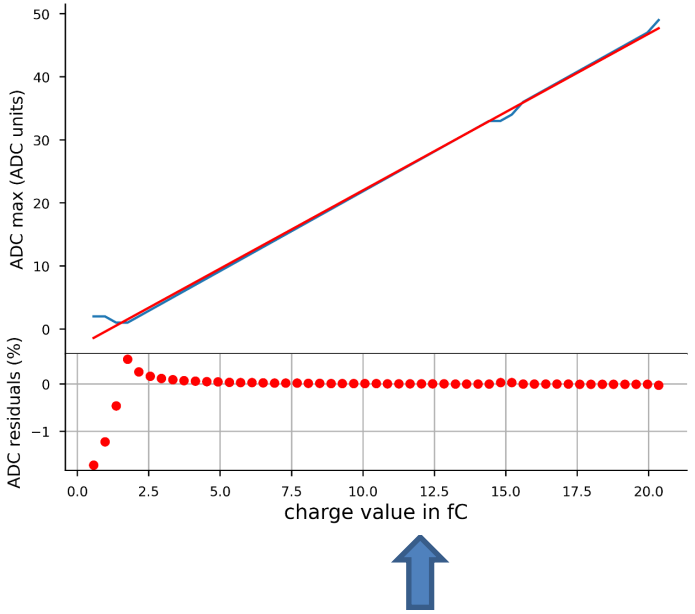
ADC studies (preliminary)

Board #2.3B (with sensor, channel #0)

No clock gating, pedestal subtraction of DAC = 1



ADC Pulse reconstruction
(obtained after pedestal subtraction)



ADC response linearity

A. Verplancke et al. (OMEGA)

EICROC Project: EICROC0 Summary & Perspectives

- Issue preventing acurate TDC & ADC measurements **FIXED** by means of firmware update
- Each EICROC0 components (Preamp., TDC and ADC) works as expected by design
- Now start TDC & ADC fine tunings with & without an AC-LGAD sensor
- Infrared laser measurements foreseen shortly at BNL
- Thorough characterization of boards with an AC-LGAD sensor wire-bonded
- Beta source measurements foreseen after the summer (IJClab, BNL)

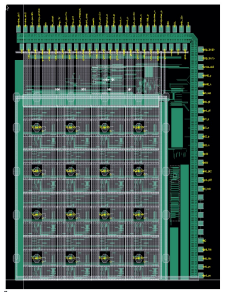
❖ **Perspectives:**

- **EICROC0 bump-bonded to an AC-LGAD**, prestation)
- Characterization of electronics r**sensor** (flip chip to be provided by BNL)
  Wire-bonding of hybrids onto uodated PCBs (IPHCesponses (PA, TDC, ADC)
- Beta Source (evaluation of charge sharing) & IR laser (evaluation of spatial resolution)
- **Test beam in Spring 2025 (submitted to ePIC collaboration)**

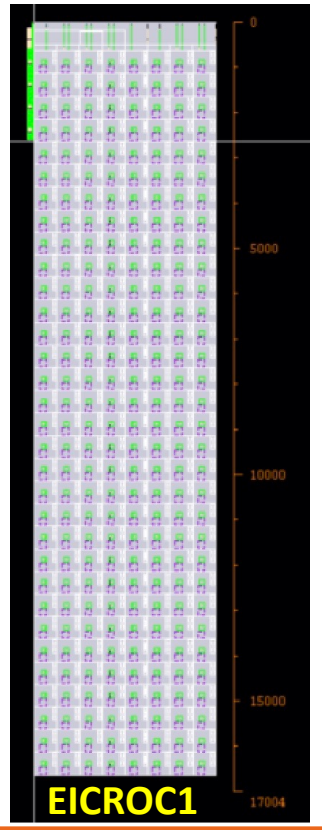
EICROC Project: Perspectives

- **EICROC0** is a testbeam prototype => sensor characterization
  - Present power ~2 mW/ch + 4*20 mW « analog probe preamp »
  - ADC power + shaper/driver to be reduced from ~1 mW to 100 µW/ch
    => **EICROC0A (Submission @ end of 2024)**

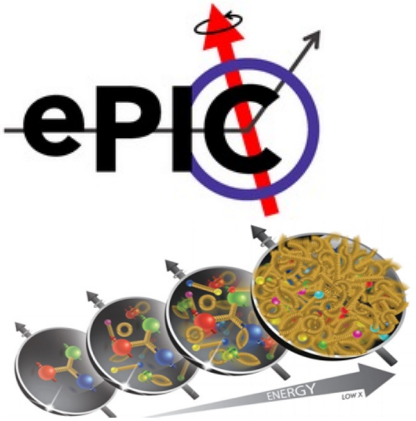
EICROC0A



- **EICROC1** will address larger dimensions more likely **8x32**
  - Address floor planning and power distribution
  - Option for selective readout : hit + 8 neighbouring channels
  - Status : layout started based on EICROC0, adding more testability
  - Still EICROC0-like readout
  - **Submission @ end of 2024 (together with EICROC0A & CALOROC)**



- **EICROC2** final size : 32x32



Thank you for your attention

The EICROC Project French team:

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Support from DOE/eRD109