



ALCOR - dRICH Readout

Fabio Cossio on behalf of the ALCOR group
INFN Torino

EPIC Electronics & DAQ WG meeting
eRD109 Monthly Progress Reports

01.08.2024

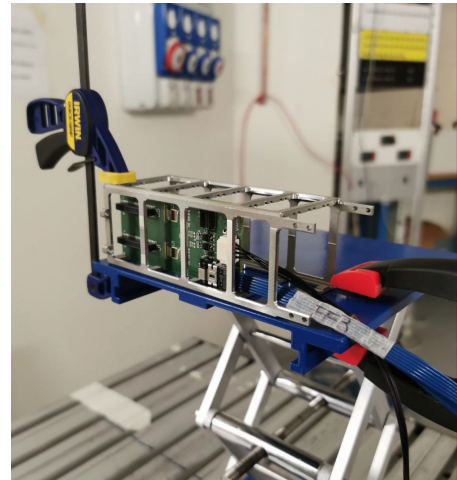
ALCOR irradiation tests

SEU/SEL and TID tests at Centro of Proton-Therapy in Trento with ALCOR v2.1 (July 2024)

- Beam: 100 MeV proton
- Intensity: 10 - 100 nA
- Runs: typically 600 s
- Fluence collected per run: $10^{11} - 10^{12}$ p/cm²

➤ **Total TID: 436 krad**

➤ **Total fluence: $4.64 \cdot 10^{12}$ p/cm²**



Other requirements: radiation tolerance



The dRICH-PDUs are in a moderately hostile radiation environment

- Φ (p+n > 20 MeV) = 200 Hz/cm²
 - TID \cong 650 rad (for 1000 fb⁻¹) < 1 krad
- } note these values include a safety factor 5

SEU-SEL

- **Pixel** configuration registers and FSMs **already protected against SEU** in ALCOR v2
- TMR SEU **protection added also for periphery** configuration registers, Hamming code SEU protection for FSMs: Single Error Correction, Double Error Detection codes (SECDED)
- On board prevention of SEL: **current monitor** on FEB regulators

TID

- Same technology already verified for TID up to a **few hundreds of krad**
- Also other FEB components will be tested and validated

- Irradiation tests campaign: SEU/SEL and TID tests at Centro of Proton-Therapy in Trento with ALCOR current version foreseen in July 2024

ALCOR SEU/SEL

ECCR/BCR/PCR registers checked against SEU (every second)

- ECCR $\sigma = (9.4 \pm 1.8) \cdot 10^{-14} \text{ cm}^2/\text{bit}$ periphery register \rightarrow no TMR in ALCOR v2.1
- BCR $\sigma = (7.6 \pm 1.1) \cdot 10^{-14} \text{ cm}^2/\text{bit}$ periphery register \rightarrow no TMR in ALCOR v2.1
- PCR $\sigma = (3.3 \pm 0.5) \cdot 10^{-15} \text{ cm}^2/\text{bit}$ pixel register \rightarrow TMR

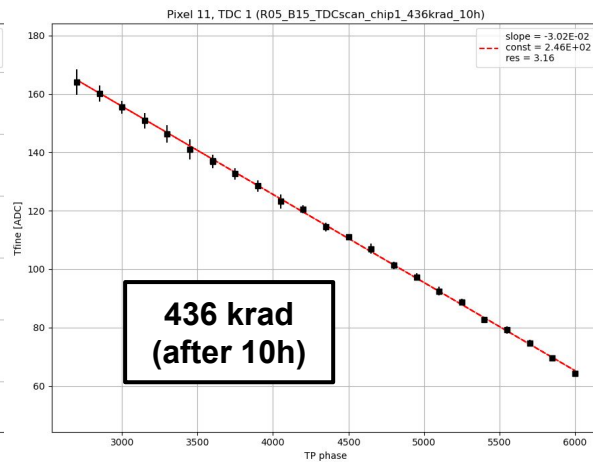
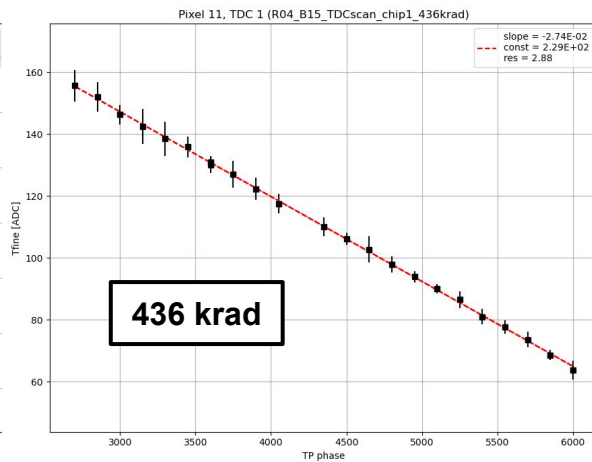
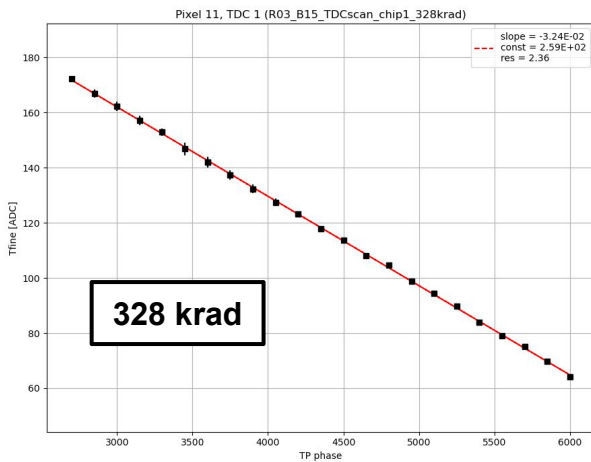
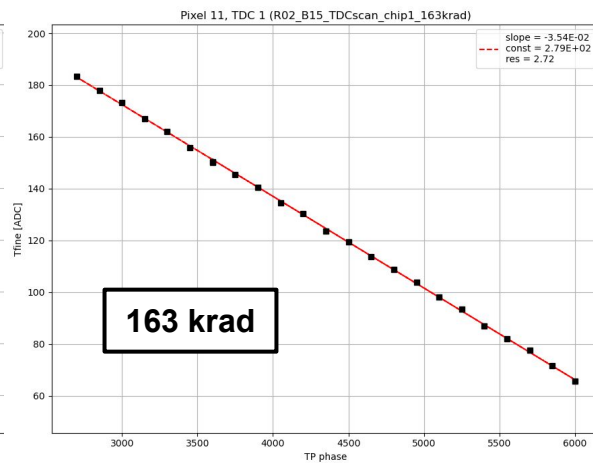
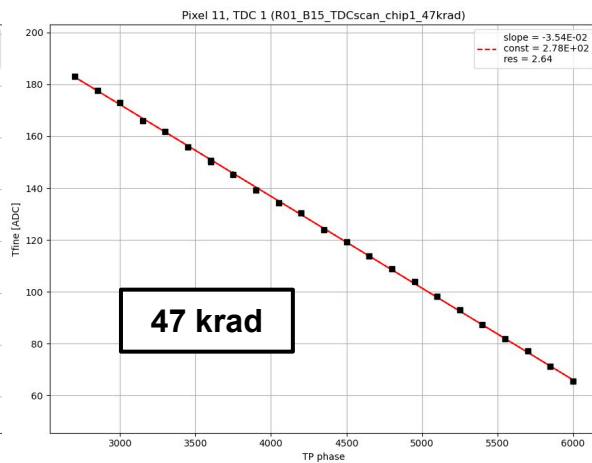
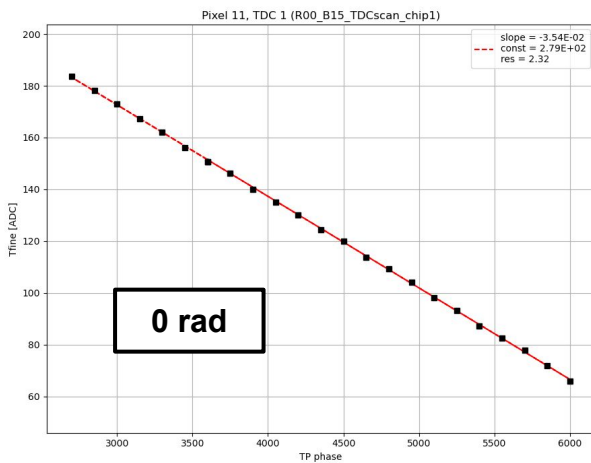
SEU rate in ePIC:

- dRICH Flux = 20 ($h > 20 \text{ MeV}$) / ($\text{cm}^2 \text{ s}$)
- ALCOR bits: (2048 + 192) = 2240 \rightarrow ALCOR-64 bits will be 4480
- Total ALCOR: 4992
- Total bits: 4992 \cdot 4480 = $2.2 \cdot 10^7$ bits

➤ $\sigma = 3.3 \cdot 10^{-15} \text{ cm}^2/\text{bit} \rightarrow \text{MTBF} = 6.9 \cdot 10^5 \text{ seconds} \rightarrow \text{every 191 hours}$

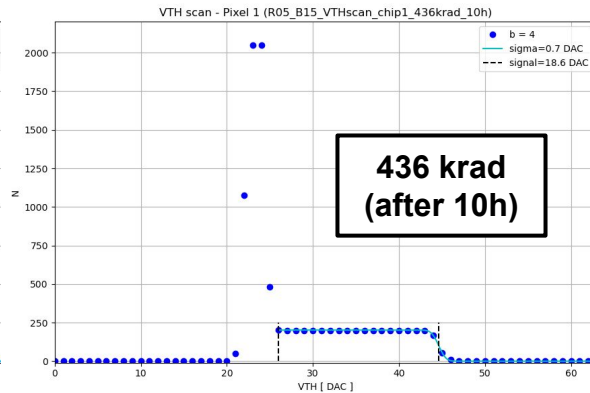
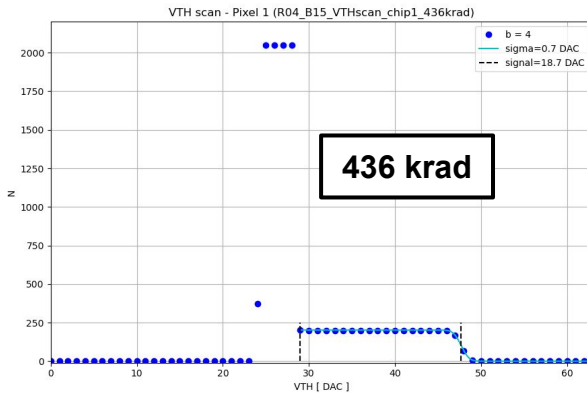
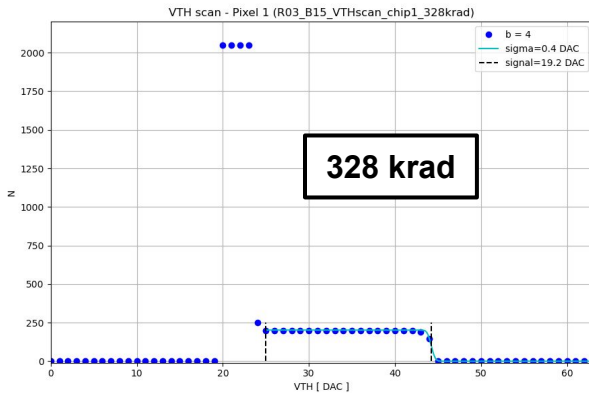
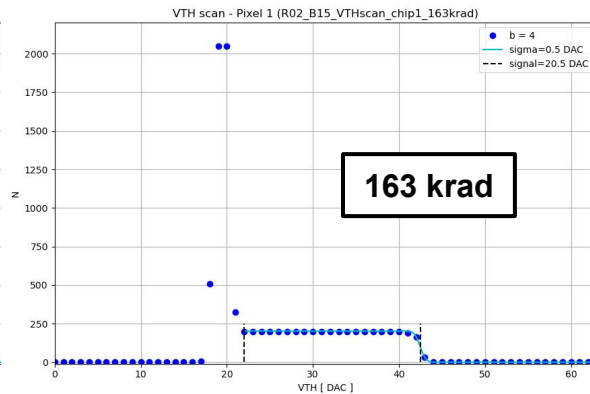
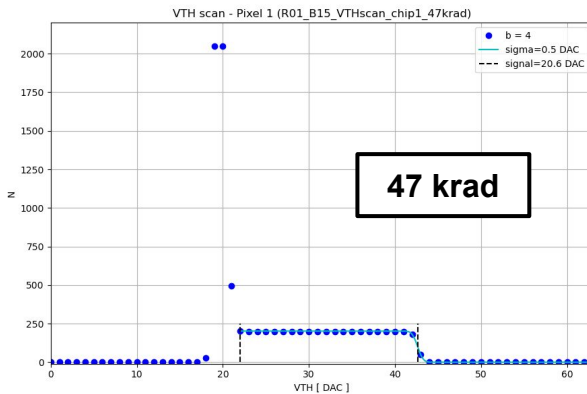
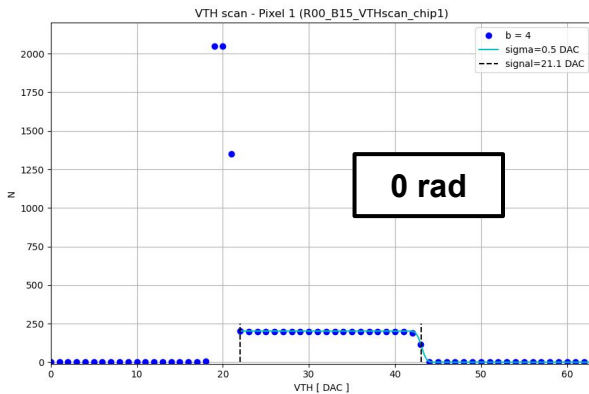
➤ No latchup events (from currents monitoring)

ALCOR TID - TDC response



TP phase scan (3600 → 1 clk cycle) at different TID → check TFine MIN, MAX, sigma, slope, IF, LSB

ALCOR TID - FE response

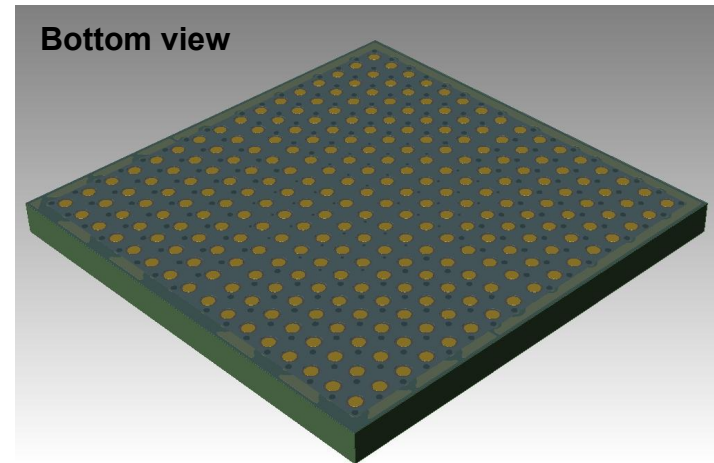
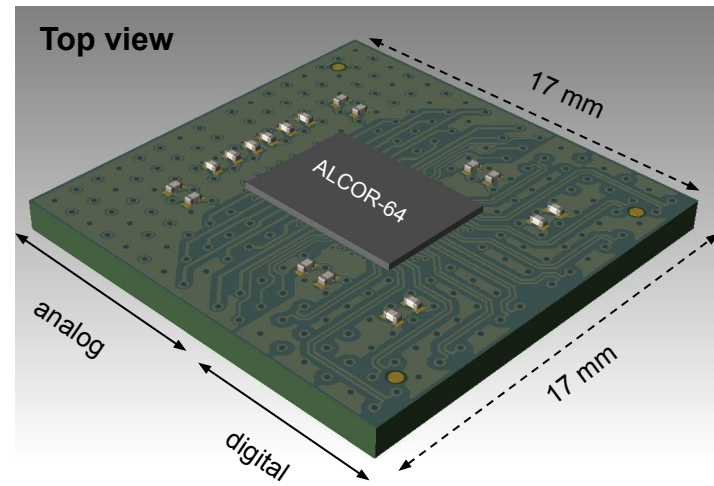
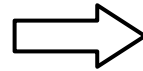
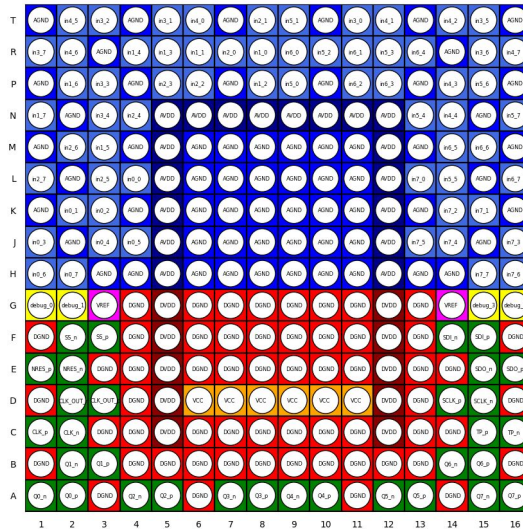


VTH scan (6-bit DAC) with internal TP at different TID → check baseline level, signal amplitude and sigma

ALCOR BGA package

BGA substrate designed by INFN Torino, package assembly done by external company

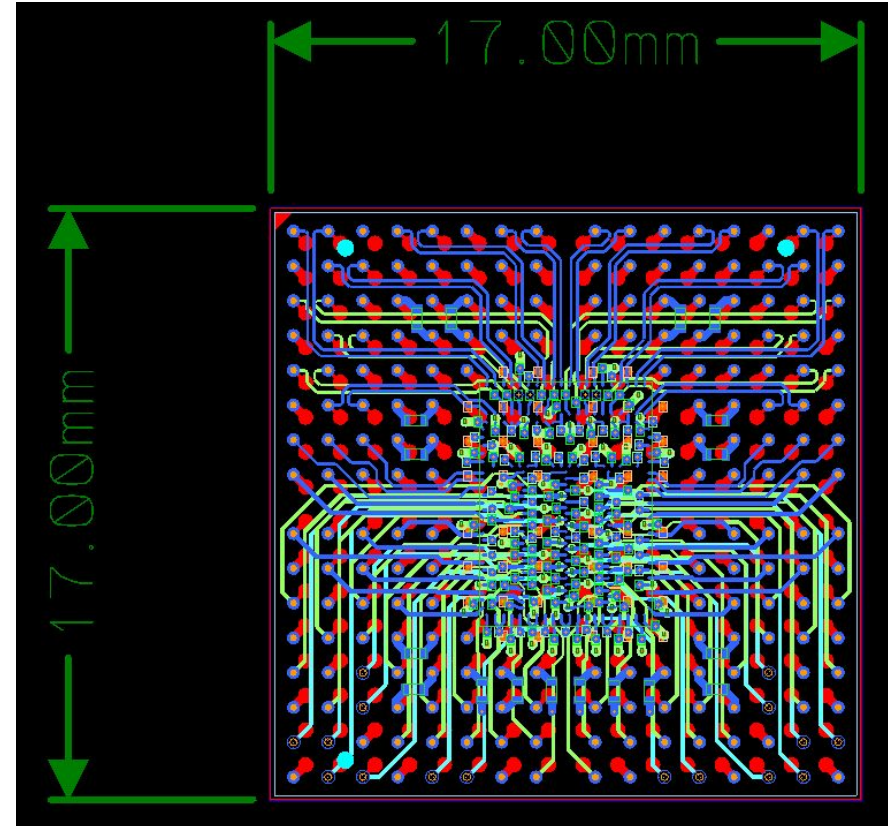
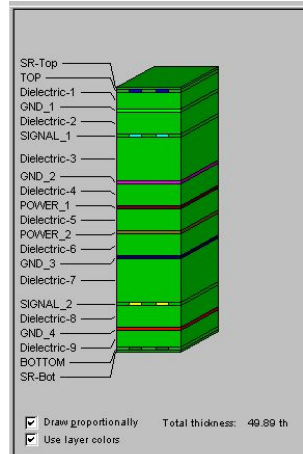
- Size: 17 x 17 mm²
- Balls number: 256 (16x16)
- Pitch: 1 mm



ALCOR BGA package

BGA substrate designed by INFN Torino, package assembly done by external company

- Size: 17 x 17 mm²
- Balls number: 256 (16x16)
- Pitch: 1 mm
- Material: Isola I-Tera MT40
- Number of layers = 10
- Total thickness = 1.27 mm



ALCOR v3 MPW run

25th Nov MPW run canceled by UMC

- We need to go to the first MPW shuttle of next year

UMC

Old schedule

MPW € MPW mini@sic € mini@sic

UMC MPW	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
UMC 28N Logic/Mixed-Mode – HPC		19		22			22	26	30	28		
UMC 40N Logic/Mixed-Mode – LP			11			24	29	26			18	
UMC 65N Logic/Mixed-Mode/RF – LL	2	26							2	21		
UMC L110AE Logic/Mixed-Mode/RF		26				3			2		25	
UMC L180 Logic GII, Mixed-Mode/RF			4					26				

UMC

New schedule

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Milestones

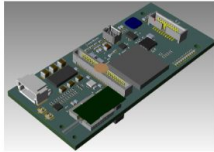
- ❑ Readiness at 75% of the final design of ALCOR v3 by September 2024
 - Top level integration and verification ongoing, ALCOR v3 will be ready for tapeout by this Fall
 - MPW run canceled by UMC, waiting for 2025 MPWs schedule from UMC and IMEC

- ❑ Completion of irradiation tests on ALCOR v2 and evaluation of SEU cross-section by July 2024
 - Preliminary results show good radiation tolerance for dRICH requirements
 - No effects from TID up to 200-300 krad
 - MTBF due to SEU more than adequate for dRICH operations

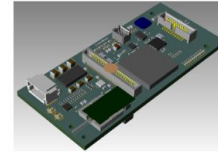
RDO update

See Davide's talk from last week ePIC Collaboration Meeting:

https://indico.bnl.gov/event/24127/contributions/94262/attachments/56082/95952/dRICH_RDO_25Jul2024.pdf



Status of the design and conclusions



- the schematic design of **dRICH RDO** is almost finished:
 - now performing the final checks and cross-checking the most critical parts:
 - clock distribution
 - remote programmability
- the desired placement is ready
- the PCB layout is going to start soon
- we plan to have the first prototypes ready by the end of 2024 and to do extensive debug (also the radiation tolerance will be tested)
- we are working on the firmware in the meanwhile