# The possible compensation idea of the "half entry chips"

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Our goal

- We have been encountered the half entry issues from the beginning of the INTT development.

- The goal of this study is to come up with the solution to restore the full entries using one of the slow control commands implemented to the FPHX chip.
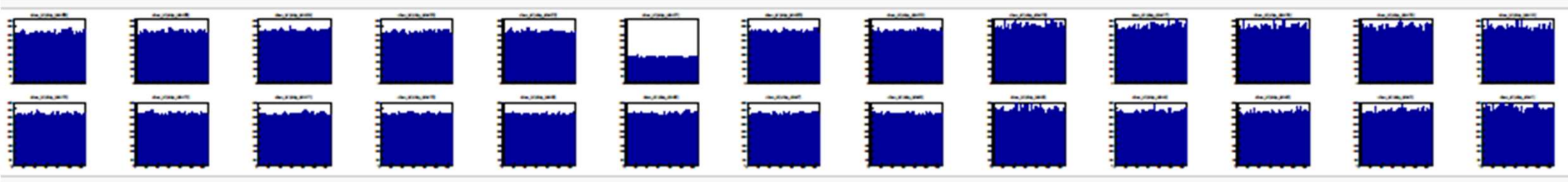
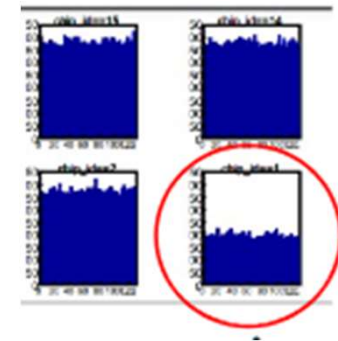* This data is for calibration mode

Definition of Two key symptoms(1)

・INTT half ladder has 26 chips and each chip contains 128channels

Definition of two symptoms play key roles in this study:

Half entry

-The number of detected signals is just half that of the other chip

Clonehit

-The same signal is received twice at the same time

Definition of Two key symptoms(2) <u>Clonehit</u>

-The same signal is received twice at the same time

```
*******************************************************************************
*    Row    *    adc.adc * ampl.ampl * chip_id.c * fpga_id.f * module.mo * chan_id.c * fem_id.fe *   bco.bco *
*******************************************************************************
  10044 *        1 *      44 *       13 *        0 *        8 *        0 *        4 *       55 *
  10045 *        1 *      44 *        4 *        0 *        8 *        0 *        4 *       55 *
  10046 *        3 *      44 *        5 *        0 *        8 *        0 *        4 *       55 *
  10047 *        3 *      44 *        6 *        0 *        8 *        0 *        4 *       55 *
  10048 *        2 *      44 *        7 *        0 *        8 *        0 *        4 *       55 *
  10049 *        2 *      44 *        8 *        0 *        8 *        0 *        4 *       55 *
ype <CR> to continue or q to quit ==>
  10050 *        1 *      44 *        9 *        0 *        8 *        0 *        4 *       55 *
  10051 *        0 *      44 *        1 *        0 *        8 *        0 *        4 *       55 *
  10052 *        0 *      44 *       10 *        0 *        8 *        0 *        4 *       55 *
  10053 *        2 *      44 *        2 *        0 *        8 *        0 *        4 *       55 *
  10054 *        2 *      44 *       11 *        0 *        8 *        0 *        4 *       55 *
  10055 *        3 *      44 *        3 *        0 *        8 *        0 *        4 *       55 *
  10056 *        1 *      44 *       12 *        0 *        8 *        0 *        4 *       55 *
  10057 *        2 *      44 *        7 *        0 *        8 *        0 *        4 *       55 *
  10058 *        2 *      44 *        8 *        0 *        8 *        0 *        4 *       55 *
  10059 *        0 *      44 *       10 *        0 *        8 *        0 *        4 *       55 *
  10060 *        2 *      44 *       11 *        0 *        8 *        0 *        4 *       55 *
  10061 *        0 *      44 *        1 *        0 *        8 *        0 *        4 *       55 *
```

Background：The origin of the half entry (1)

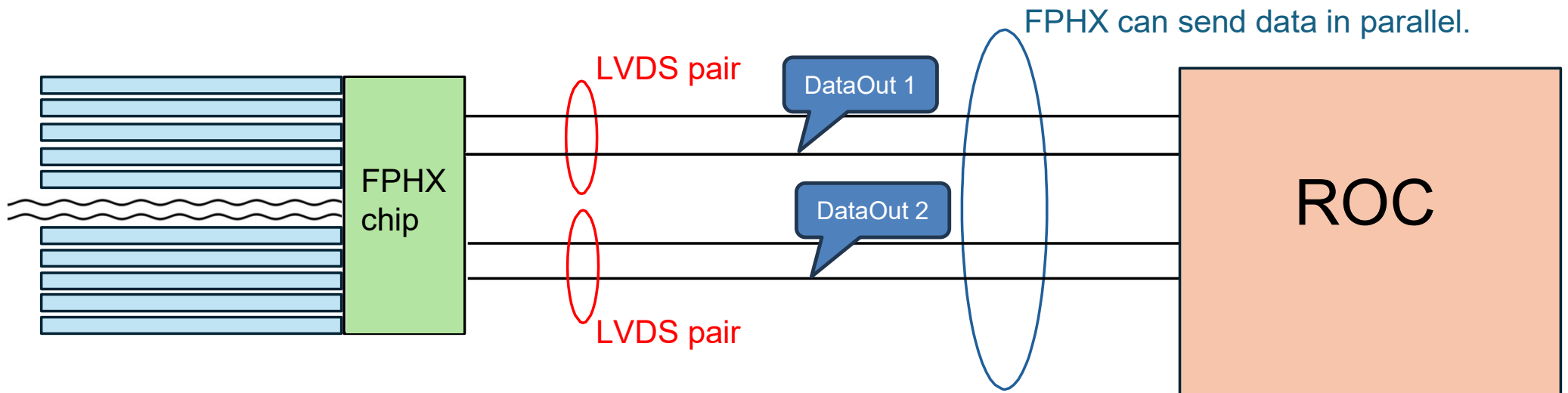- There are two sets of LVDS pair output data lines (DataOut1 and DataOut2) implemented in the FPHX chips
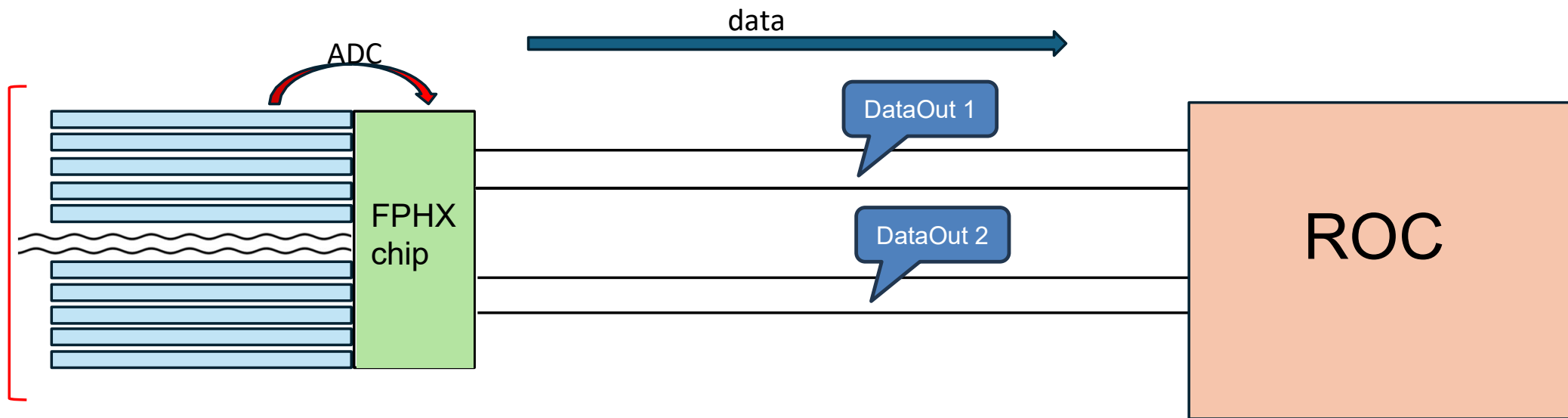
Reference：Kikuchi senpai

Background ： The origin of the half entry (2)

- Hits are sent out from alternating LVDS pairs
  between DataOut1 and DataOut2

FPHX can send data in parallel.

LVDS pair

DataOut 1

DataOut 2

LVDS pair

FPHX chip

ROC

Reference ： Kikuchi senpai

Background：The origin of the half entry (3)

- The half entry occurs when one of the output LVDS pairs is not functioning.
- There is a slow control function implemented which controls these output LVDS lines.
- Using this function, we explored if we can send all hits using only one DataOut line which is alive.
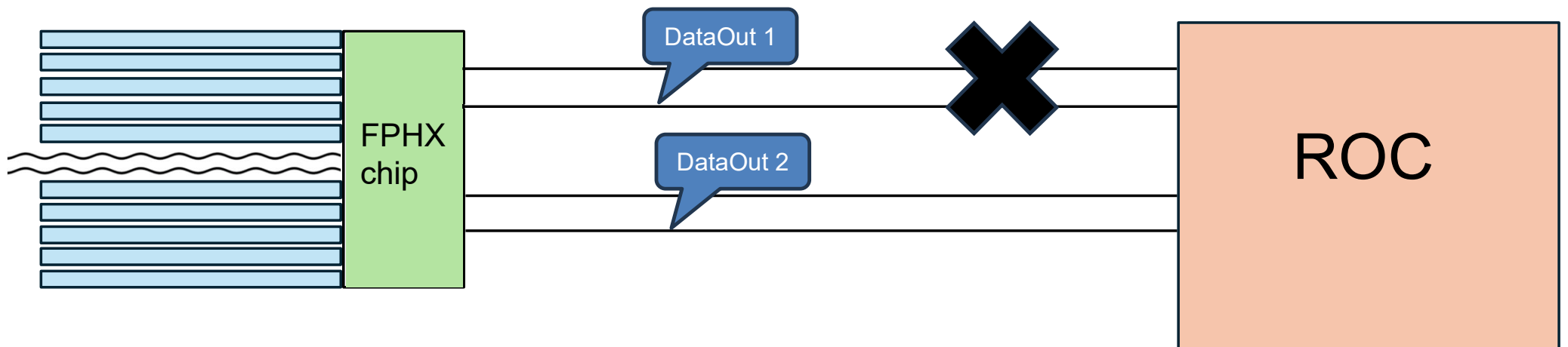
Background：Digital control

- This is the main topic in this measurement.

- When sending instructions to the FPHX chip, all communications are conducted using digital signals.

- Digital Control has four function. They can control using digital signals(Bit0~Bit3). For example,(0101,0100).

Digital Control Function

- Digital Control takes 4 bits parameters.

- The parameters which is involved in this study is bit-0 and bit-3.

- Since we don't know which DataOut line is not functioning, we need to vary parameters to find out which DataLine is alive.

The registers, their addresses and defaults are shown in .

Table 2 - Register Addresses and Defaults

Address	Name	Bits	Default	Notes
1	Mask	N/A	N/A	Set Command = Mask Channel Reset Command = Unmask Channel Data bits D6-D0 = Channel Address Data bit D7 = Global Command (i.e. Mask all channels or Unmask all channels)
2	Digital Control	7:0	1	Bit 0 = Active Serial Lines (1=Two, 0=One) Bit 1 = Accept (1=Accept Hits, 0=Reject) Bit 2 = Global Inject Enable Bit 3 = Serial Output Order
3	Vref	1:0	1	
4	Threshold DAC 0	7:0	8	
5	Threshold DAC 1	7:0	16	
6	Threshold DAC 2	7:0	32	
7	Threshold DAC 3	7:0	48	
8	Threshold DAC 4	7:0	80	
9	Threshold	7:0	112	

Digital Control : Bit0

- The default (Bit-0=1) function of Bit-0 : Hits in FIFO are sent out from alternating DataOut Lines.

SerialOut1 (DataOut1)   SerialOut2 (DataOut2)

Serializer 1   Serializer 2

FIFO Word 1	Out Word 1
FIFO Word 2	Out Word 2
FIFO Word 3	Out Word 1
FIFO Word 4	Out Word 2
FIFO Word 5	Out Word 1
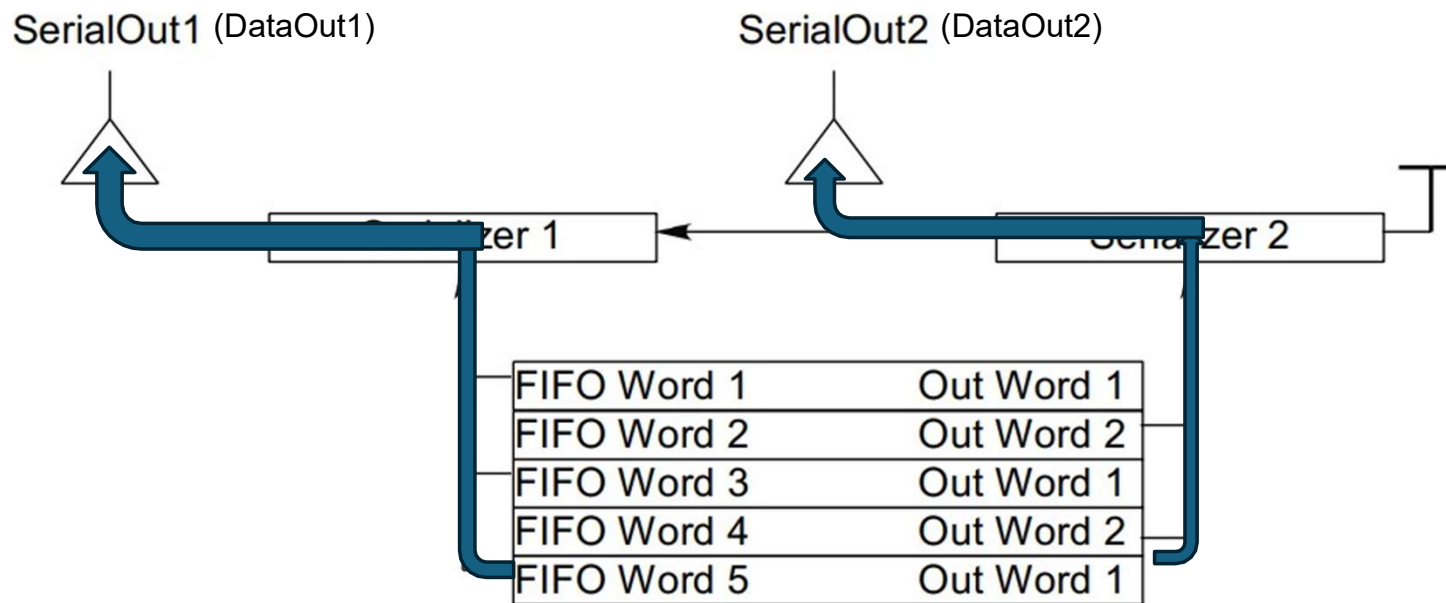
Figure 16 - The Serializers

Reference: https://wiki.sphenix.bnl.gov/images/5/5b/FPHXspecs_June2009Revision.pdf

Digital Control : Bit0

- Bit-0=0 sends copy (clone hits) to the another DataOut line as well as original one.

- The price we pay is the transmission speed, since this option double the traffic of one of DataOut line.

SerialOut1   SerialOut2

zer 1   Serializer 2

FIFO Word 1	Out Word 1
FIFO Word 2	Out Word 2
FIFO Word 3	Out Word 1
FIFO Word 4	Out Word 2
FIFO Word 5	Out Word 1
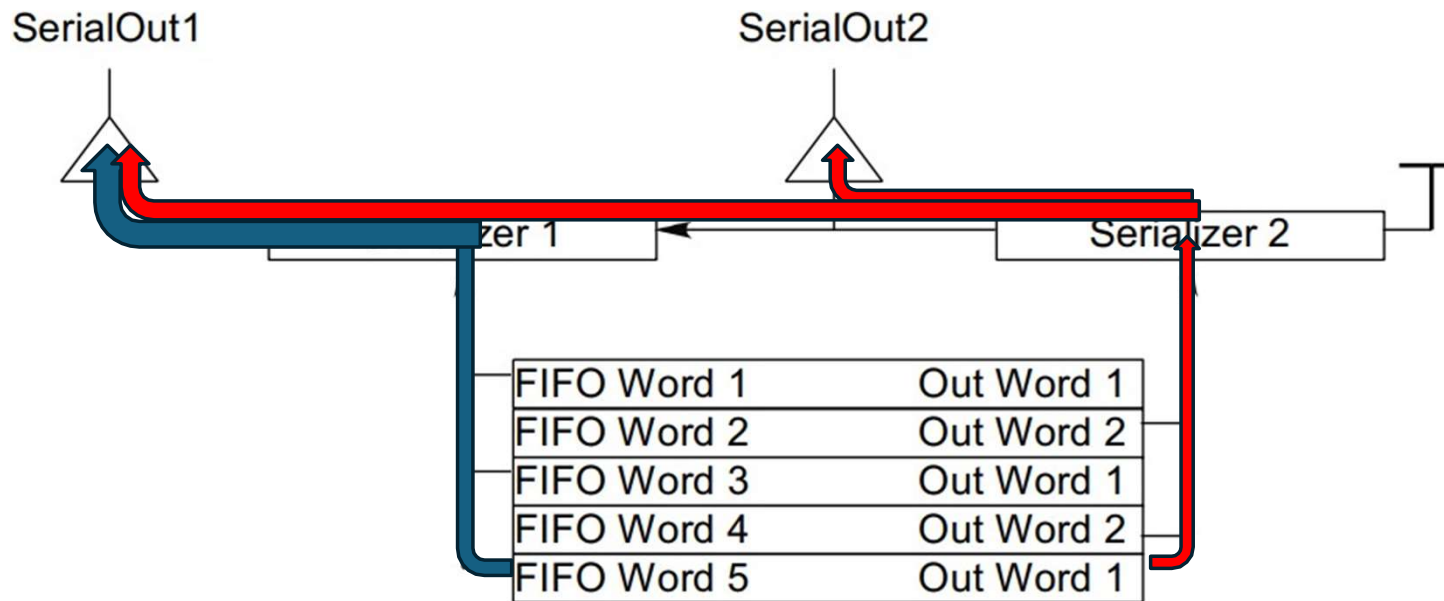
Figure 16 - The Serializers

Digital Control : Bit3

- Bit3 means "Serial Output Order".
- Bit-3 function depends on Bit-0 status
- Bit-3 controls which hit is to be cloned.
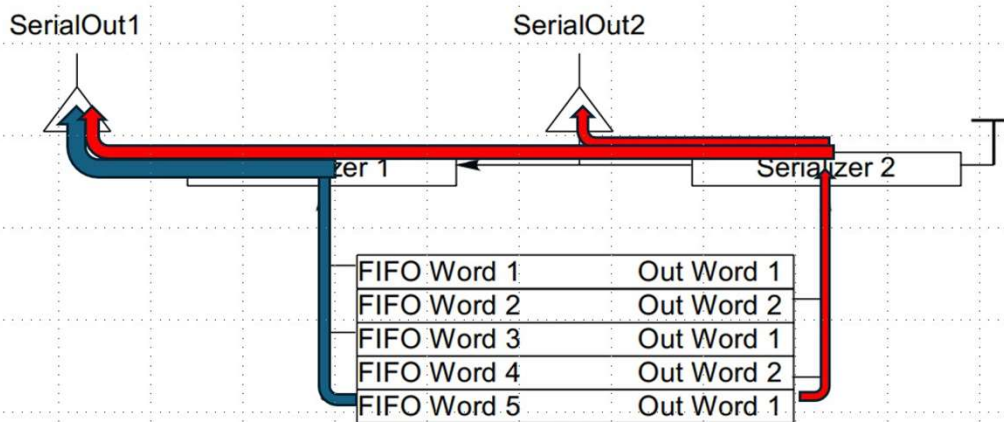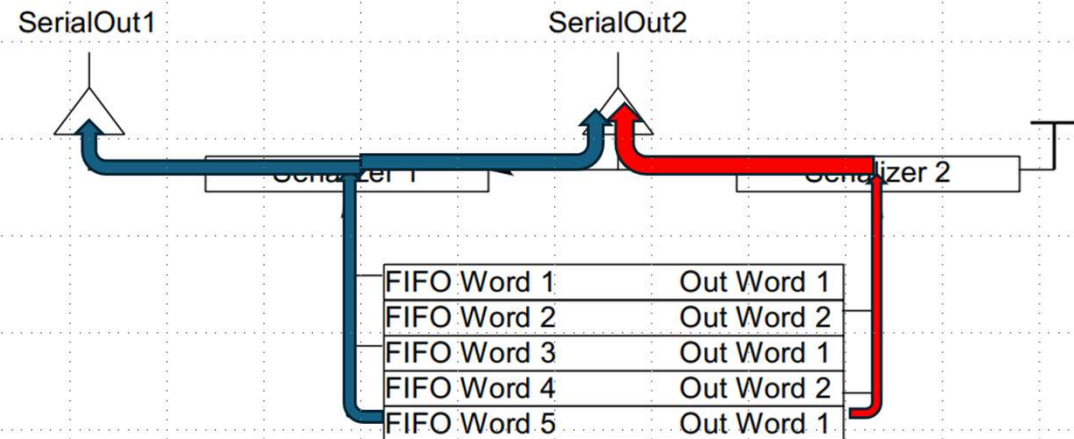
Figure 16 - The Serializers

Change of clone hits DataOut line by the Bit-3 parameter

Digital Control Function Test

- Following combinations of Bit-3 and Bit-0 parameters were tested to see if the response is as we expect.

- An artificially half entry chip was created for this test by shorting between a LVDS pair lines using the interception board only for chip=26.

- The common digital control parameters are applied for all chips in a half ladder and ran calibration.

	digital control			
	"0100"	"0101"	"1100"	"1101"
No short				
DataOut2 shorted				
DataOut1 shorted				

Digital Control Function Test : Result

Expected Response

😊 Successful to restore full entry

😢 Unsuccessful to restore full entry

	digital control			
	"0100"	"0101"	"1100"	"1101"
No short				
DataOut2 shorted	😊	😢	😢	😢
DataOut1 shorted	😢	😢	😊	😢

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	4	5	12	13
	digital	control		
	0100 V	0101	1100	1101
なし	1954	~~1450~~ 14506	1457	1523
1をショート	(1559)	1559	1601	1604	Chip_id 26
0をショート	~~1528~~	1541	(1544)	1546	Chip_id #ず26
1532

Bit 0 = 0
片方のデータが 両方のデータ転送
ラインから出力

Bit 3

イターセクションボード

1回目 1950   over15 → 1,2,5,16,17,18
2回目 1954   over 15 → 全部
3回目 1957   over 15 → 全部   ↓5
4回目 1523   over 15 → 1、14、18   ↓4
5回目 ~~1528~~ 1532 over15 → 26以外 26ハーフ
6回目 1541   over 15 → 5、15、16、18   26ハーフ
7回目 1544   over 15 → 26以外   26正常
8回目 1546   over 15 → 5、14、15、16、18 26ハーフ
9回目 1557   over 15 → 26以外   26ハーフ正常
10回目 1559   over 15 → 1、17、18   26ハーフ
11回目 1601   over 15 → 26以外   26ハーフ
12回目 1604   over 15 → 5、14、17、18 26ハーフ

Digital Control
: 0100 or 1100

- DataOut1 is shorted (disabled).
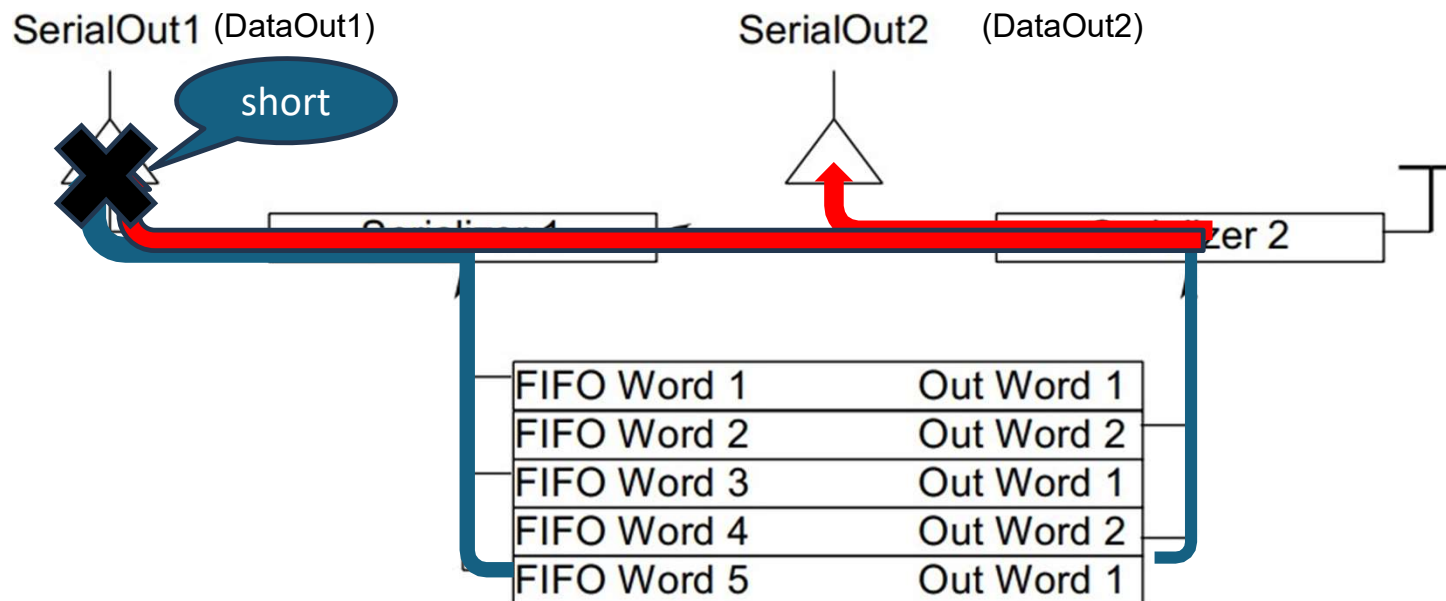- The result is expected to be half entry.

SerialOut1 (DataOut1)

short

SerialOut2 (DataOut2)

Serializer 1

Serializer 2

FIFO Word 1	Out Word 1
FIFO Word 2	Out Word 2
FIFO Word 3	Out Word 1
FIFO Word 4	Out Word 2
FIFO Word 5	Out Word 1

Figure 16 - The Serializers

Digital Control
: 0100 or 1100

- DataOut2 is shorted (disabled).
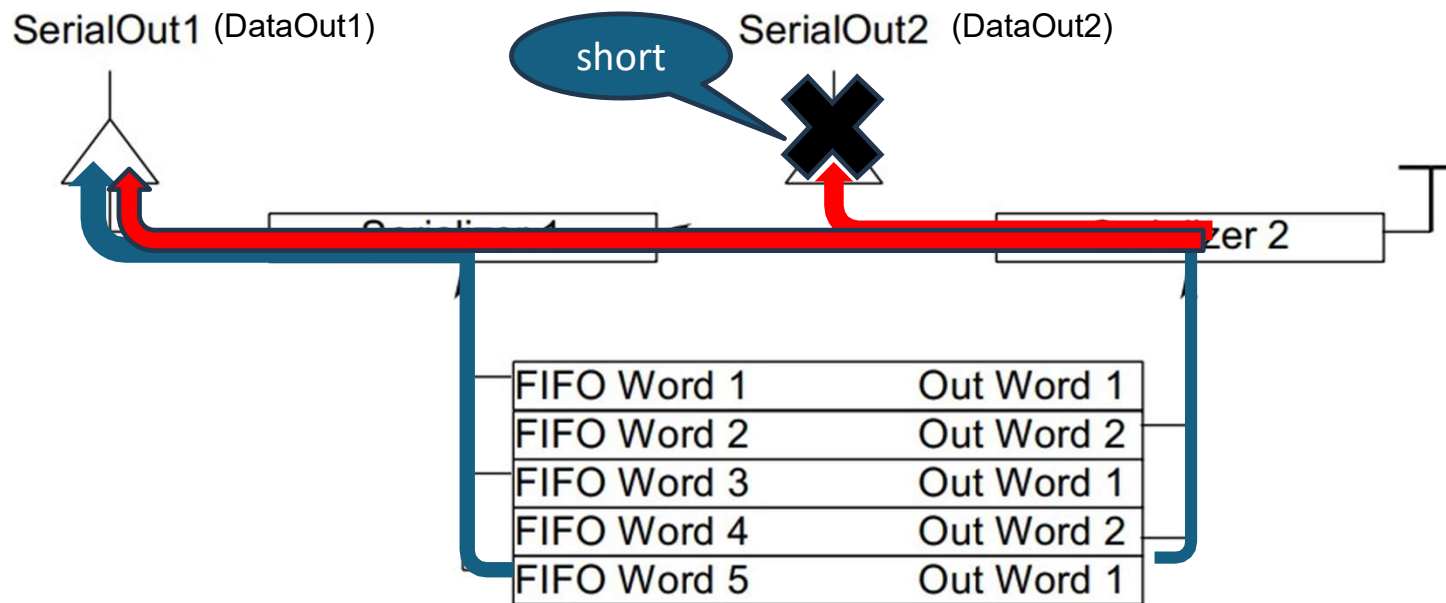- The result is expected to be full entry.
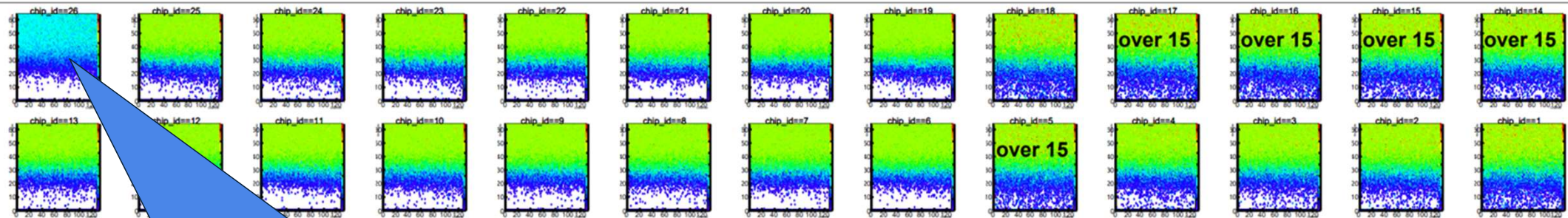

Figure 16 - The Serializers

Analysis

- Series of calibration data were analyzed for different digital control parameter combinations.

- If the value of adc and chip_id were equal among the same bco,we judged them as clone hits.
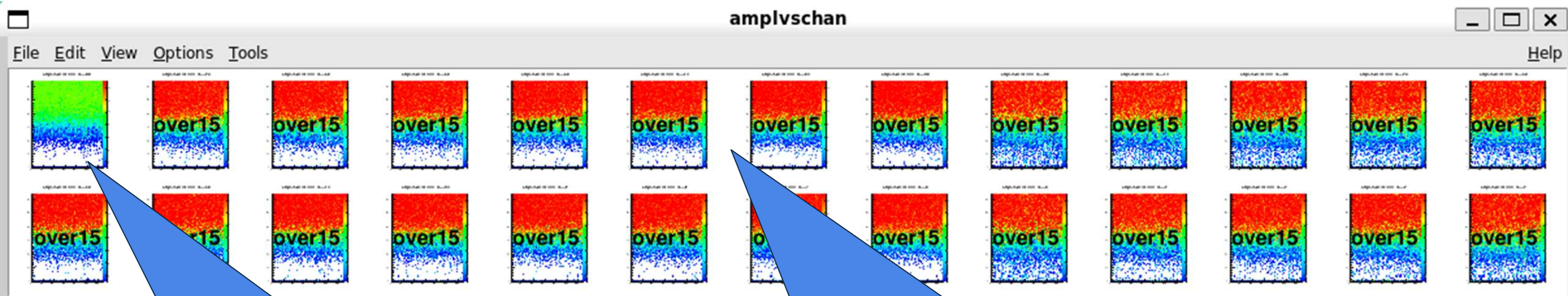
Run#1546
Digital Control Parameter = 1101(no clone hit)
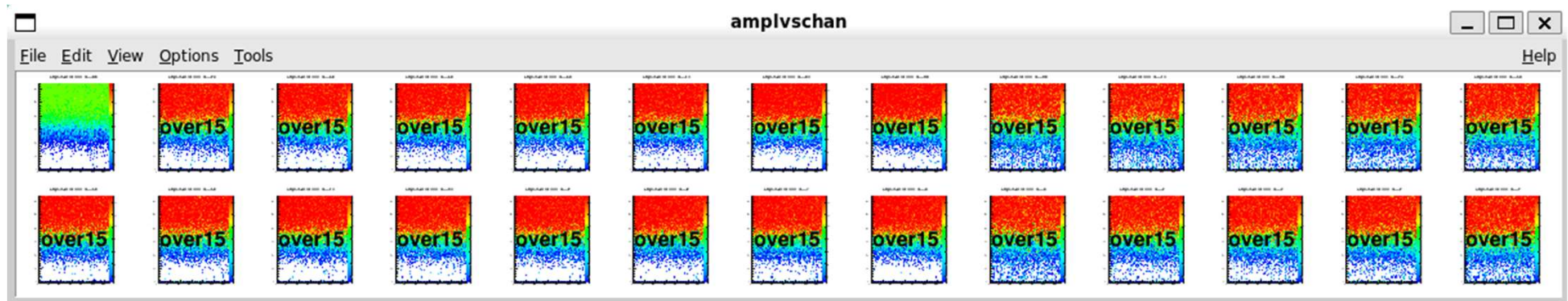
ampl vs channel data

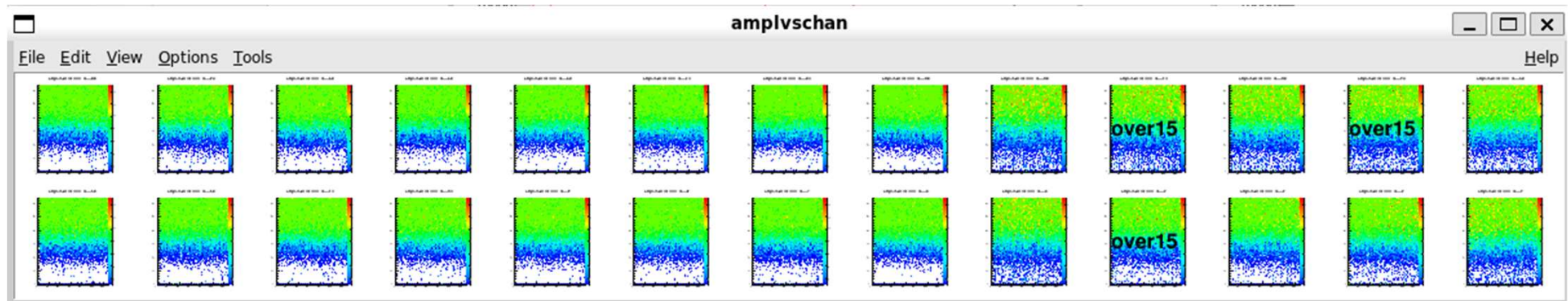Short chip#26

Run#1544 DC = 1100 Introduce clone hit

chip#26
restored full entry

chip#1~25
Extra entries for non-shorted chips

Run#1544 DC = 1100 remove clone hit

After removing clone hits in offline,
the entries become normal for non-shorted chips

Clone hit removal of non-shorted chips

- The red raw histogram accumulated 150% of normal calibration entries except for chip#26 as expected

- After removing clone hits from chip#1~25, the entry becomes normal as consistent with chip#26.

- Excess of the data in un-shorted ones are perfectly explained by the clone hits.

- For those of chips that the DataOut2 is not functioning, DC=1101 will restore the full entry
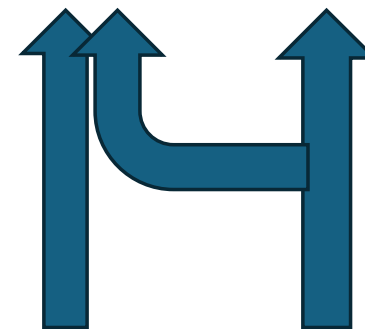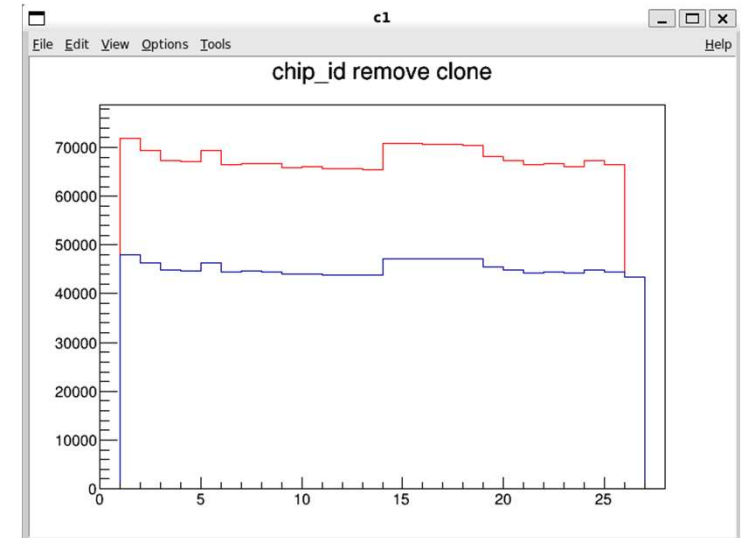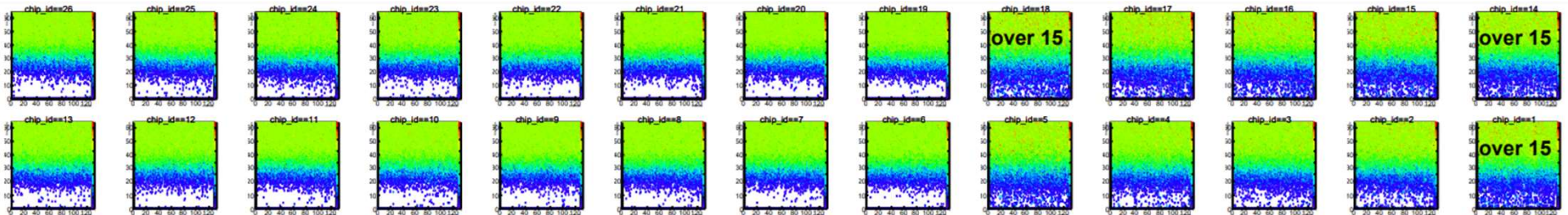

chip_id=26
right side ×
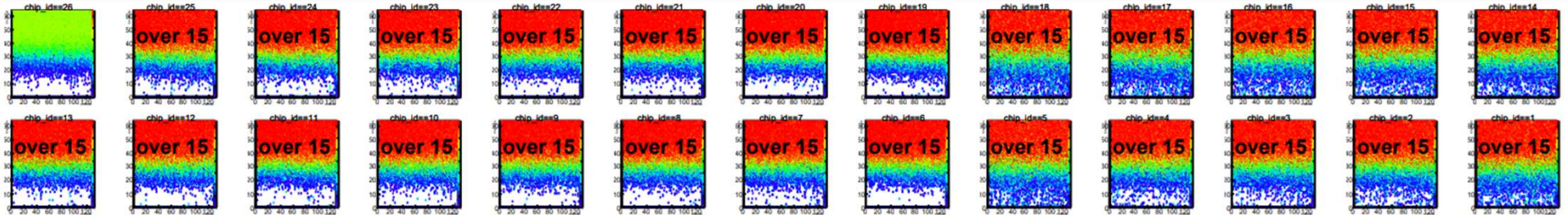
Run#1544(DC=1100)
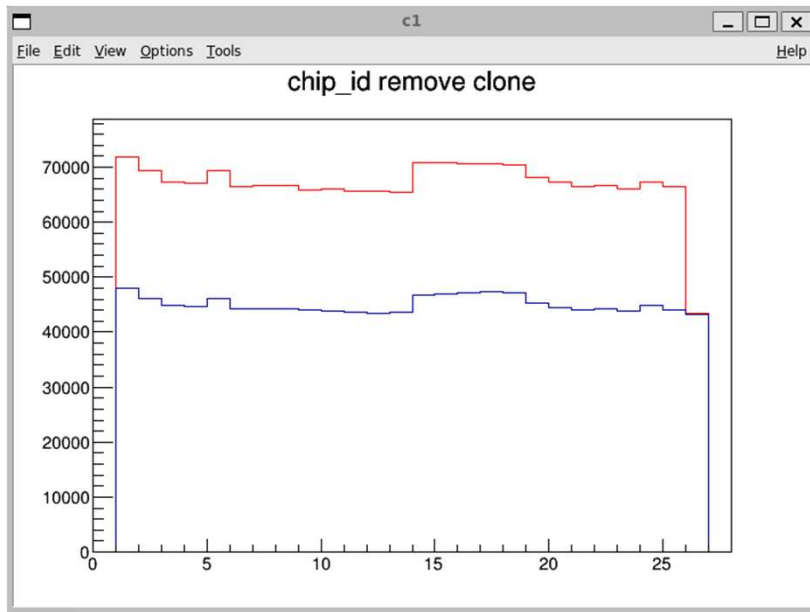

Run#1523(DC=1101)

No copy hits. No short.
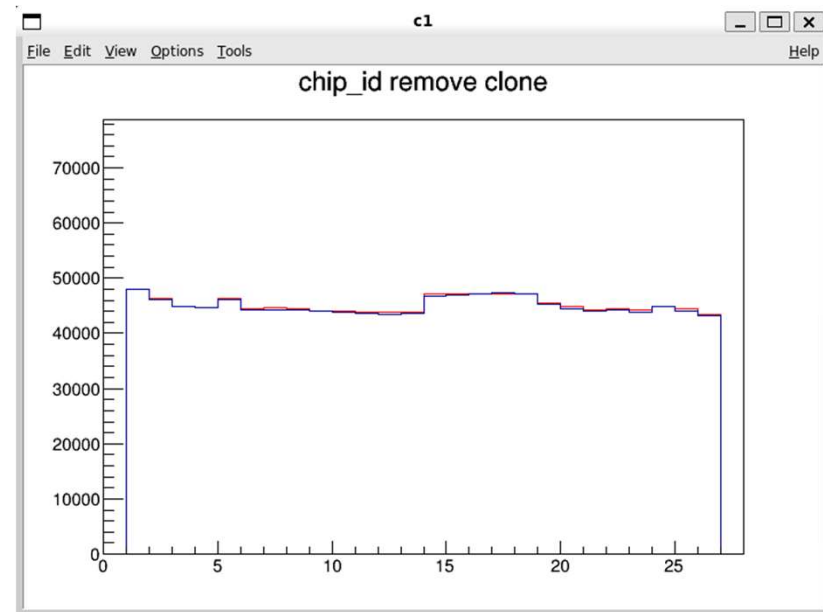Swap priority between DataOut1 and DataOut2 (effectively normal calibration run)

Bit0 difference

Red:1544(DC1100)
Blue:1523(DC1101)

Red:1544(DC1100)remove clone
Blue:1523(DC1101)

After removing clone hits, the entries of the normal calibration run are almost perfectly reproduced even with copy hits mode.

Conclusion

- We have tested if a half entry can be recovered by applying relevant Digital Control parameters.

- The result was positive. We found the relevant DC parameters to restore fuu events for each of non-funtioning Dataout1 and Dataout2, respectively.

- The parameter combinations has to be examined in order to restore half entries in the INTT barrels since which Dataout Line is not functioning is not known.

- The mechanism to create clone hits in FPHX is identified for the first time. Existing clone hits can be originated from leaking in the copy line due to the malfunction of FPHX

Future analysis

- Repeat testing with real half entry chip (not artificially made one) to rehearsal actual procedure in 1008.

- Test Reproducibility.

- Consider any way to test the rate effect

- For clone hits, we are planning following studies to verify if the origin of existing clone hits is indeed malfunction of "copy hit" circuit in FPHX

  - Check the reproducibility (frequency, specific channel, etc) of clone hits from a given chip.

  - If the reproducibility is good, we verify these clone hits are neither port nor ROC origin by swapping ladders, ports, columns

Acknowledgement (please, Nakagawa…..)

- The attention on the digital control function was initiated by **Cheng-Wei** to study if we can use this function to disable noisy channel.

- Back then, we didn't know well how the digital control functions (we even misunderstood from the FPHX manual.)

- **Takahiro** executed testing DC parameters and he discovered "copying" function of the digital control.

- Although we couldn't figure out to be valid for original motivation though, we found it is useful to recover the half entry.