

LFHCAL (+EEEMC) Test Beam August/September 2024

Oskar Hartbrich

(for the whole testbeam crew and everyone involved)



ORNL is managed by UT-Battelle LLC for the US Department of Energy



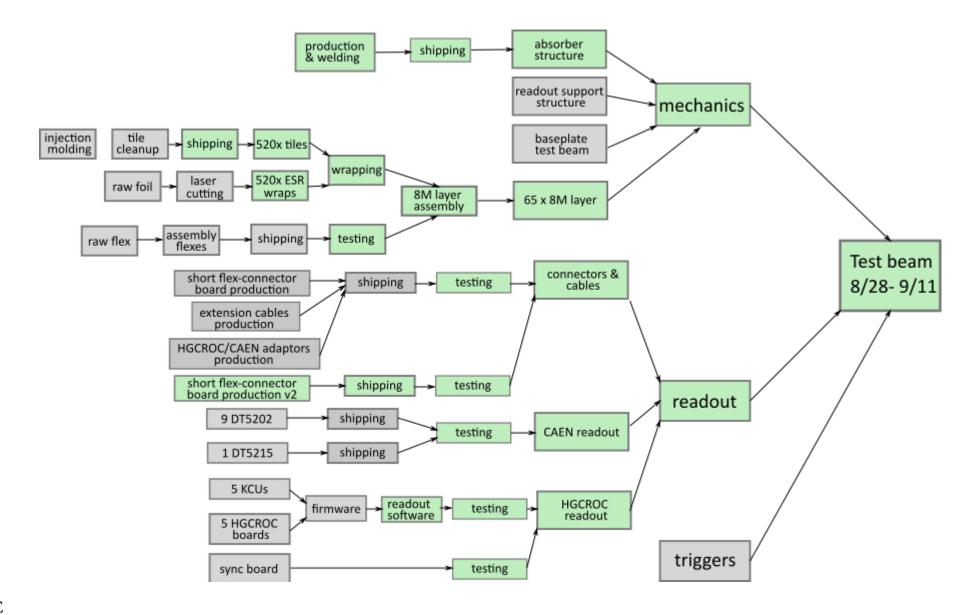
LFHCAL Prototype: The Plan

- First full LFHCAL module: 64 layers
 - 20cm*10cm
 - 512 readout channels
 - +parasitic EEEMC module testing

- Two continuous weeks of beam time at CERN PS.
- August 28-September 11
- First week: HGCROC Readout
- Second week: CAEN DT5202+DT5215 Readout

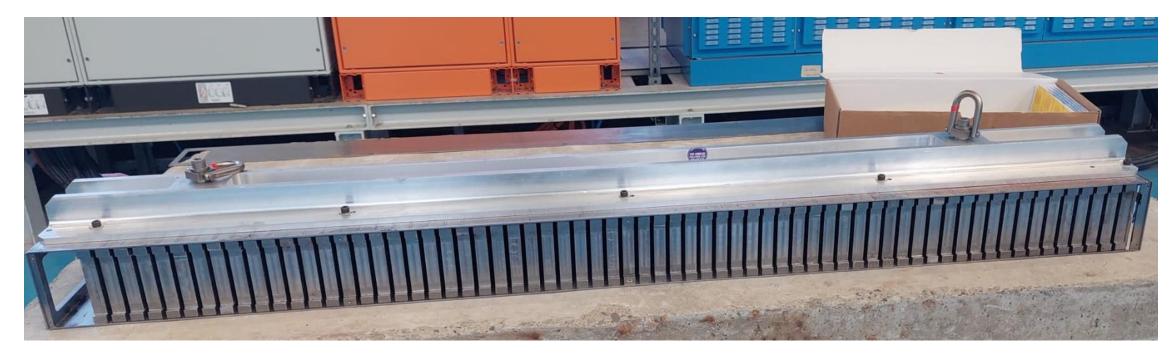


LFHCAL Prototype: Status at LeHigh Meeting



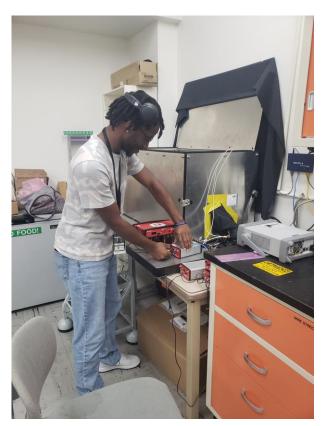
LFHCAL Prototype: Mechanics

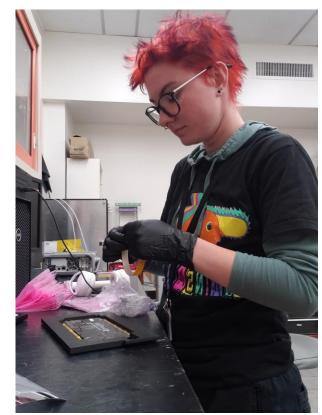
- First mechanics module available since August
 - E-beam welded in CA, shipped to ORNL for compliance testing
 - Shipped to CERN few weeks in advance

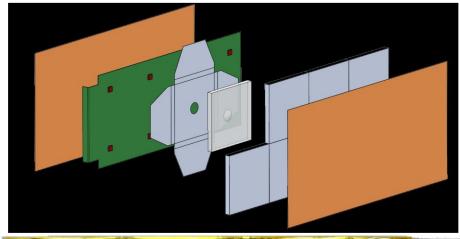


LFHCAL Prototype: Scintillator Layers

- All tiles available at ORNL (produced by FNAL, cleaned by Valpo)
- ORNL summer interns Droc and Hagen (both UTK) assembled and tested 74 scintillator layers





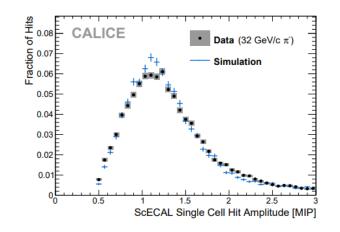


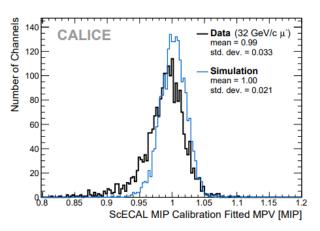


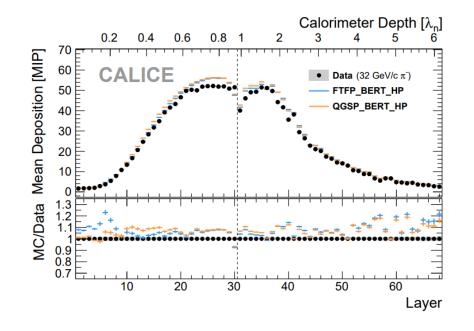


LFHCAL Prototype: Goals

- Expose LFHCAL module to muons, electrons, pions in energy range 1-10GeV
- Muons: Cell-by-cell MIP calibration
- Electrons: Response, resolution
 - Single cell hit spectra, SiPM saturation effects
 - + Geant4 comparison
- Pions: no chance to laterally contain pion showers
 - Longitudinal shower profiles, hit spectra
 - + Geant4 comparisons
- Publish in NIM/JINST:
 - Single paper?: construction, beam analysis?
 - Two papers?: construction, lab tests, 2023 beam + 2024 beam



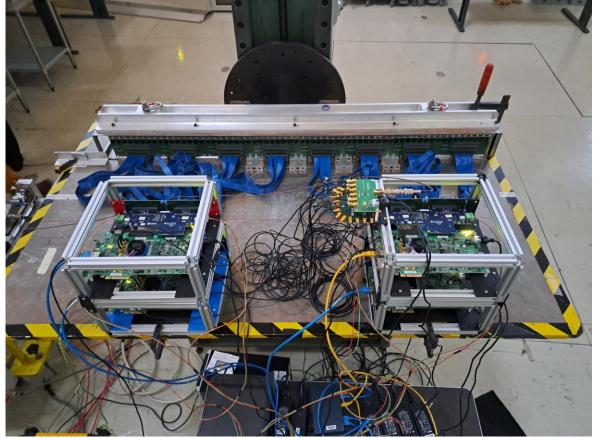






Initial Setup





HGCROC Run Summary

- Setup without major issues
- First useful runs within hours of setup
 - Some calibrations etc. needed of course
- Trigger rates very very low (single digit events per spill)
 - Ultimately traced down to misconfigured FOCAL trigger board
- Still acquired full dataset:
 - Muons, electrons 1GeV-5GeV, hadrons (+-) 3-15GeV
- There will be a dedicated talk on HGCROC experience soon™



Live Data Monitoring

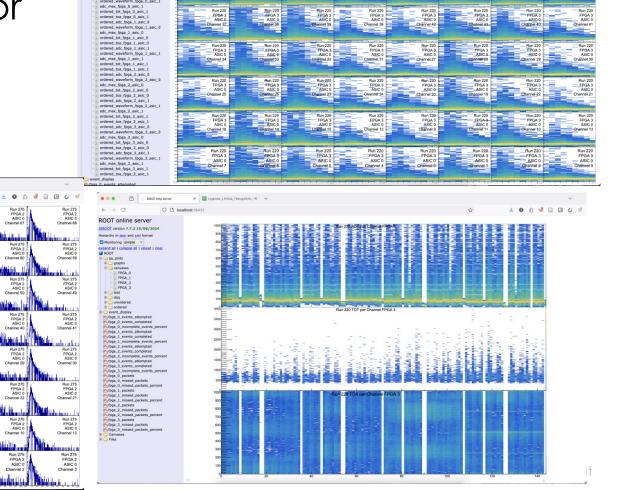
ROOT online server

FPGA_1 FPGA_2 FPGA_3

FPGA 3 Events FPGA_1_Packets
FPGA_2_Packets
FPGA_3_Packets
FPGA_3_Packets

ordered_adc_fpga_0_asic_0 ordered_waveform_fpga_0_asic_0 adc_max_fpga_0_asic_0 adc_max_fpga_0_asic_0
ordered_tot_fpga_0_asic_0
ordered_toa_fpga_0_asic_0
ordered_adc_fpga_0_asic_1
ordered_waveform_fpga_0_asic_
adc_max_fpga_0_asic_1 ordered_tot_fpga_0_asic_1
ordered_tot_fpga_0_asic_1
ordered_tos_fpga_0_asic_0
ordered_adc_fpga_1_asic_0
ordered_waveform_fpga_1_asic_0
adc_max_fpga_1_asic_0 ordered tot foga 1 asic 0 ordered_tot_pga_1_asic_0
ordered_toa_fpga_1_asic_0
ordered_adc_fpga_1_asic_1
ordered_waveform_fpga_1_asic_
adc_max_fpga_1_asic_1
ordered_tot_fpga_1_asic_1 ordered_toa_fpga_1_asic_1 ordered_adc_fpga_2_asic_0
ordered_waveform_fpga_2_asic_0
adc_max_fpga_2_asic_0
ordered_tot_fpga_2_asic_0

- Tristan Protzmann (LeHigh) developed live data monitor for HGCROC (+CAEN) data
 - Available to everyone interested



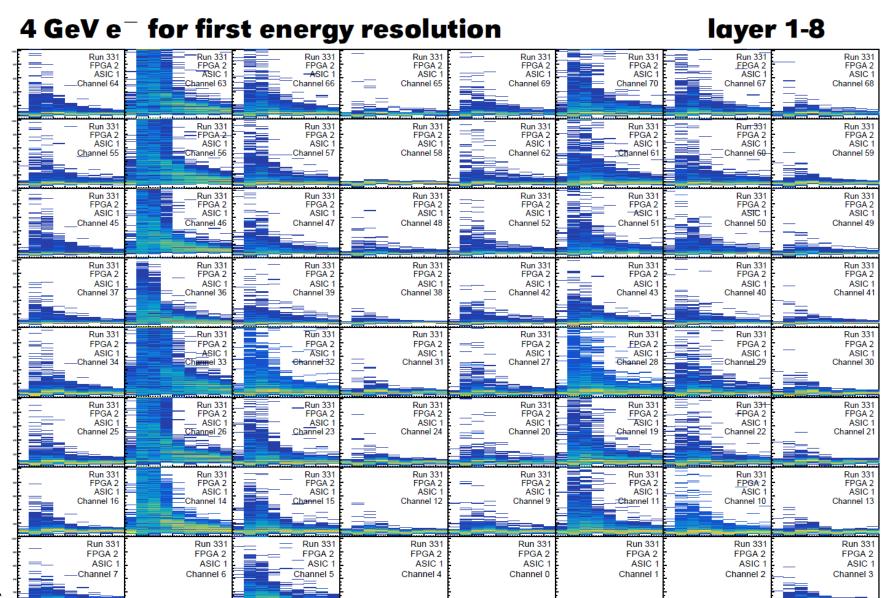
ROOT version 7.7.2 19/06/202

ordered_waveform_fpga_0_asic_i adc max foga 0 asic 0 ordered_tot_fpga_0_asic_0 ordered_toa_fpga_0_asic_0 ordered_toa_fpga_0_asic_1

ordered_waveform_fpga_0_asic_



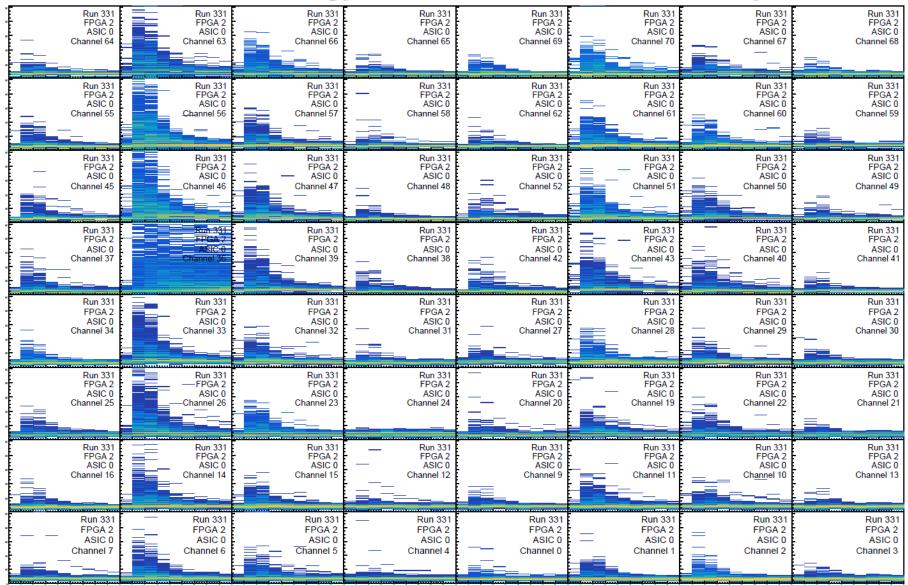
4 GeV e⁻ in HGCROC LFHCAL: Layer 1-8



4 GeV e⁻ in HGCROC LFHCAL: Layer 9-16

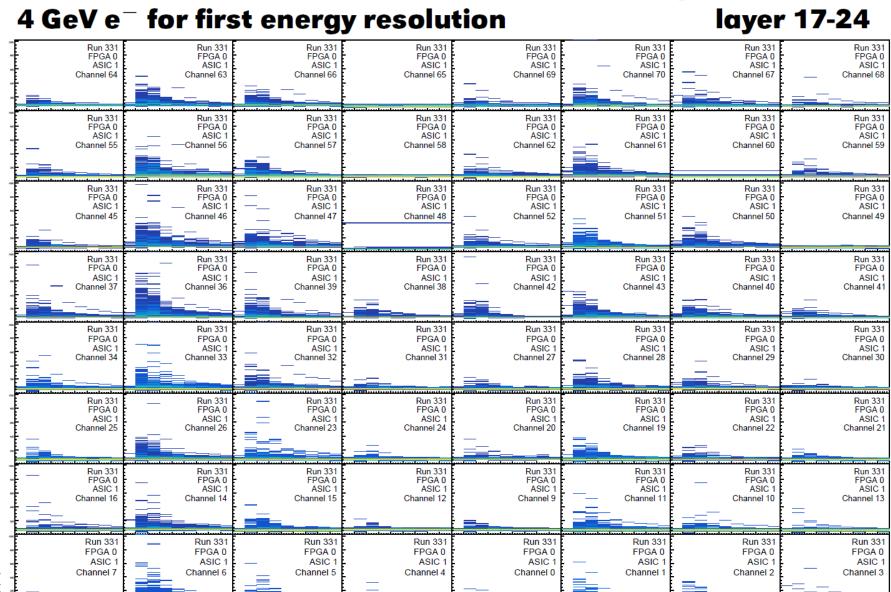
4 GeV e⁻ for first energy resolution

layer 9-16





4 GeV e⁻ in HGCROC LFHCAL: Layer 17-24



4 GeV e⁻ in HGCROC LFHCAL: Layer 25-32

4 GeV e⁻ for first energy resolution

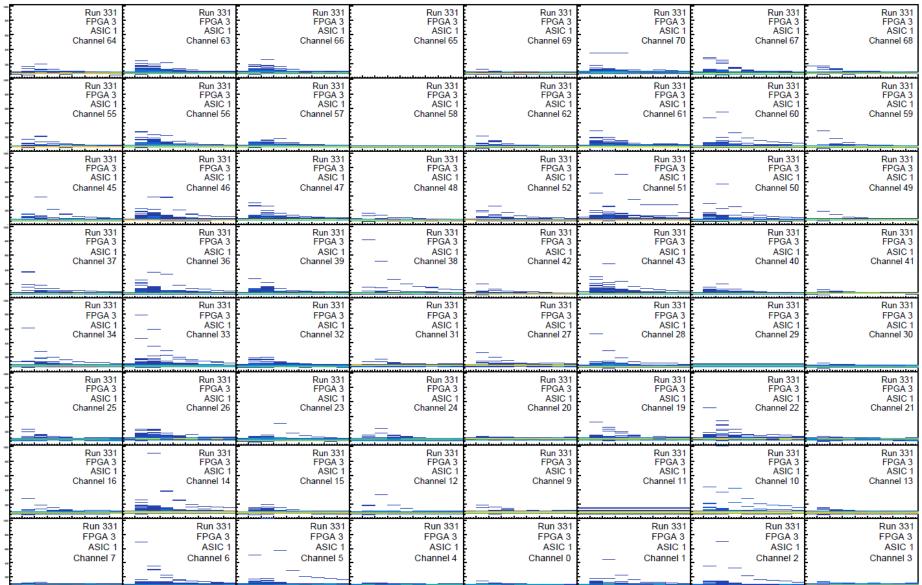
layer 25-32



4 GeV e⁻ in HGCROC LFHCAL: Layer 33-40

4 GeV e⁻ for first energy resolution

layer 33-40



4 GeV e⁻ in HGCROC LFHCAL: Layer 41-48

4 GeV e⁻ for first energy resolution

layer 41-48

Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331
FPGA 3	FPGA 3	FPGA 3	FPGA 3	FPGA 3	FPGA 3	FPGA 3	FPGA 3
ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0
Channel 64	Channel 63	Channel 66	Channel 65	Channel 69	Channel 70	Channel 67	Channel 68
Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331
FPGA 3	FPGA 3	FPGA 3	FPGA 3	FPGA 3	FPGA 3	FPGA 3	FPGA 3
ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0
Channel 55	Channel 56	— Channel 57	Channel 58	Channel 62	Channel 61	Channel 60	Channel 59
Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331
FPGA 3	FPGA 3	FPGA 3	FPGA 3	FPGA 3	FPGA 3	FPGA 3	FPGA 3
ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0
Channel 45	Channel 46	— Channel 47	Channel 48	Channel 52	Channel 51	Channel 50	Channel 49
Run 331 FPGA 3 ASIC 0 Channel 37	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331
	FPGA 3	FPGA 3	FPGA 3	FPGA 3	FPGA 3	FPGA 3	FPGA 3
	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0
	Channel 36	Channel 39	Channel 38	Channel 42	Channel 43	Channel 40	Channel 41
Run 331 FPGA 3 ASIC 0 Channel 34	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331
	FPGA 3	FPGA 3	FPGA 3	FPGA 3	FPGA 3	FPGA 3	FPGA 3
	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0
	Channel 33	Channel 32	Channel 31	Channel 27	Channel 28	Channel 29	Channel 30
Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331
FPGA 3	FPGA 3	FPGA 3	FPGA 3	FPGA 3	FPGA 3	FPGA 3	FPGA 3
ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	— ASIC 0
Channel 25	Channel 26	Channel 23	Channel 24	Channel 20	Channel 19	Channel 22	Channel 21
Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331
FPGA 3	FPGA 3	FPGA 3	FPGA 3	FPGA 3	FPGA 3	FPGA 3	FPGA 3
ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0
Channel 16	Channel 14	Channel 15	Channel 12	Channel 9	Channel 11	Channel 10	Channel 13
Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331
FPGA 3	FPGA 3	FPGA 3	FPGA 3	FPGA 3	FPGA 3	FPGA 3	FPGA 3
ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0
Channel 7	Channel 6	Channel 5	Channel 4	Channel 0	Channel 1	Channel 2	Channel 3

4 GeV e⁻ in HGCROC LFHCAL: Layer 49-56

4 GeV e⁻ for first energy resolution

layer 49-56

Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331
FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1
ASIC 1	ASIC 1	ASIC 1	ASIC 1	ASIC 1	ASIC 1	ASIC 1	ASIC 1
Channel 64	Channel 63	Channel 66	Channel 65	Channel 69	Channel 70	Channel 67	Channel 68
Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331
FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1
ASIC 1	ASIC 1	ASIC 1	ASIC 1	ASIC 1	ASIC 1	ASIC 1	ASIC 1
Channel 55	Channel 56	Channel 57	Channel 58	Channel 62	Channel 61	Channel 60	Channel 59
Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	ASIC 1
FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	
ASIC 1	ASIC 1	ASIC 1	ASIC 1	ASIC 1	ASIC 1	ASIC 1	
Channel 45	Channel 46	Channel 47	Channel 48	Channel 52	Channel 51	Channel 50	
Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331
FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1
ASIC 1	ASIC 1	ASIC 1	ASIC 1	ASIC 1	ASIC 1	ASIC 1	ASIC 1
Channel 37	Channel 36	Channel 39	Channel 38	Channel 42	Channel 43	Channel 40	Channel 41
Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331
FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1
ASIC 1	ASIC 1	ASIC 1	ASIC 1	ASIC 1	ASIC 1	ASIC 1	ASIC 1
Channel 34	Channel 33	Channel 32	Channel 31	Channel 27	Channel 28	Channel 29	Channel 30
Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	ASIC 1
FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	
ASIC 1	ASIC 1	ASIC 1	ASIC 1	ASIC 1	ASIC 1	ASIC 1	
Channel 25	Channel 26	Channel 23	Channel 24	Channel 20	Channel 19	Channel 22	
Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331
FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1
ASIC 1	ASIC 1	ASIC 1	ASIC 1	ASIC 1	ASIC 1	ASIC 1	ASIC 1
Channel 16	Channel 14	Channel 15	Channel 12	Channel 9	Channel 11	Channel 10	Channel 13
Run 331 FPGA 1 ASIC 1 Channel 7	Run 331 FPGA 1 ASIC 1 Channel 6	Run 331 FPGA 1 — ASIC 1 Channel 5 — —	Run 331 FPGA 1 ASIC 1 Channel 4	Run 331 FPGA 1 ASIC 1 Channel 0	Run 331 FPGA 1 ASIC 1 Channel 1	Run 331 FPGA 1 ASIC 1 Channel 2	ASIC 1

4 GeV e⁻ in HGCROC LFHCAL: Layer 57-64

4 GeV e⁻ for first energy resolution

layer 57-64

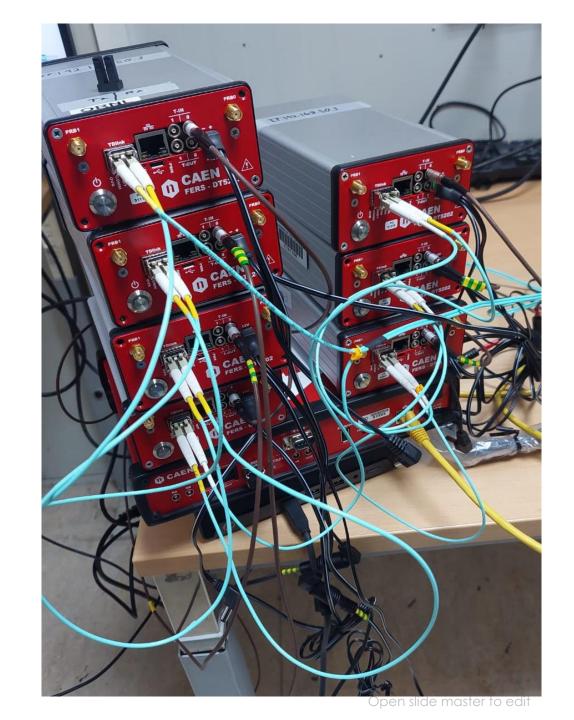
Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 33
FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA
ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC
Channel 64	Channel 63	Channel 66	Channel 65	Channel 69	Channel 70	Channel 67	Channel 6
Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 33
FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA
ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC
Channel 55	Channel 56	Channel 57	Channel 58	Channel 62	Channel 61	Channel 60	Channel 5
Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 33
FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA
ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC
Channel 45	Channel 46	Channel 47	Channel 48	Channel 52	Channel 51	Channel 50	Channel 4
Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 33
FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA
ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC
Channel 37	Channel 36	Channel 39	Channel 38	Channel 42	Channel 43	Channel 40	Channel 4
Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 3
FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA
ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC
Channel 34	Channel 33	Channel 32	Channel 31	Channel 27	Channel 28	Channel 29	Channel :
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Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 33
FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA
ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC
Channel 25	Channel 26	Channel 23	Channel 24	Channel 20	Channel 19	Channel 22	Channel 2
Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 33
FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA
ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC
Channel 16	Channel 14	Channel 15	Channel 12	Channel 9	Channel 11	Channel 10	Channel 1
Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 331	Run 33
FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA 1	FPGA
ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC 0	ASIC
Channel 7	Channel 6	Channel 5	Channel 4	Channel 0	Channel 1	Channel 2	Channel

The CAEN Saga pt1

- 8 DT5202 readout units + 1 DT5215 data concentrator
 - Using several loaned DT5202s from all over the world
 - Readout PC <-> single ethernet <-> DT5215 <-> "TDLink" fibers to DT5202
- Cabled up everything: pedestals good
 - No grounding issues, no ground lift to flex boards necessary (PS testbeam is cleaner environment than ORNL lab)
- However: no signal whatsoever.



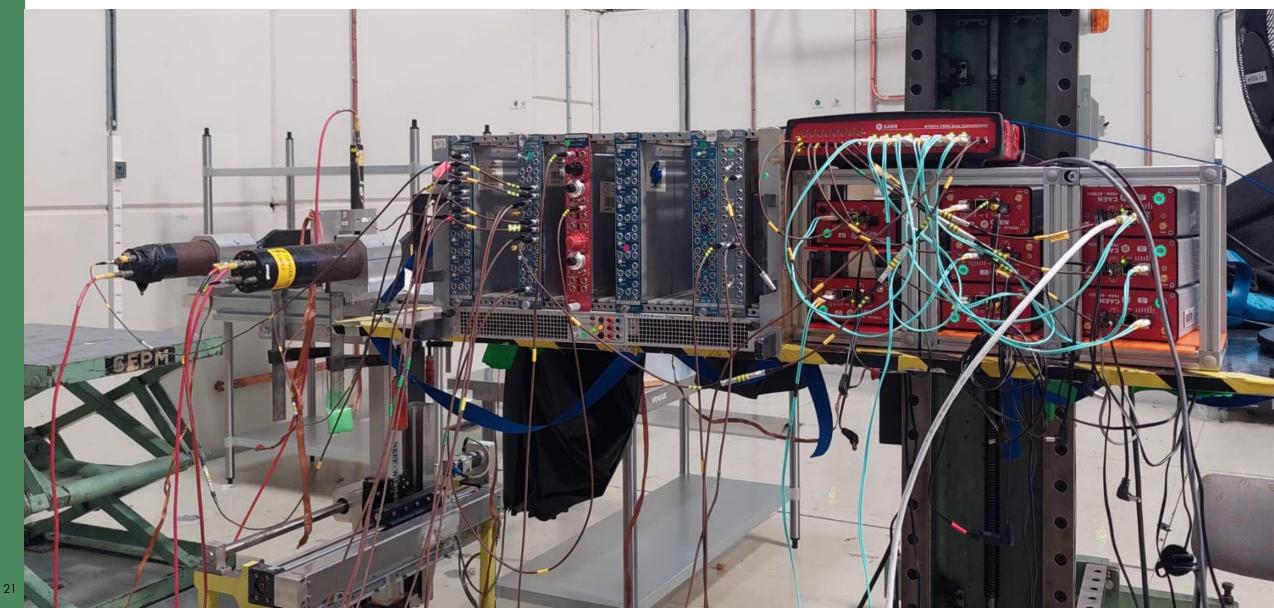
The CAEN Saga pt1

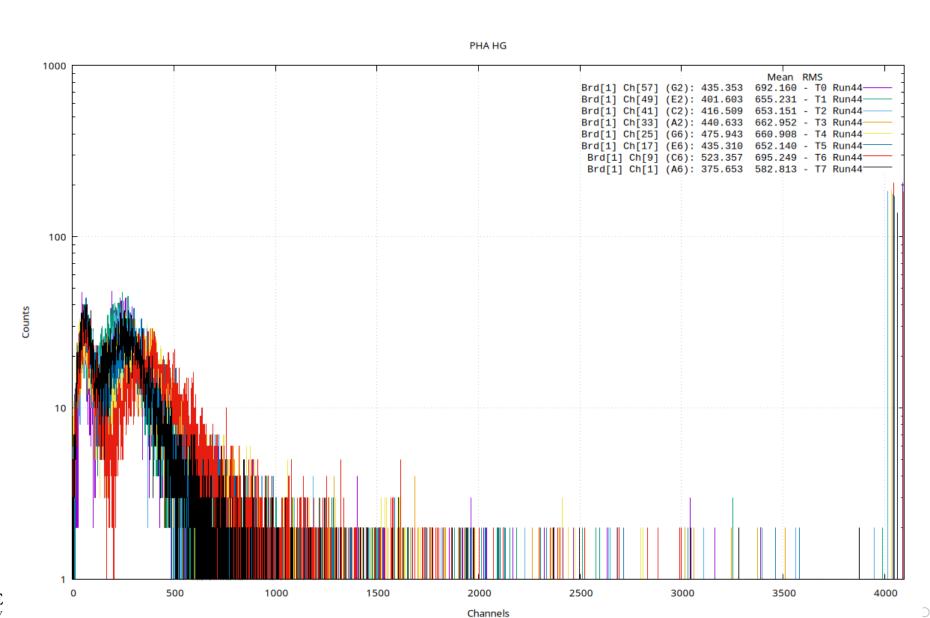


The CAEN Saga pt2: Fighting for Nanoseconds

- Trigger signal propagation delay too long.
- Did everything to reduce latency.
 - Smallest number of devices in chain, shortest cables, optimized geometry.
 - DT5215 integrated trigger fanout has 20ns delay by itself (CAEN confirmed this...)
- Increased shaping time of DT5202 to maximum
 - 87.5ns up from 25ns
 - Will need conversion factor between 25ns lab LED+cosmics and 87.5ns beam data...
- Finally saw some MIPs







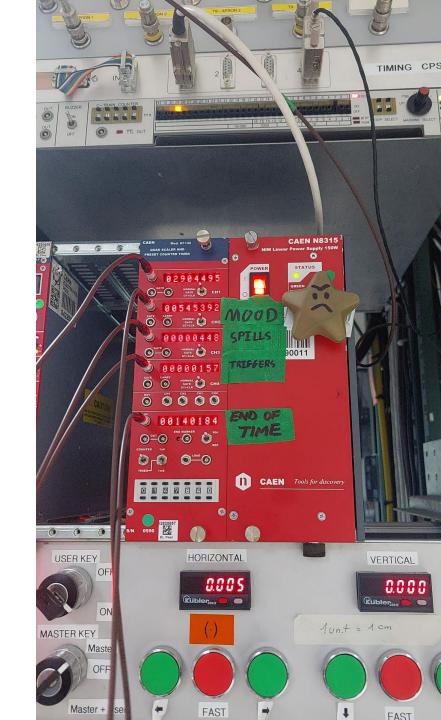
The CAEN Saga pt3: Fighting TDLinks

- Found the signal, but readout very unstable
 - Crashing every 0-5 minutes
 - Most likely due to instabilities in "TDLink" between units
- Suspected temperature issues
 - Stripped all CAEN units of their casing and forced air through everything
- Contacted CAEN, had Zoom meeting with their engineers Friday afternoon: no result
 - New firmwares available with CRC checks, but made things way worse
- The mood got considerably worse at this point.



pt4: Happily Ever After

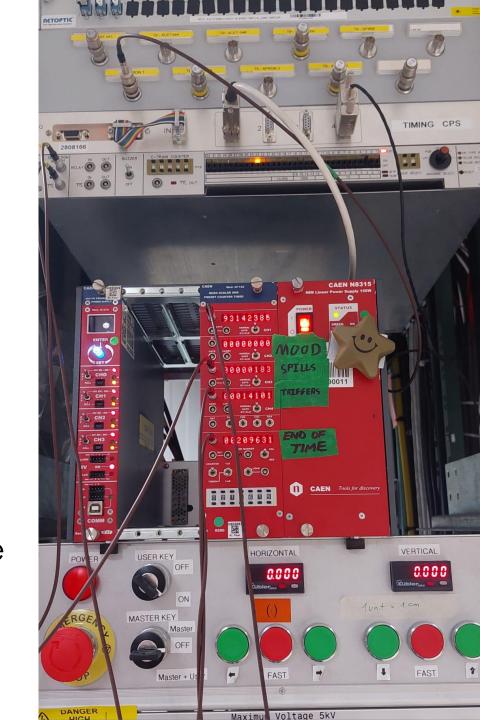
- Run without data concentrator?
 - DT5202 can be run individually in "parallel" via ethernet.
 - Asynchronous, but we distribute synchronous external triggers...
- That actually worked...
 - Needed some minor adjustments in trigger holdoff (maximum 600ish triggers per spill)
 - Shifter needs to make **really** sure all runs are started in between spills.
 - Otherwise no more major issues.

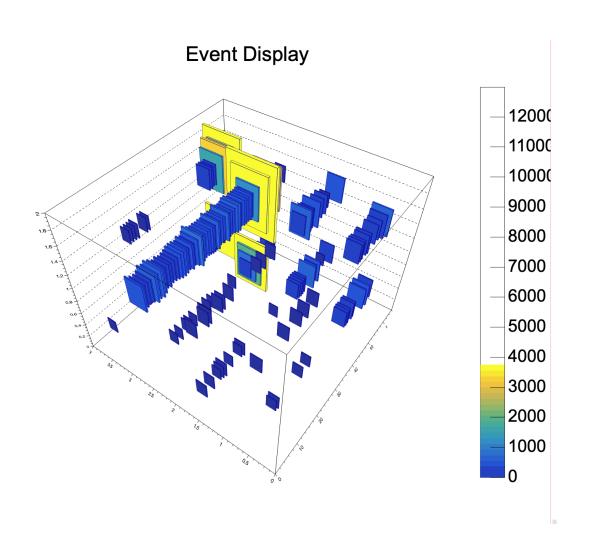




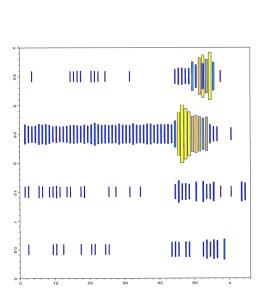
pt4: Happily Ever After

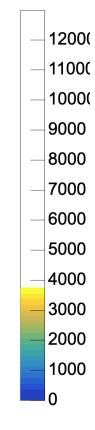
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Event Display

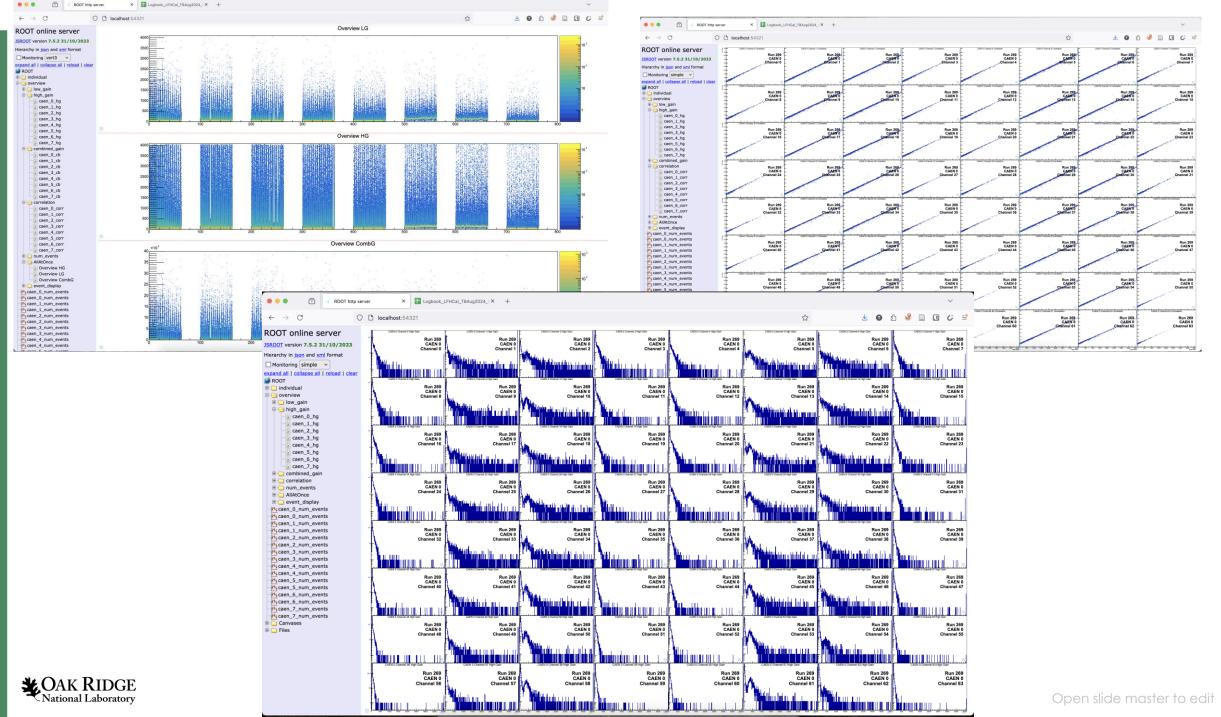




CAEN Run Summary

- 4.5days of full-time data.
- Full muons, electrons, hadrons at 3 SiPM bias voltages
 - Full rerun of 45V bias point at the end for validation
- Muon scan with various shaper settings
 - To intercalibrate beam vs. lab measurements
- Full electron energy scan at 6 SiPM bias points total
 - Including dedicated muon calibrations before and after each electron scan
- All QA'd by Tristan's live data monitor (modified for CAEN)





Shifters Summary

- Strong participation of various ePIC member institutes
 - Thanks to Fredi's tireless advertisement and "encouragement" to join
- Special thanks for support from ALICE FOCAL experts





Summary

- Testbeams never work as planned.
 - Always stressful, but ultimately always quite fun
- Nevertheless very successful campaign
 - Thanks to incredible support from many groups and people!
- All data backed up locally and on grid courtesy of Bill Li.
- Testbeams are bad for your diet.
- Additional resources





The 2025 Testbeam

- May (?) 2025: 8 fully equipped LFHCAL modules
 - 40cmx40cm, almost enough to contain hadron showers...
 - Full readout scheme test: HGCROC, summing boards
- 8x more of everything
 - Challenge in construction, setup, QA...
 - and then we need to do two more order of magnitude steps up towards full ePIC LFHCAL
- Software and simulation efforts from 2024 beam will enable 2025 analysis...
 - Moving towards implementing test beam analysis in eicsoft/eicrecon



CPAD 2024

- CPAD 2024 in Knoxville, TN!
 - November 19-22
 - Co-hosted by UTK and ORNL
- Extended abstract submission deadline 10/04 (this Friday!)

