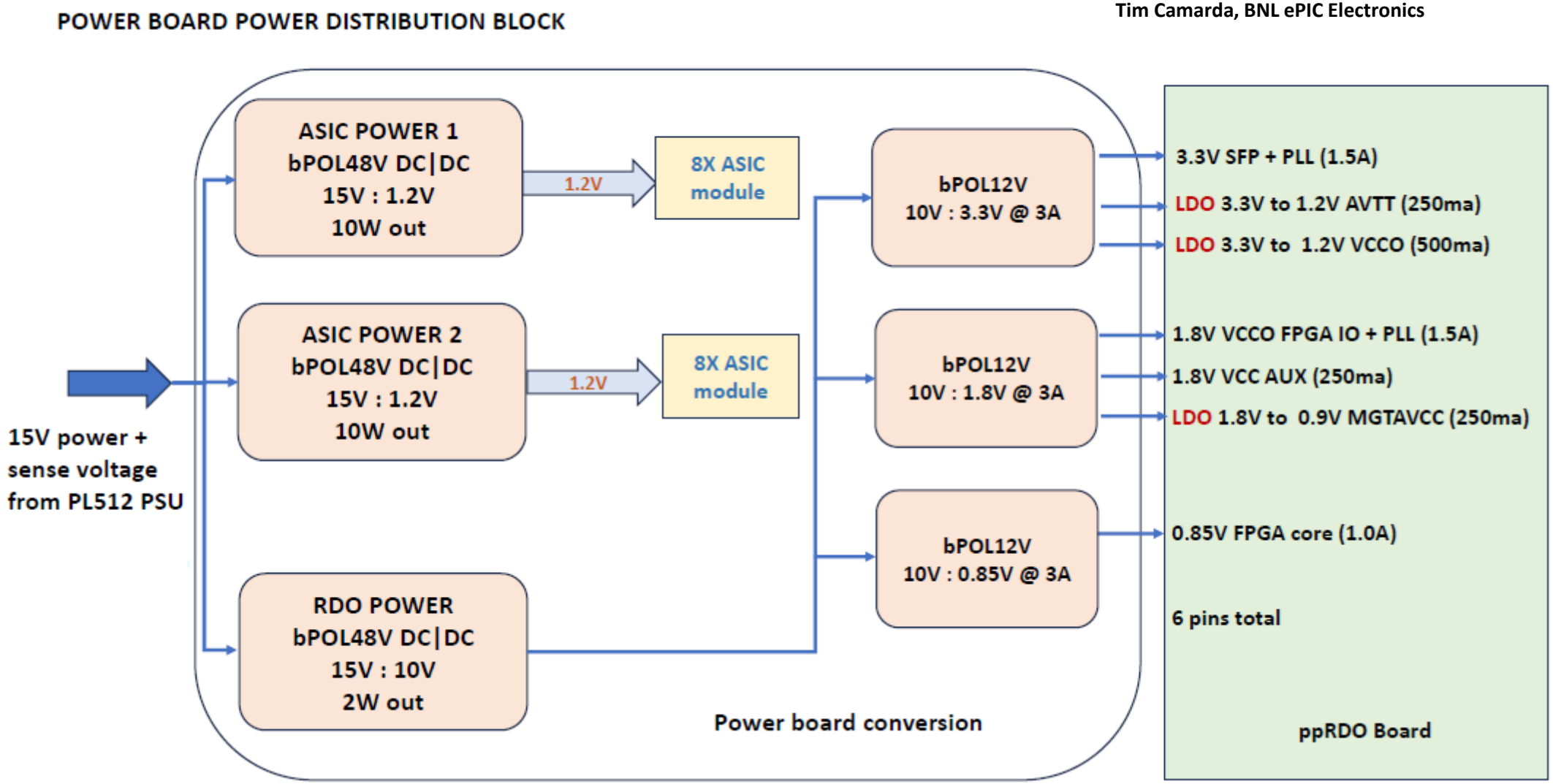
ePIC fTOF power board

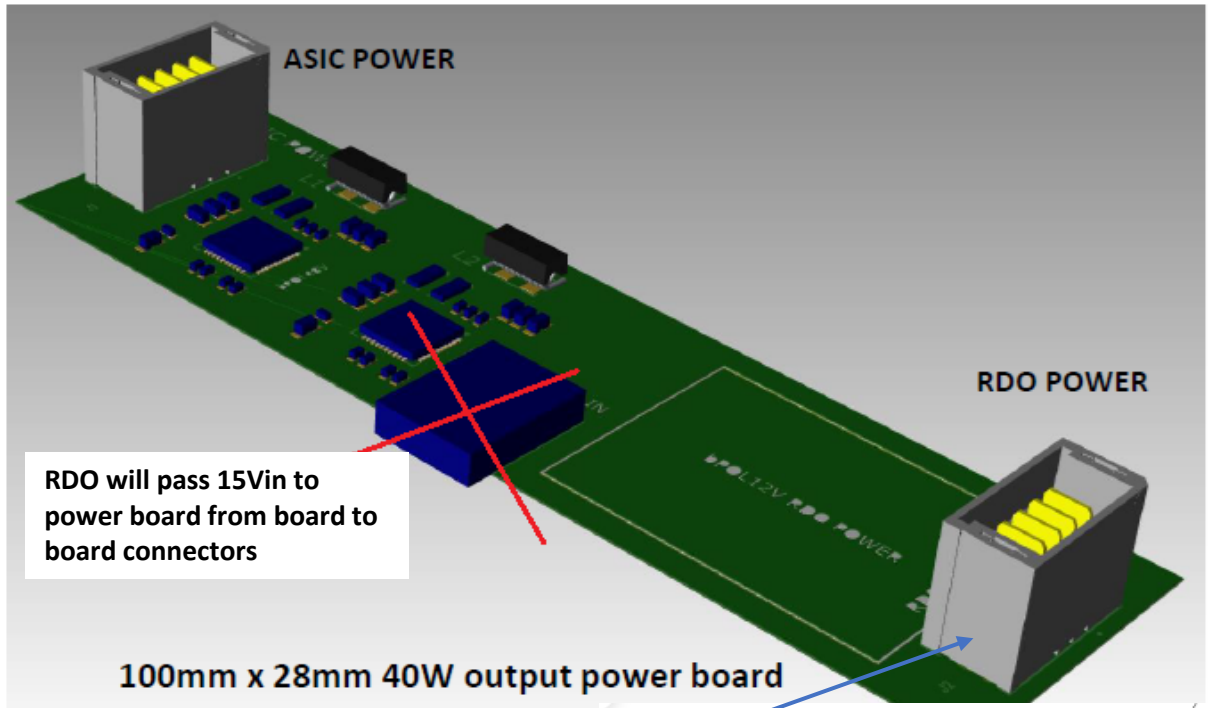
Update August/8/2024

Tim Camarda, BNL ePIC Electronics



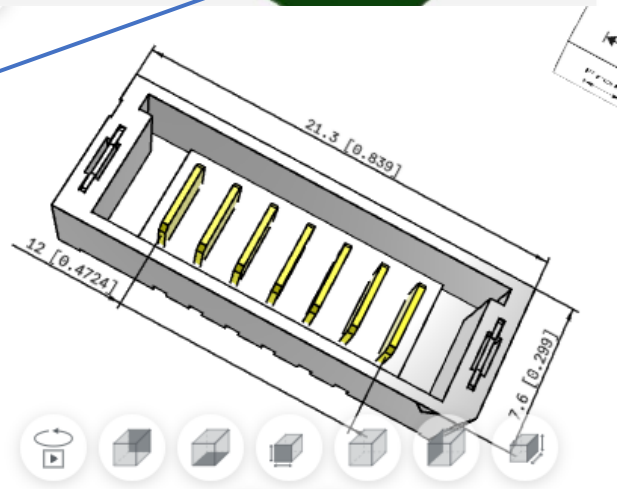
POWER BOARD PROTOTYPE DEVELOPMENT

Layers:	**4x to 6x**
	2.0 mm thick
Copper Weight:	**2oz top/bottom**
Heat transfer:	**Bottom copper w/ gold finish**
	Thermal compound or sil-pad
	mount to plate w/2.0mm screws
Component Mount:	**Top only**
Power Dissipation:	**~50W (~75% efficiency)**



1.PBv0 schematics 50% complete, Order major parts
Date: January 2025
2.PBv0 schematics 100% complete (with internal review); Order all parts
Date: March 2025
3.PBv0 PCB layout complete (with internal review)
Date: May 2025
4.PBv0 fabrication and assembly complete. Boards delivered.
Date: July 2025
5.Basic electrical, power QA, acceptance testing.
Date: September 2025

UMPT-07-01.5-G-V-S-W-TR



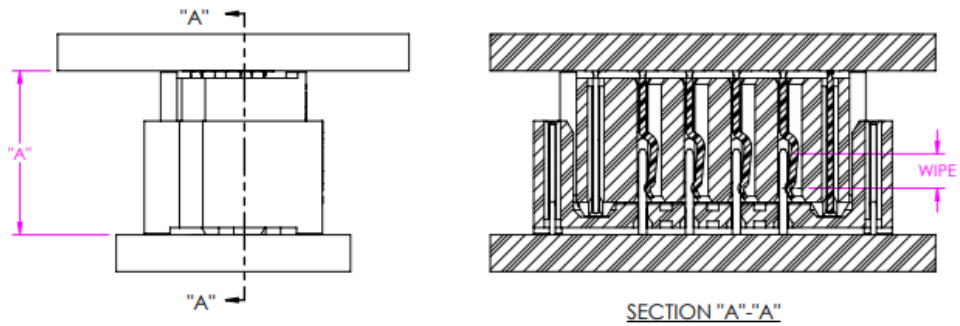
ASIC POWER	RDO POWER
1. +15V in	1. 3.3V+
2. 15V rtrn	2. 3.3V-
3. 1.2V +1	3. 1.8V+
4. 1.2V -1	4. 1.8V-
5. 1.2V +2	5. 0.85V+
6. 1.2V -2	6. 0.85V-
7. enable	7. ASIC reset

REVISION D

10/6/2021 | ECN-420354

UMPX MATED VIEWS

DESIGNED & DIMENSIONED IN MILLIMETERS[INCHES]



SECTION "A"-"A"
SCALE 4 : 1

FIG 1
UMPT MATED WITH UMPS

TABLE 1

		UMPS LEAD STYLE						WIPE	
		-03.5		-05.5		-07.5			
		"A" FULLY MATED	"A" MAX	"A" FULLY MATED	"A" MAX	"A" FULLY MATED	"A" MAX	FULLY MATED	MIN @ "A" MAX
UMPT LEAD STYLE	-01.5	5.00 [.197]	6.09 [.240]	7.00 [.276]	8.09 [.319]	9.00 [.354]	10.09 [.397]	1.47 [.058]	0.38 [.015]
	-02.5	6.00 [.236]	7.09 [.279]	8.00 [.315]	9.09 [.358]	10.00 [.394]	11.09 [.437]	1.47 [.058]	0.38 [.015]
	-06.5	10.00 [.394]	11.09 [.437]	12.00 [.472]	13.09 [.515]	14.00 [.551]	15.09 [.594]	1.47 [.058]	0.38 [.015]
	-07.5	11.00 [.433]	12.09 [.476]	13.00 [.512]	14.09 [.555]	15.00 [.591]	16.09 [.633]	1.47 [.058]	0.38 [.015]
	-12.5	16.00 [.630]	17.09 [.673]	18.00 [.709]	19.09 [.752]	20.00 [.787]	21.09 [.830]	1.47 [.058]	0.38 [.015]

NOTES:
1. ALL DIMENSIONS BASED ON NOMINAL VALUES FOR SAMTEC RECOMMENDED PCB LAYOUTS.
2. ALTHOUGH MAX DIMENSIONS ARE LISTED SAMTEC RECOMMENDS FULLY MATING COMPONENTS.

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RDO preliminary power measurements

Label	Vout	VSHUNT	IAMPS	WVREG(OUT)	VDROP	WLOSS	Eff
3.3FMC	3.3	0	0.000	0.000	0.7	0	
1.8MGT	1.80	4.000E-04	0.020	0.036	2.2	0.044	45.0%
FPGA 1.2V	1.20	2.000E-03	0.100	0.120	2.8	0.28	30.0%
0.9AVCC	0.90	8.000E-04	0.040	0.036	3.1	0.124	22.5%
1.2AVTT	1.20	2.800E-03	0.140	0.168	2.8	0.392	30.0%
0.85	0.85	4.000E-03	0.200	0.170	3.15	0.63	21.3%
1.8V	1.80	1.610E-02	0.805	1.449	2.2	1.771	45.0%
3.3V	3.30	1.160E-02	0.580	1.914	0.7	0.406	82.5%
Total				3.893		3.647	