Update on estimates for the Insert design and readout scheme

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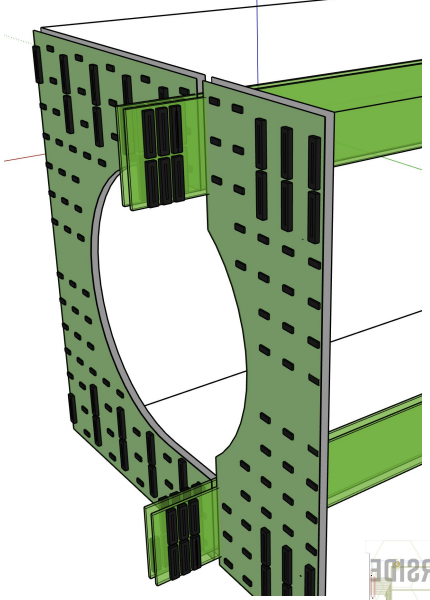
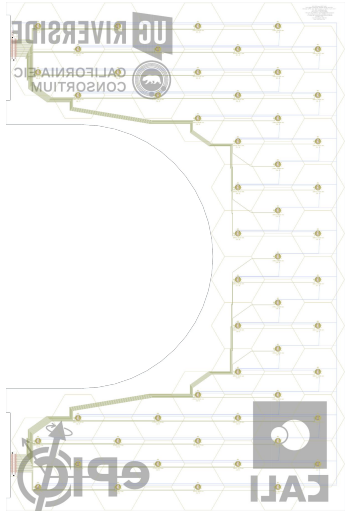
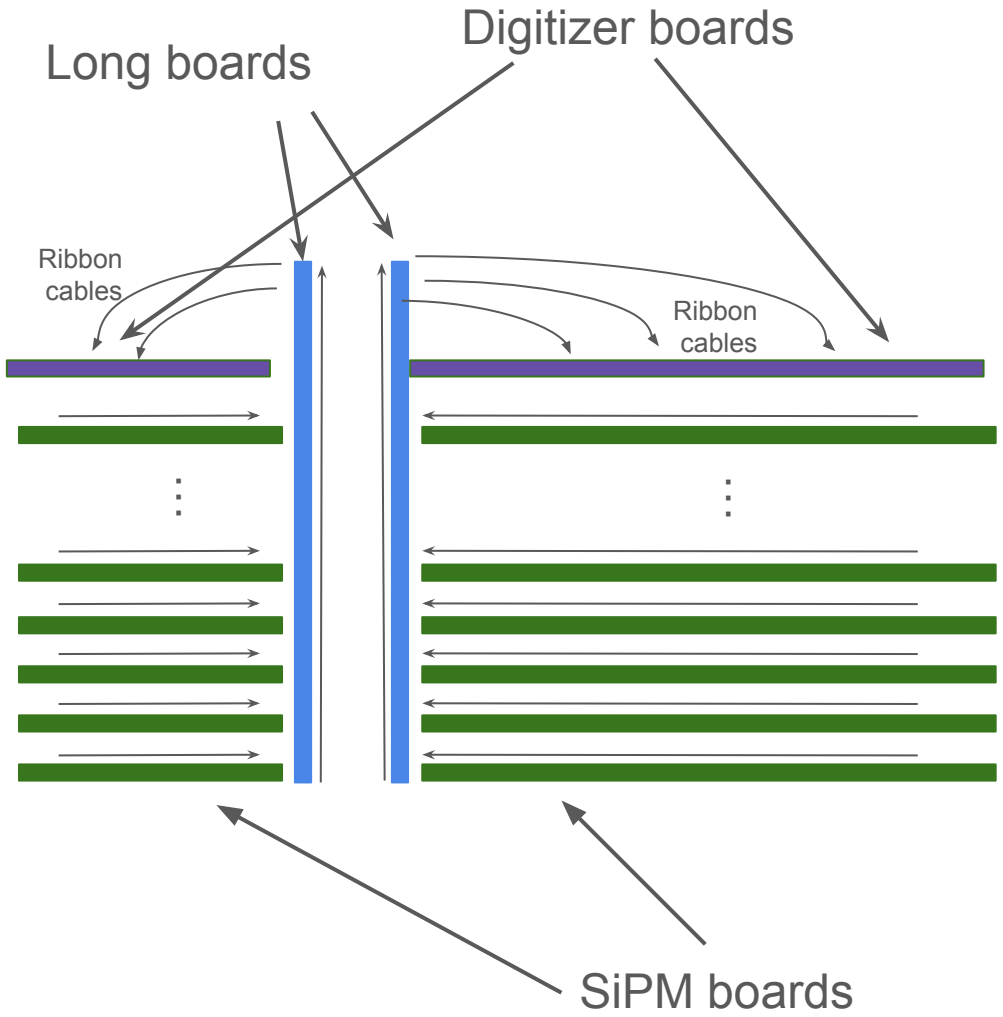




General schematics

- PCB boards with PCBs connect to the 4 long boards (2 on right, 2 on left)
- Long boards transfer signals to the ASIC digitizer boards at the back with ~100 CALOROC chips via ribbon cables



Long board for transfer to readout (4 total)

Part of this board sticks out at downstream end so that it can connect to ASIC digitizer boards

Board goes along length of detector

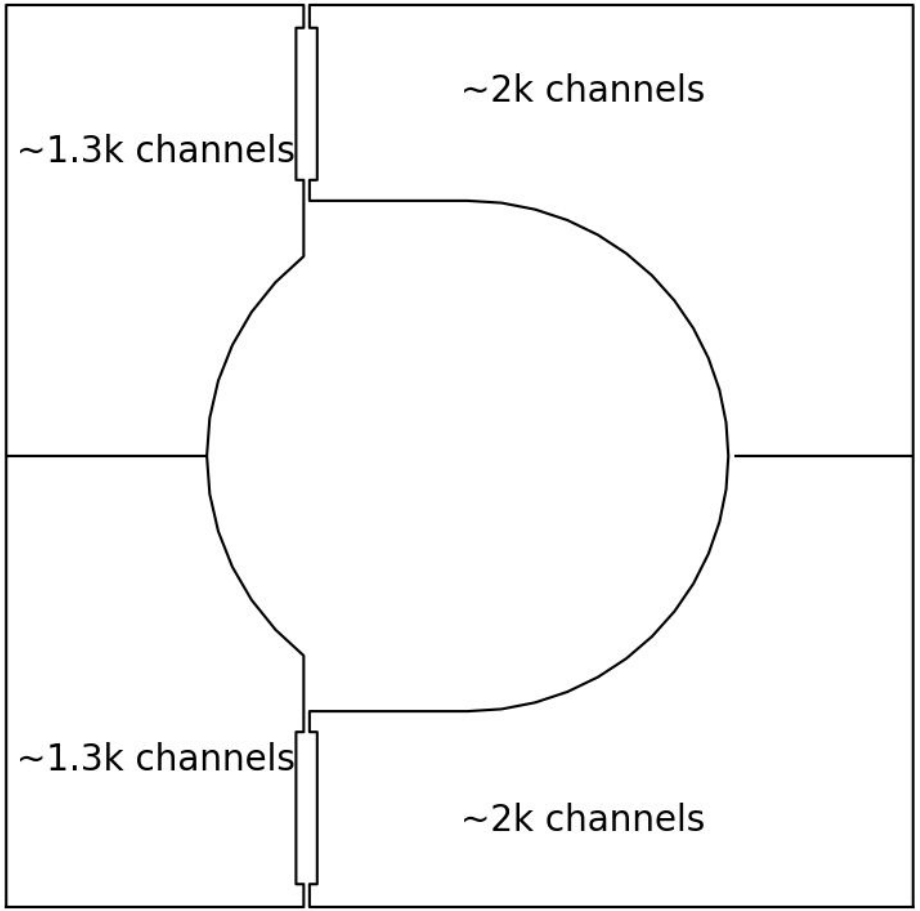
~4.2k traces (1 anode + 1 cathode) can be read out with nine 500-pin ribbon connectors*

*connectors shown are one possible implementation

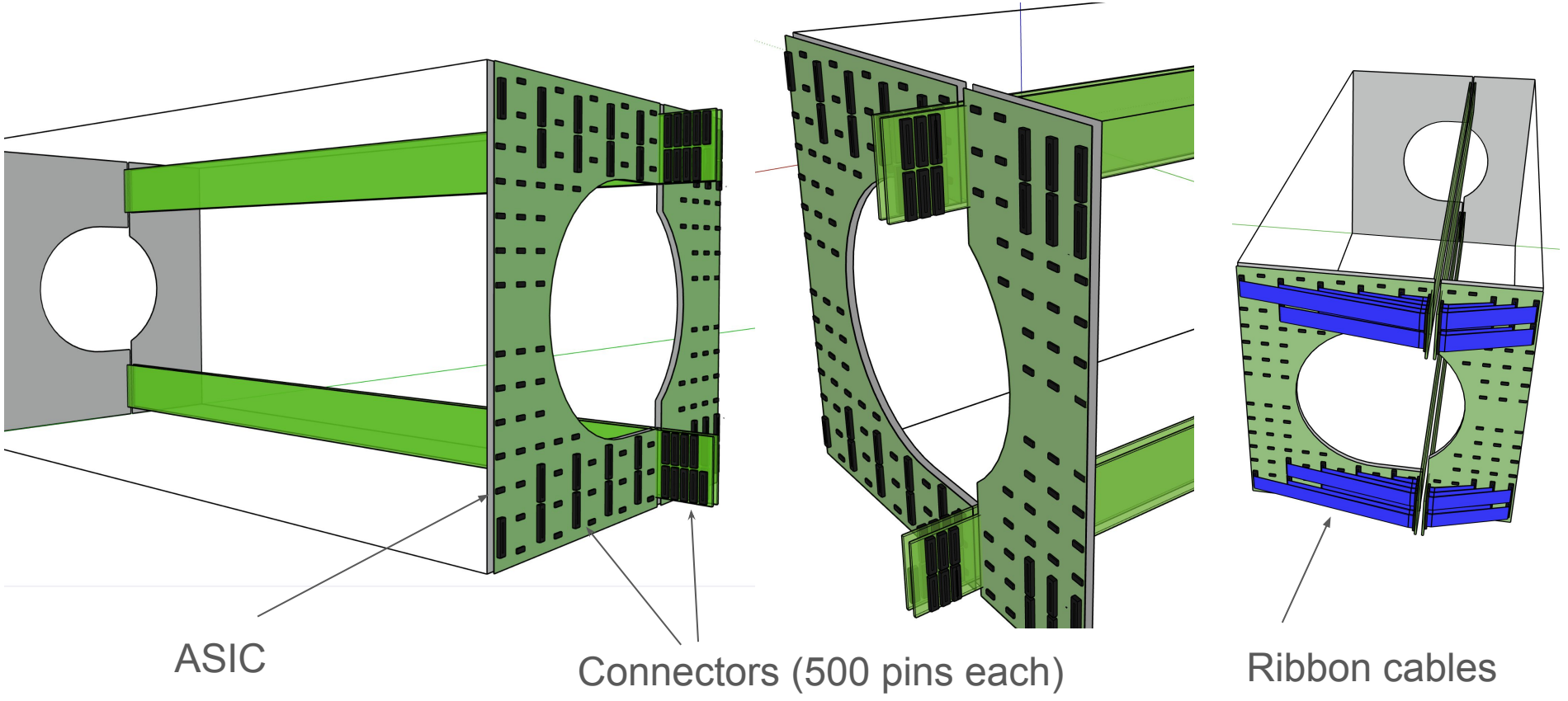
How many signals per quadrant?

Each long board services one quadrant of the insert

Total number of channels assumed ~7k.



Long boards stick out at the front of the detector, to connect with the ASIC boards



ASIC boards

Each ASIC and its electronics require ~2x2 cm^2

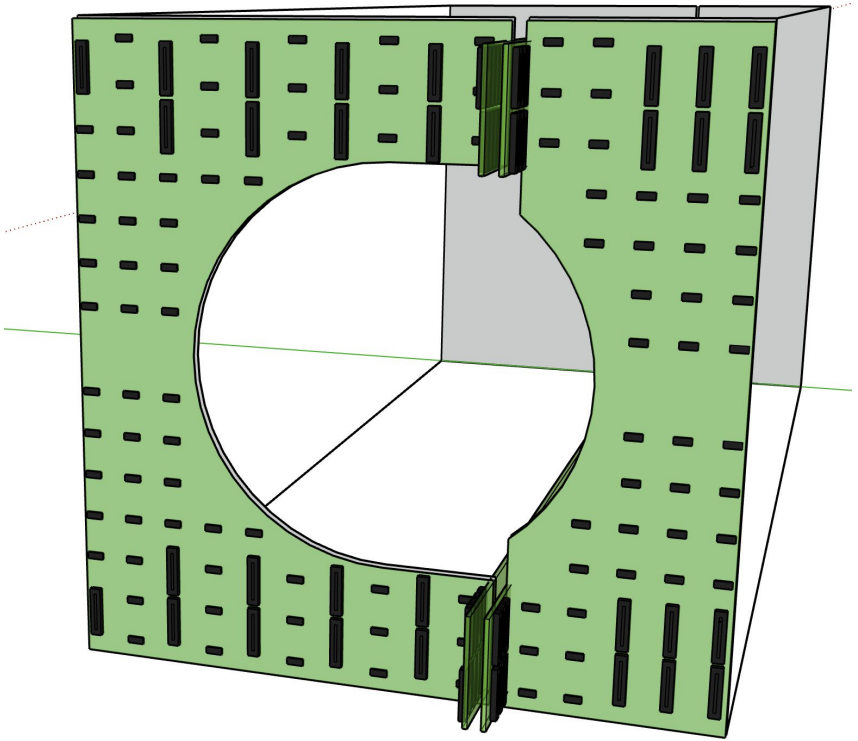
72 channels per H2GROC ASIC → 60 chips for right-side channels and 40 for left-side ASICs

Here we show 4 cm center-to-center of ASIC chips

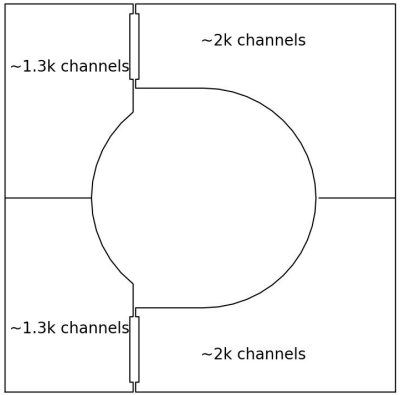
Total: 100 ASICs chips ~ 225 W.

Total connectors on ASIC boards (both sides)=30

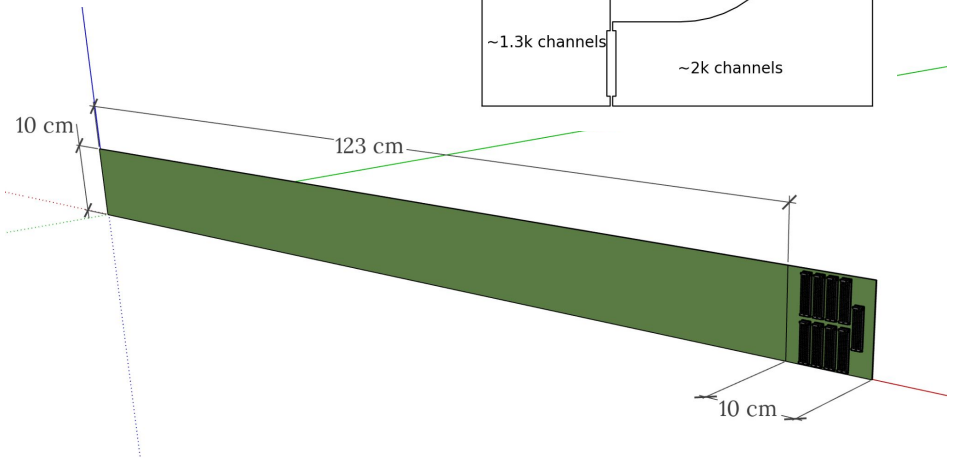
Total pins=15k (2 per signal)



Trace estimate in Long boards (one per quadrant)

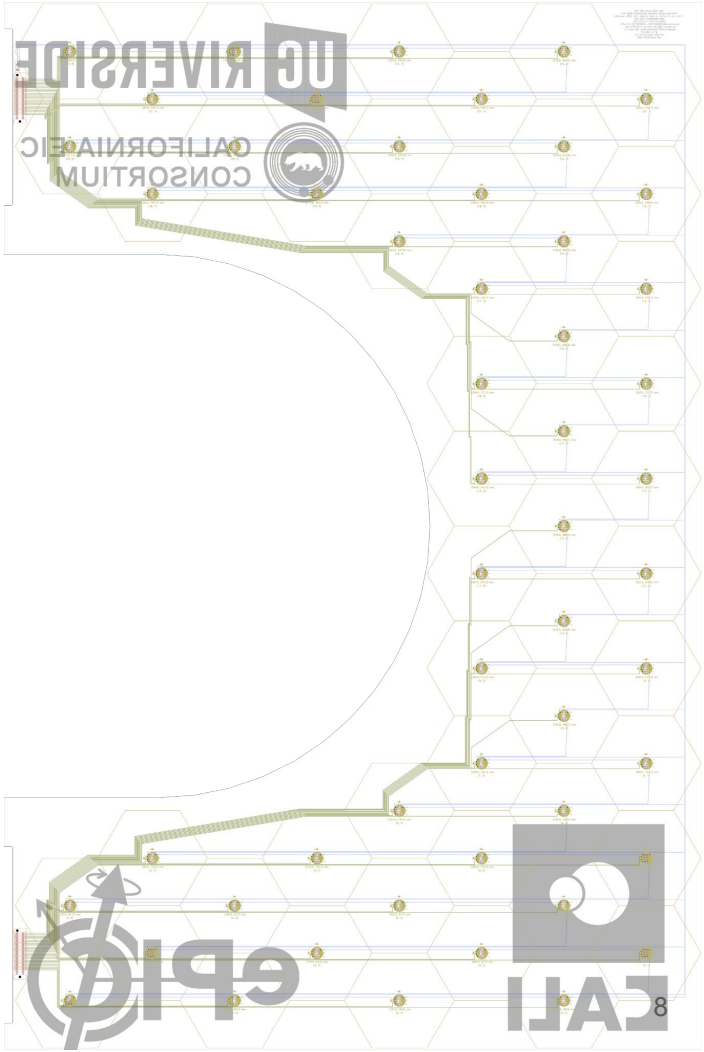


- Can we fit all the traces we need?
  - Gerard suggested us **“Differential pairs with 200 µm traces, 200 µm between them, with 500 µm between them → 1.1 mm per signal”**
  - Requires ~1.3k*1.1mm/12cm ~ 12 signal layers for left boards, and ~2k*1.1mm/12cm~18 signal layers for right boards

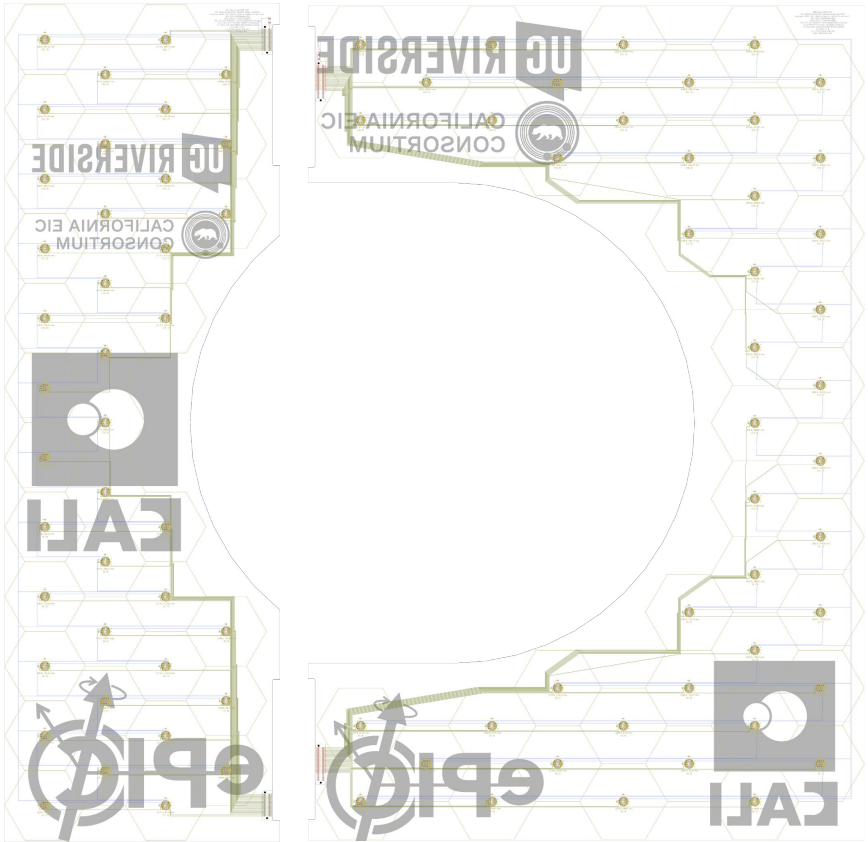


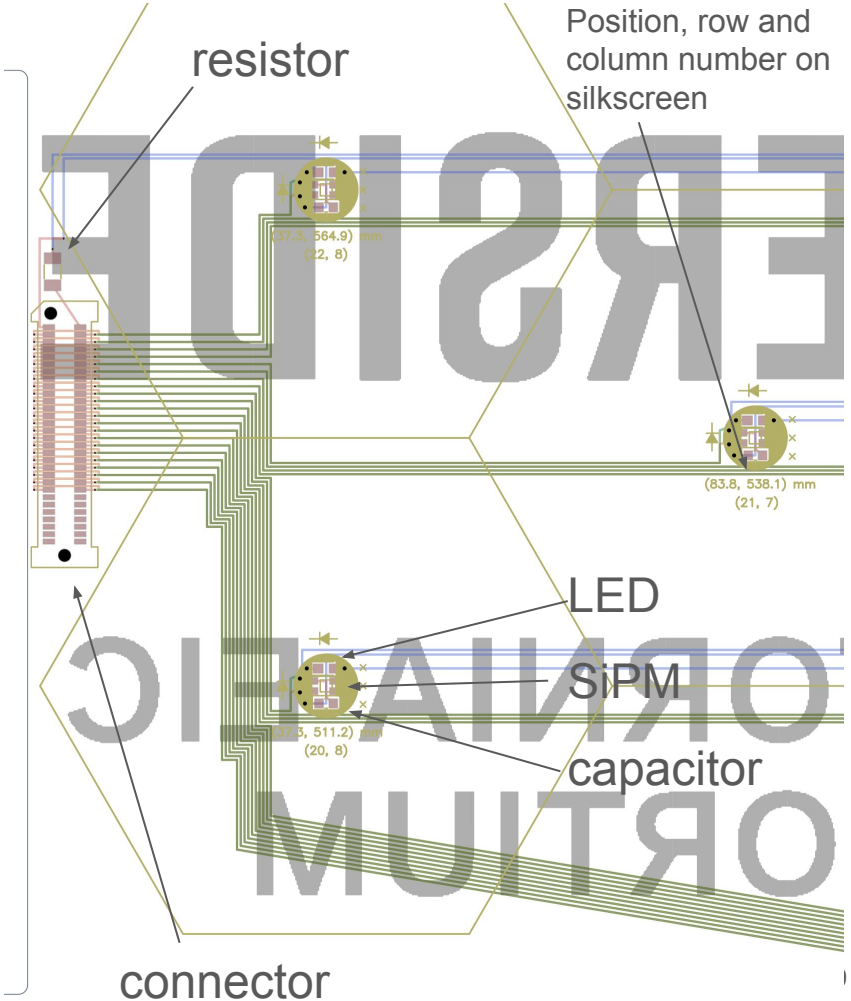
Status of SiPM-carrying boards

- Algorithms determine the position of the boards
- Generates layouts for left-side boards (all layers) and right-side boards (layers 21-60)



Some more screenshots of PCB boards

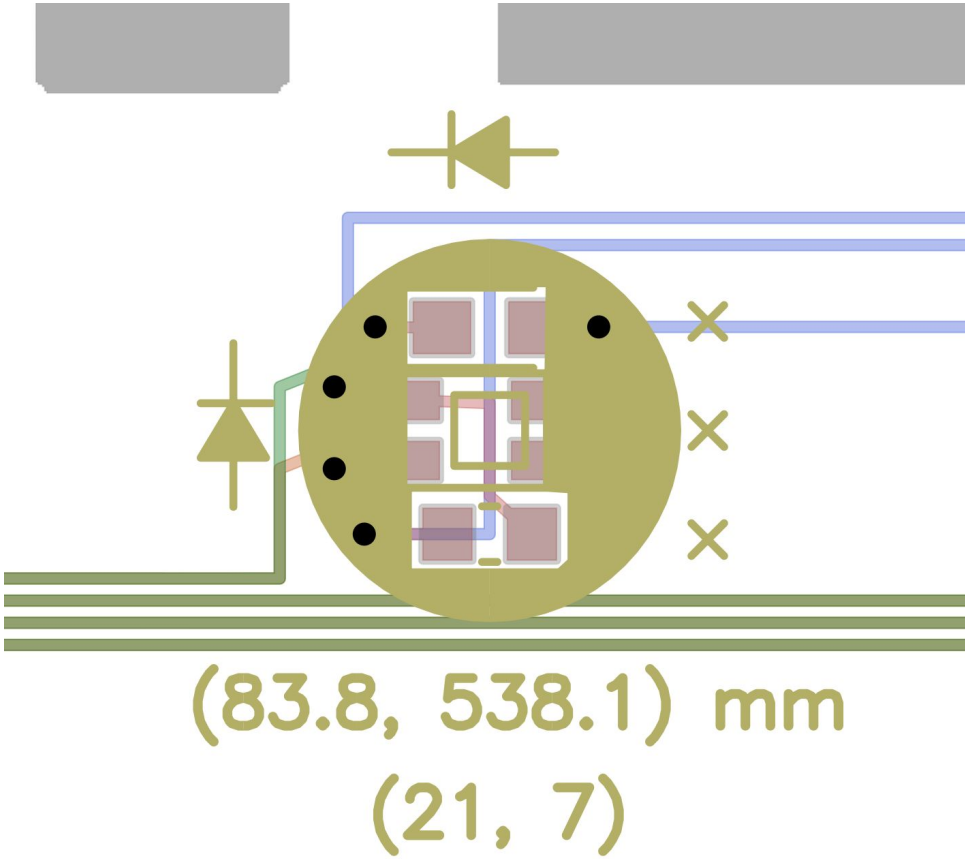




More screenshots

Documentation on back

CALI PCB board R60
minimum space between channels=0.4064 mm
From top to bottom in each dimple: LED, SiPM, capacitor
LED=SM0603UV-405 x45
SiPM=S14160-1315PS x45
capacitor=AGC0603X7R101-103KNP (10 nF) x45
connector=HSEC8-130-01-I-S-DV-A x2
resistor=CRCW120649R9FKEAC (50 ohm) x1
# of cells=45
cell side length=3.10 cm
cell area=25.0 cm2

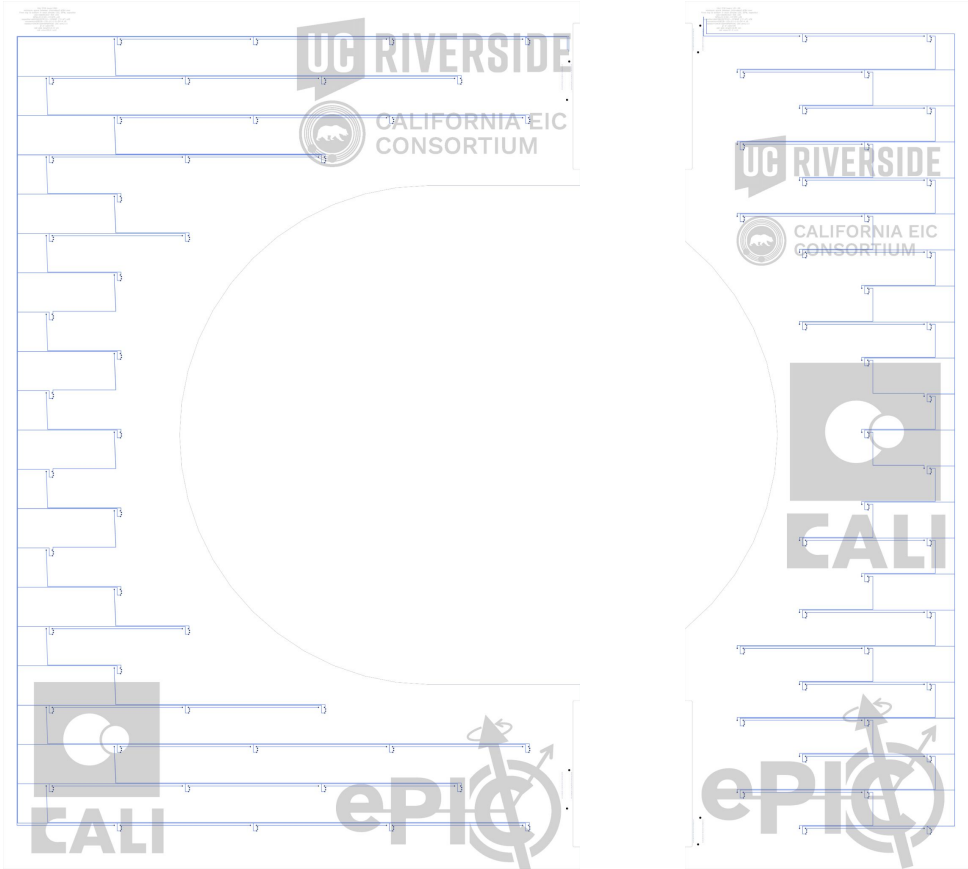


Back sides:

Traces for ground, LEDs

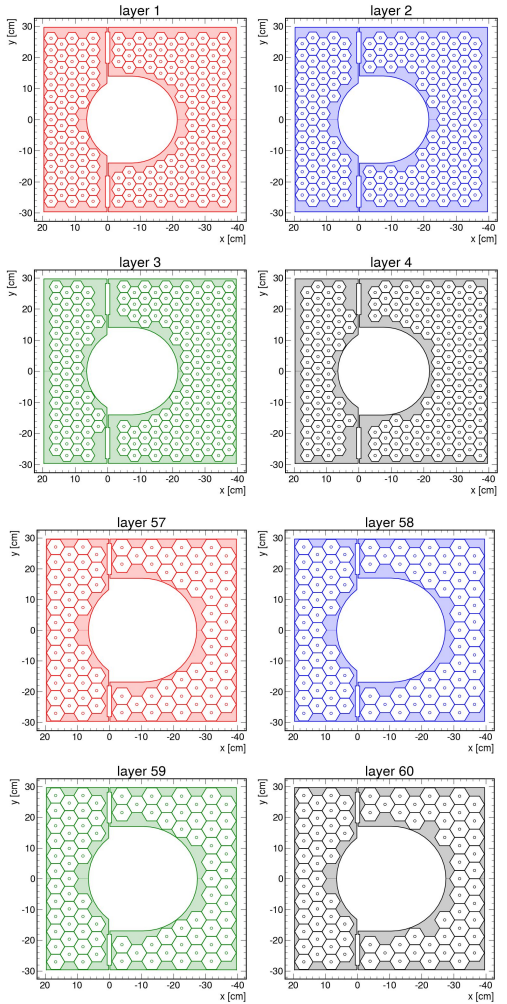
Documentation

Logos



Update of geometry in ePIC repository

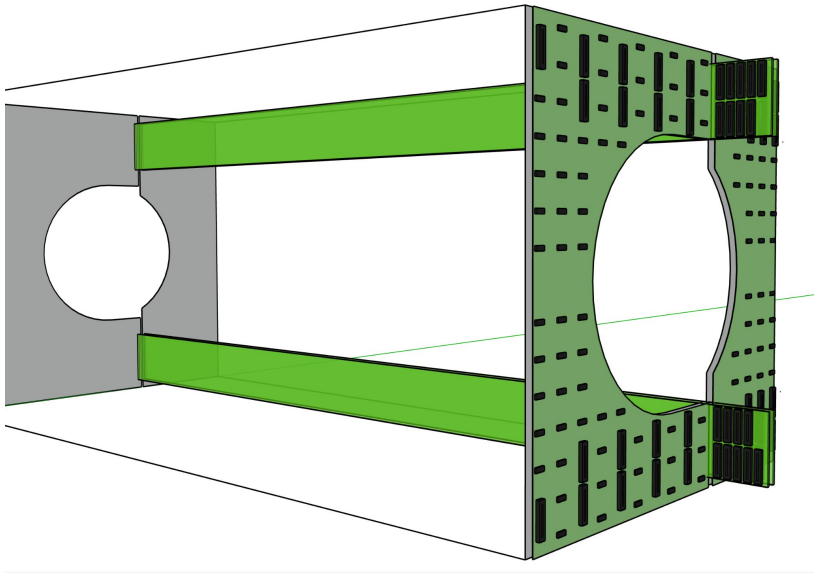
- Previously, we had the entire detector implemented with small hexagons that were staggered
- Pull request 771: updated geometry with small hexagons (~12 cm^2) for layers 1-20, and larger hexagons (21 cm^2 and 25 cm^2) in the later layers
  https://github.com/eic/epic/pull/771
- TODO make sure the transverse offsets in each section match those I had determined algorithmically



https://github.com/eic/epic/pull/771

Summary

- We estimate that we can readout ~7k channels with space available at the backend, using ~20 signal layers for long-PCBs
- SiPM-carrying boards are being developed algorithmically
- ePIC repository is being updated with the corrected geometry



Backup

Coverage of the insert

Though much smaller than the endcap, it covers a very large range in pseudorapidity for its size:

- Endcap (without insert): roughly $1<\eta^*<3$
- Insert: roughly $3<\eta^*<4$,
  - about ⅓ of the total η^* coverage in ~1.5% of its total area
  - High density of incident particles