High-Speed Data Transmission IP's in 65nm CMOS Image Sensor Process at the Electron Ion Collider

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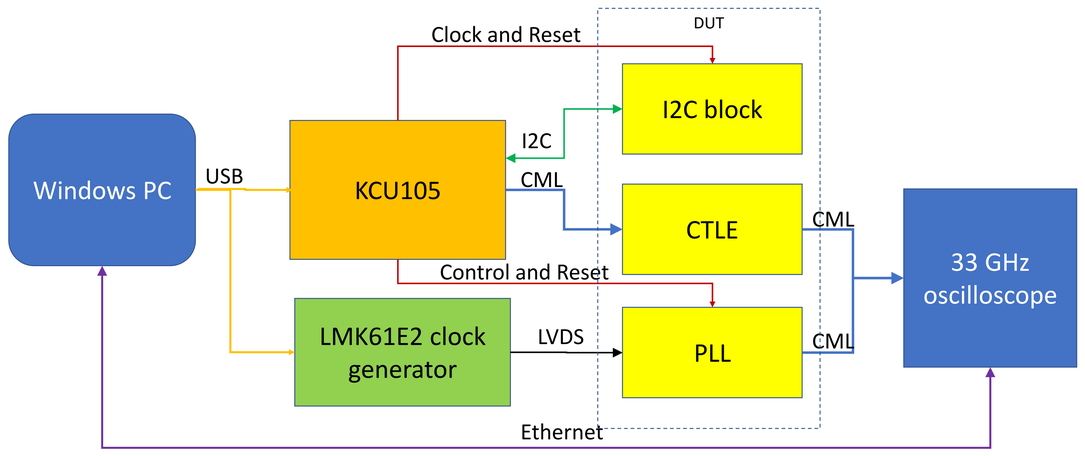
Introduction

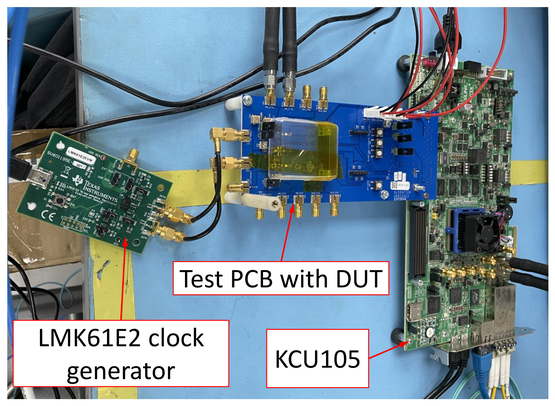
Next generation particle physics experiments like Electron Ion Collider (EIC) demand high-speed data communication and lower mass designs for its detectors, Novel scientific detectors will be based on high speed serial links.

This poster presents initial test results for circuits designed to meet these needs including a dual-frequency Phase Locked Loop (PLL), an I2C block and a high speed CML receiver.

Test setup

A PCB was designed to carry the test chip, with low speed control provided from a KCU105 Xilinx Kintex Ultrascale development board.
The reference clock for the PLL is provided from a Texas Instrument LMK61E2 clock chip evaluation card.
The input to the CTLE was provided from the KCU102 using iBert designs via SMA cables.
The high speed CML signals from the CTLE and PLL were cabled via SMA connectors to a Tektronix MSO73304DX 33 GHz oscilloscope.
Control of all blocks was automated using python.





I²C block

The I²C block is an instance of a configurable soft macro. Each I²C address provides one inbound register which can be written to over the I²C bus. These inbound registers are triplicated, with triple-majority voting and data scrubbing. Each address can also allow 8 bits of on-chip signals to be read out over I2C.

In this test chip the I²C block was configured to provide 3 I²C addresses. Two of the 3 connect the inbound register to the outbound register to allow the software to write and then read back the data to test it.

The KCU 105 was programmed with a design based on a microblaze microprocessor including an I²C master to allow read write testing of the custom I²C block.

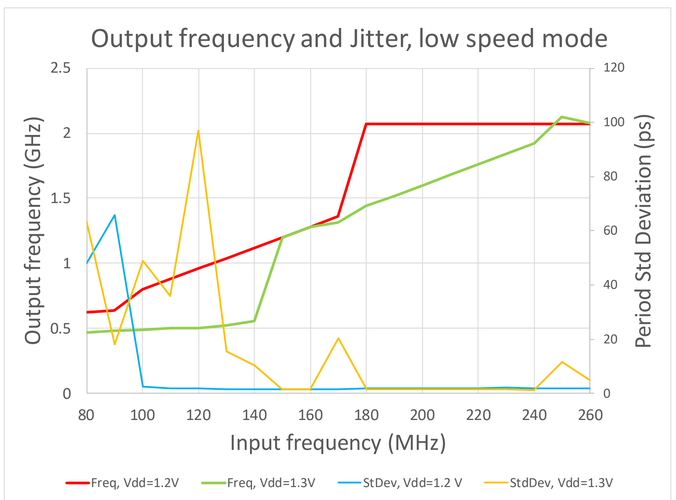
The I2C block was tested with multiple writes and reads and worked as expected.

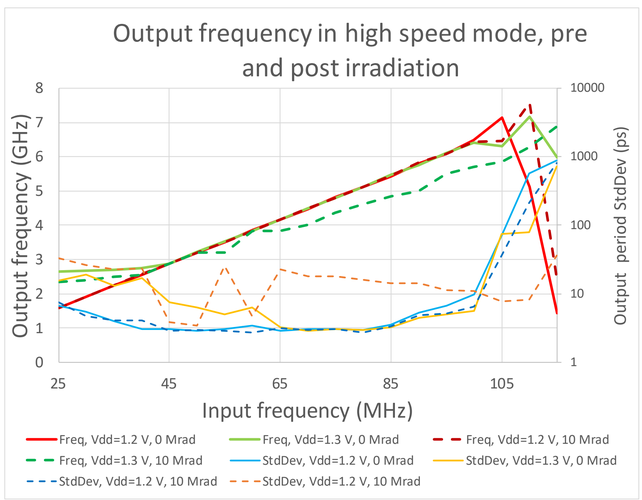
PLL

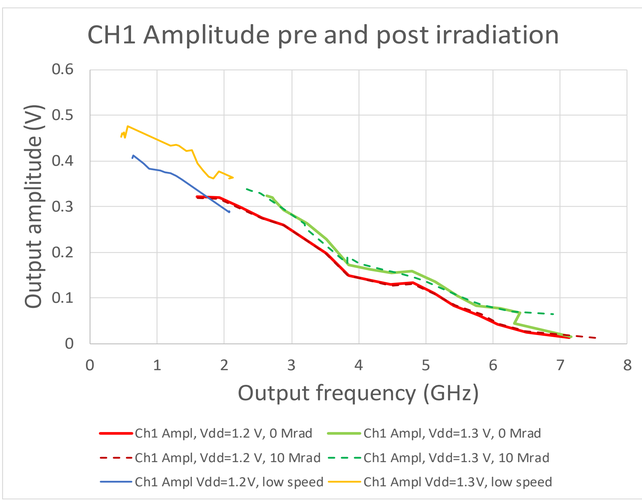
The PLL test block consists of a dual frequency PLL+VCO with a direct CML output and a PRBS generator.

In low frequency mode the VCO frequency is 8 x the input reference clock, targeting a 800 MHz to 2 GHz output.

In high speed mode the output frequency is 64 x the input, targeting a 5.5 GHz to 7 GHz output.







The graph left shows the output frequency against input frequency in low speed mode. The linear ×8 frequency relationship is maintained for different regions of input frequency depending on the supply voltage. The standard deviation of the period is plotted as a measure of jitter.

The graph middle shows the output frequency against input frequency in high-speed mode. The linear 64 × frequency relationship is maintained over a wide range of input frequencies which is changed slightly increasing Vdd to 1.3V. After 10 Mrads of irradiation the behaviour at Vdd=1.2V is not significantly changed, though at 1.3V it is.

The graphs right show the output amplitude against output frequency plotting data from both low speed mode and high speed mode. The output amplitude decreases very significantly with increasing output frequency. Increasing Vdd to 1.3V increases to output amplitude but does not change its frequency dependency. Additional tests varying the bias currents of the CML outputs did not strongly change the frequency dependency. An unpopulated board was tested and showed that the output trace had a transmission of approximately 90% at 5 GHz, so was not dominating these tests.

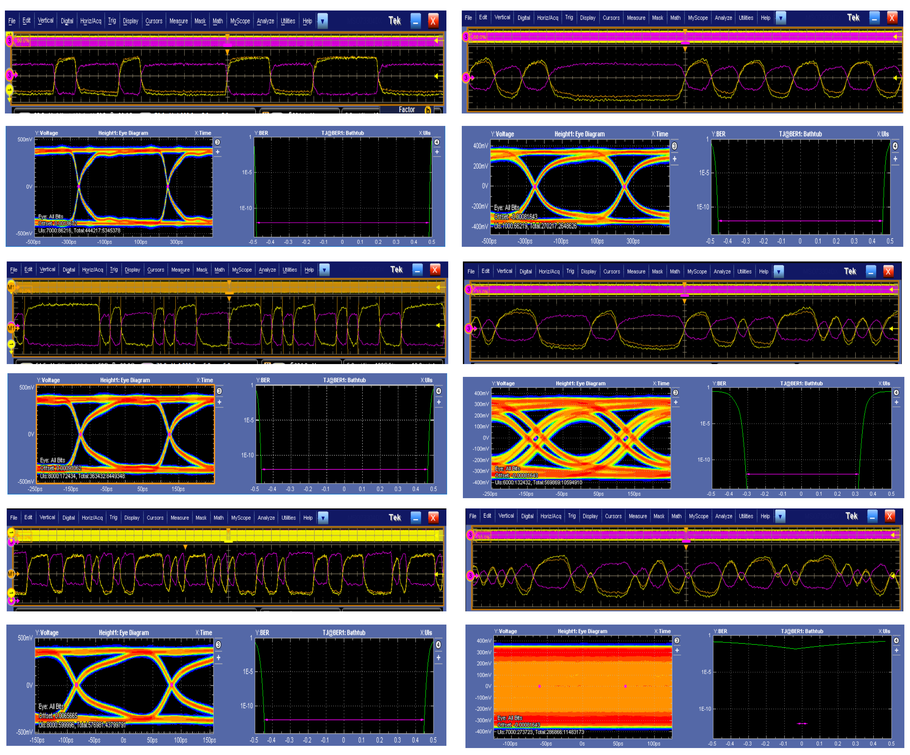
CTLE

The Current-Mode Logic (CML) receiver consists of a Continuous Time Linear Equaliser (CTLE, filter) followed by a CML to CMOS converter and then a CML output driver. The CTLE attenuates low-frequency signal components, amplifies components around the Nyquist frequency and filters off higher frequencies to compensate for transmission path loss without boosting noise.

The CTLE was tested using a Xilinx KCU105 programmed with iBERT designs to generate CML signals. The data was viewed using an oscilloscope.

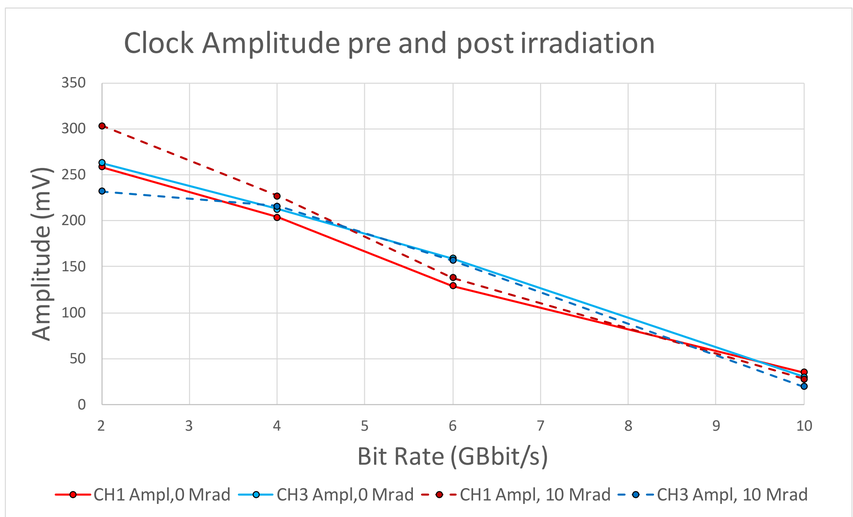
These plots show the raw data with the eye diagram and bathtub plots reconstructed by the 'scope for PRBS test patterns. LHS: KCU105 connected directly to the 'scope. RHS: via the CTLE.

The top plots are at 2 Gbits/s. The eye is clearly open.



The middle plots are at 4 Gbits/s. Note how via the CTLE the eye starts to close.

The bottom plots are at 6Gbits/s. For the signal directly from the KCU105 the eye is open, with some reduction in the open area. The 'scope cannot reconstruct an eye from the output of the CTLE. Looking at the raw data note how sometime a lone 1 does not cross the mid value.



This graphs shows the output amplitude of CH1 (p) of the CTLE when supplied with a fast clock (0101010) test pattern which can be easily quantified using the 'scopes measurements. The decreasing output amplitude with increasing frequency is clear.

The results are not significantly degraded after 10 Mrad of irradiation.