Science & Technology Facilities Council
Daresbury Laboratory

ALICE

babyMOSS training at CERN

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ePIC UK WP1 meeting

25/09/2024

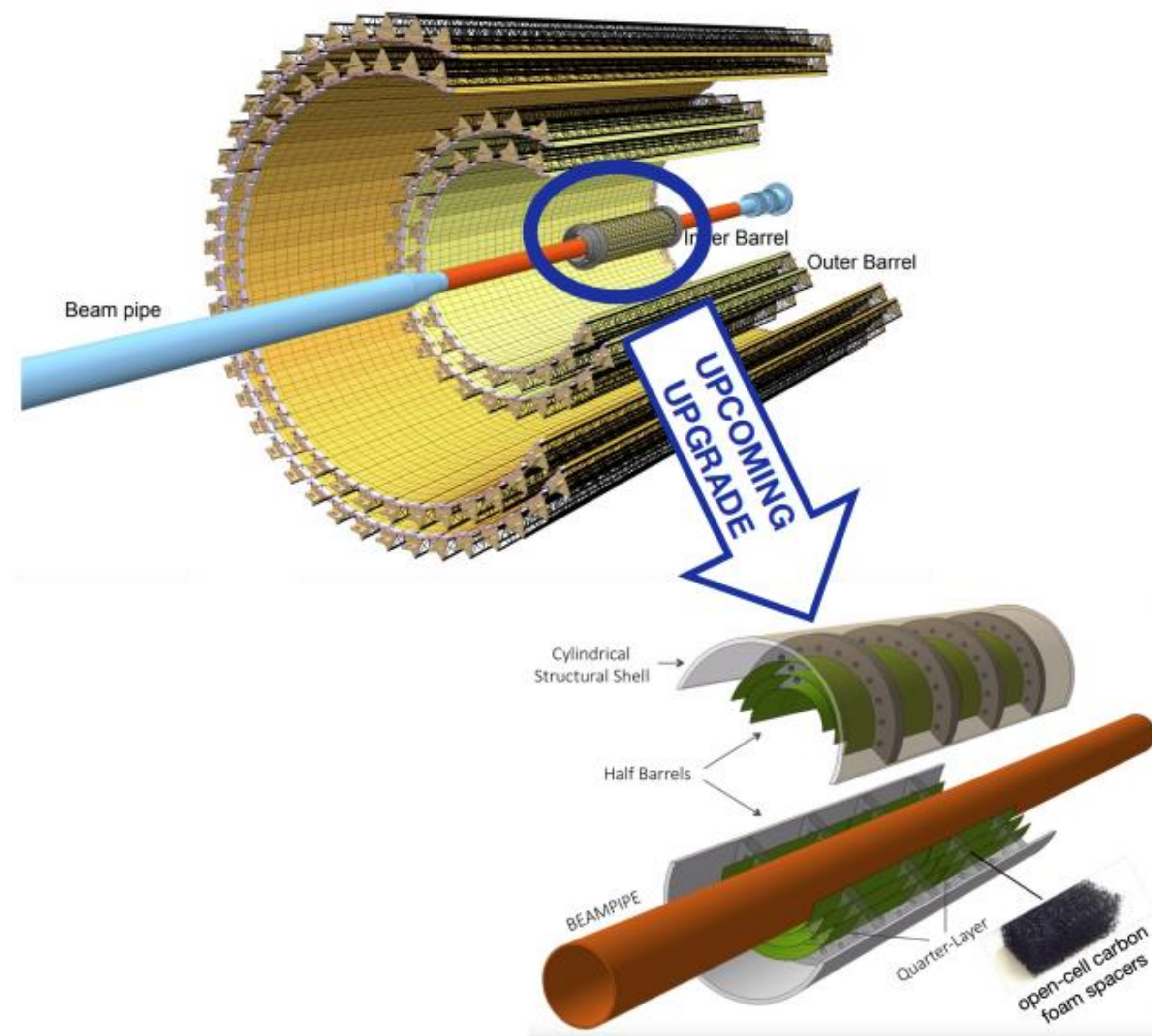
Introduction

- Daresbury is involved in the ALICE ITS3 project
- Have contributed to chip testing of the previous prototypes (MLR1)
- Want to continue the knowledge with the next prototypes (ER1)

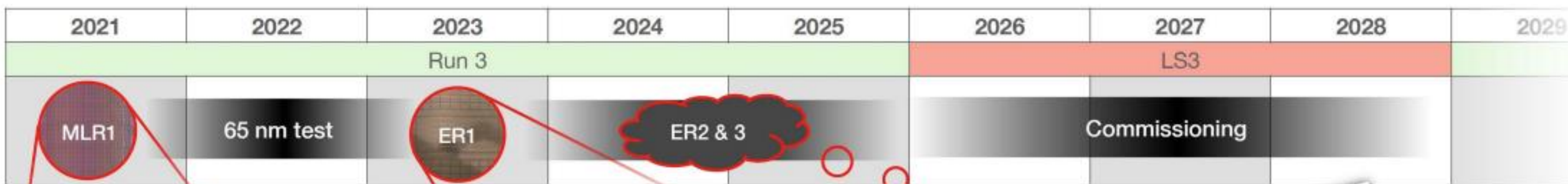
- Spent 2 weeks at CERN for training on the babyMOSS chip and test system
- Goal was to learn how the system and chip work so we can have a test system at DL and contribute to the chip characterisation

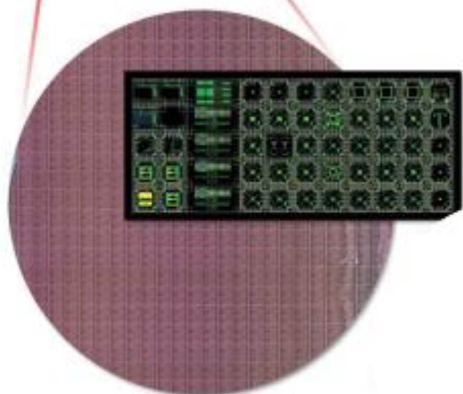
Reminder: ALICE ITS3 concept

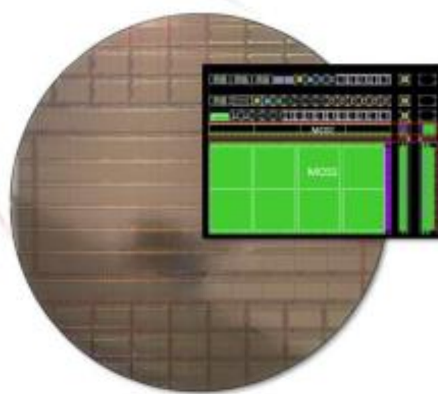
- Currently the ITS2 is installed and taking data, it uses the ALPIDE chip
- Can we improve on this by removing most of the material -> wafer-scale bent MAPS thinned < 50 µm
- Replace the 3 innermost layers with cylindrical silicon sensors in LHC LS3 (2026-2028)
- Concept:
  - Cut rectangular sensors from a stitched wafer
  - Bend to half-layers
  - Stack the 3 half-layers -> half barrel
  - Place the two half barrels around the beam pipe -> ITS3 barrel
- TDR published: https://cds.cern.ch/record/2890181



Sensor R&D timeline







Multi-Layer Reticle 1 (MLR1)

First submission in TPSCo 65 nm:

- Lots of prototypes: 55 chips
- Goal: qualify the technology (achieved)

Engineering Run 1 (ER1)

First wafer-scale stitched sensors:

- Two large stitched prototypes
- Goal: assess yield and stitching (ongoing)

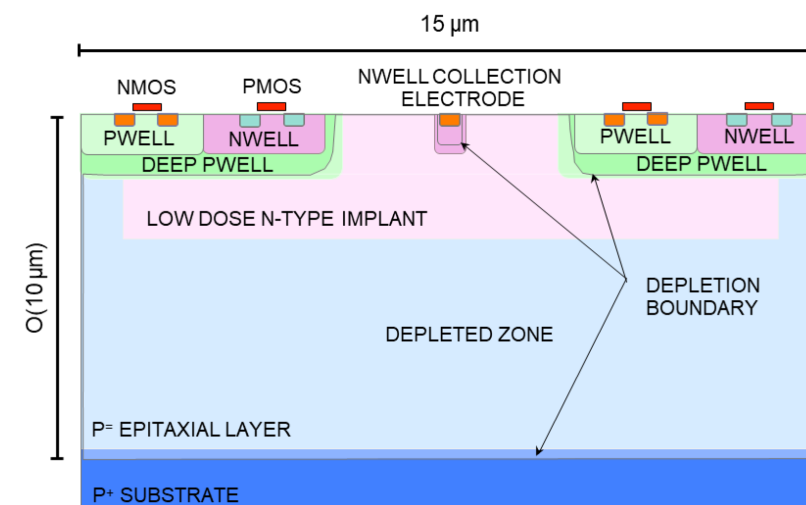
Engineering Run 2&3

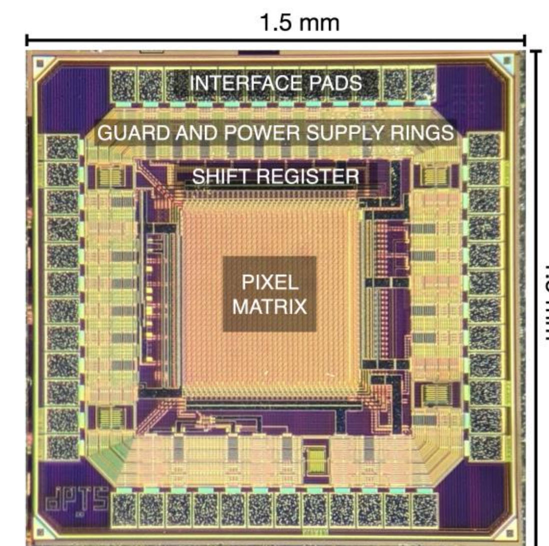
Final sensor:

- ER2 – final sensor prototype (design ongoing)
- ER3 – final sensor production

Digital Pixel Test Structure

- I previously worked on the DPTS from the MLR1 submission
- The DPTS chip:
  - 1.5 mm x 1.5 mm
  - 32 x 32 pixel matrix
  - 15 µm pixel pitch
  - Includes in-pixel pulsing
  - One analogue pixel
  - Different chip biases used to control the operation of the chip
  - Can supply a reverse bias down to -6 V (Vsub = Vpwell)
- Provides insights on the applicability of the custom digital cells used to compose the architecture
- Testing includes:
  - Laboratory characterisation to better understand the operation
  - Testbeams to investigate efficiency, spatial resolution and timing resolution
  - Look at irradiated chips up to NIEL: 1×10^{15} 1 MeV $n_{eq}cm^{-2}$ and TID: 10 Mrad
- The first test results of the DPTS were published: here





Role at DL for DPTS testing

- I continued my role as DPTS coordinator at DL to produce a 2nd paper of results
- The goal of the paper is to collate all remaining results, with a particular focus on the chip performance in low-power consumption regimes
- 2nd paper includes:
  - Chip performance at low power consumption:
    - In the lab: threshold RMS, noise and fake-hit rate (FHR)
    - Test beam: detection efficiency and timing resolution
  - Chip performance after ionising irradiation:
    - In the lab: threshold, FHR, annealing
    - Test beam: detection efficiency and annealing
  - Study into the FHR
  - Measurements of fluorescence X-rays emitted from a target, up to 28 keV
  - Chip performance with inclined tracks at a test beam
- The first draft is complete and under internal review

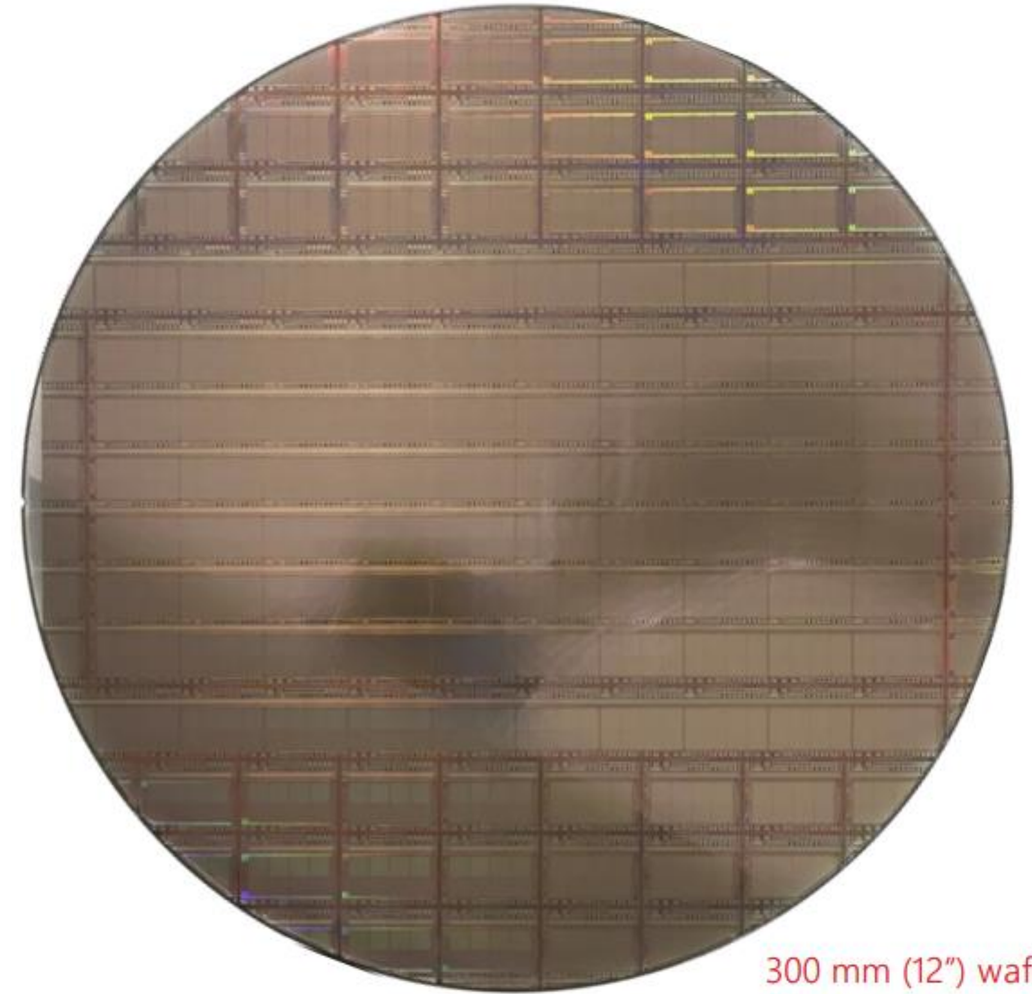
- DL contribution
- DL Supervised/contributed

Engineering Run 1 wafer

- Engineering Run 1 (ER1) consists of two stitched prototypes:
  - **MOSS**: **MO**nolithic **S**titched **S**ensor (14 x 259 mm^2)
  - MOST: Timing (2.5 x 259 mm^2)
- The goal is to show the feasibility of the stitching process:
  - Manufacturing yield (-> power segmentation granularity)
  - Power distribution and readout over 27 cm length
  - Study uniformity, noise, spread, leakage
  - Pixel architecture characterisation
- Understand stitching 'rules', redundancy, fault tolerance

ER1 wafer layout + stitching

Design reticle



300 mm (12”) wafer

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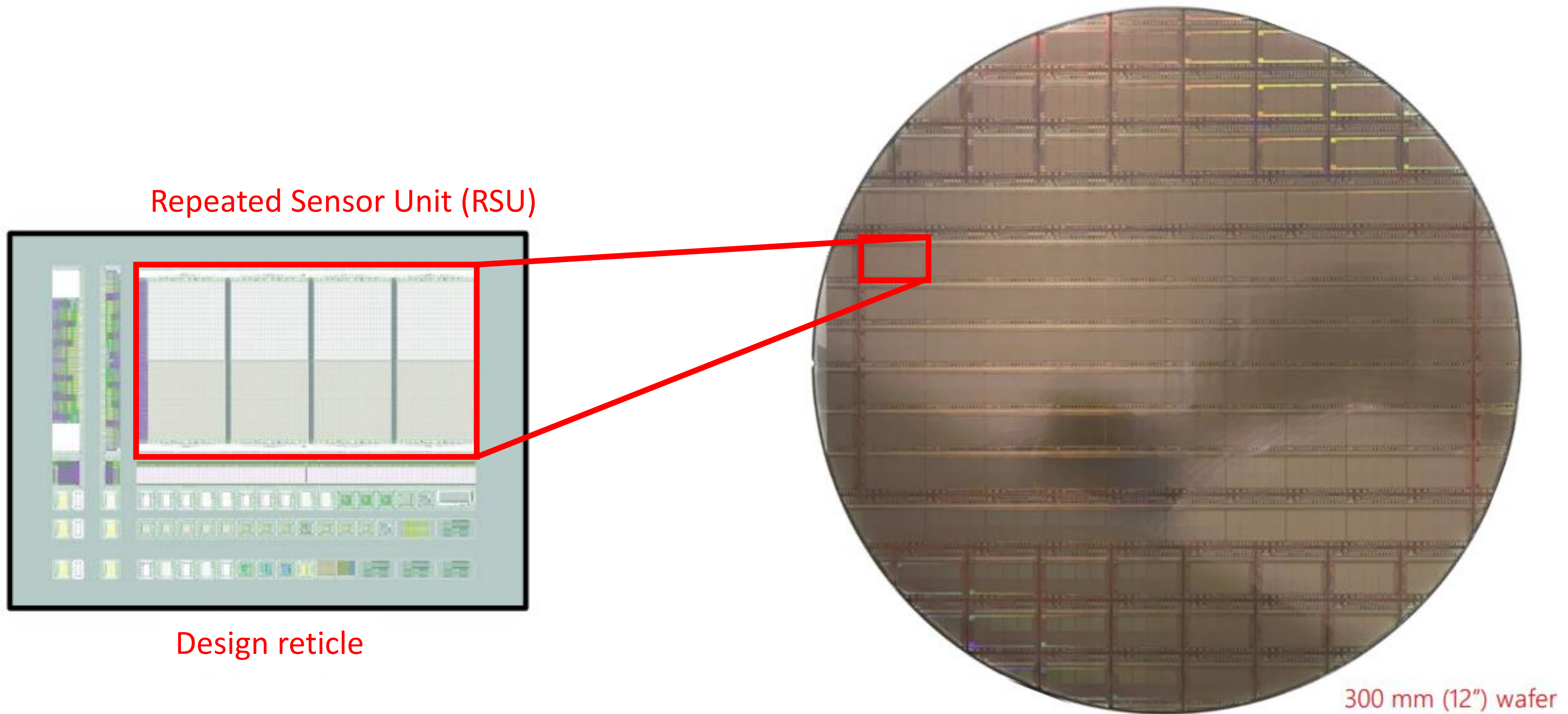
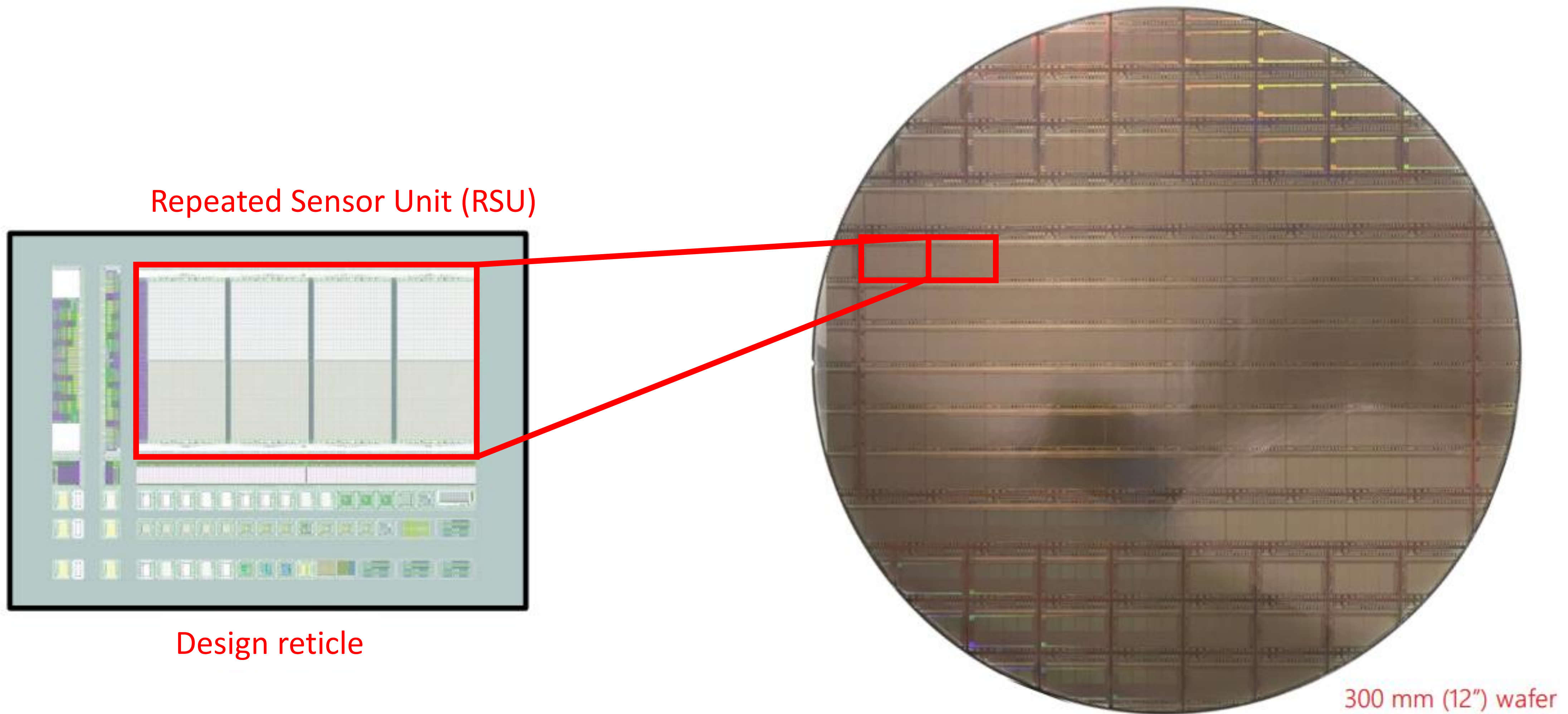
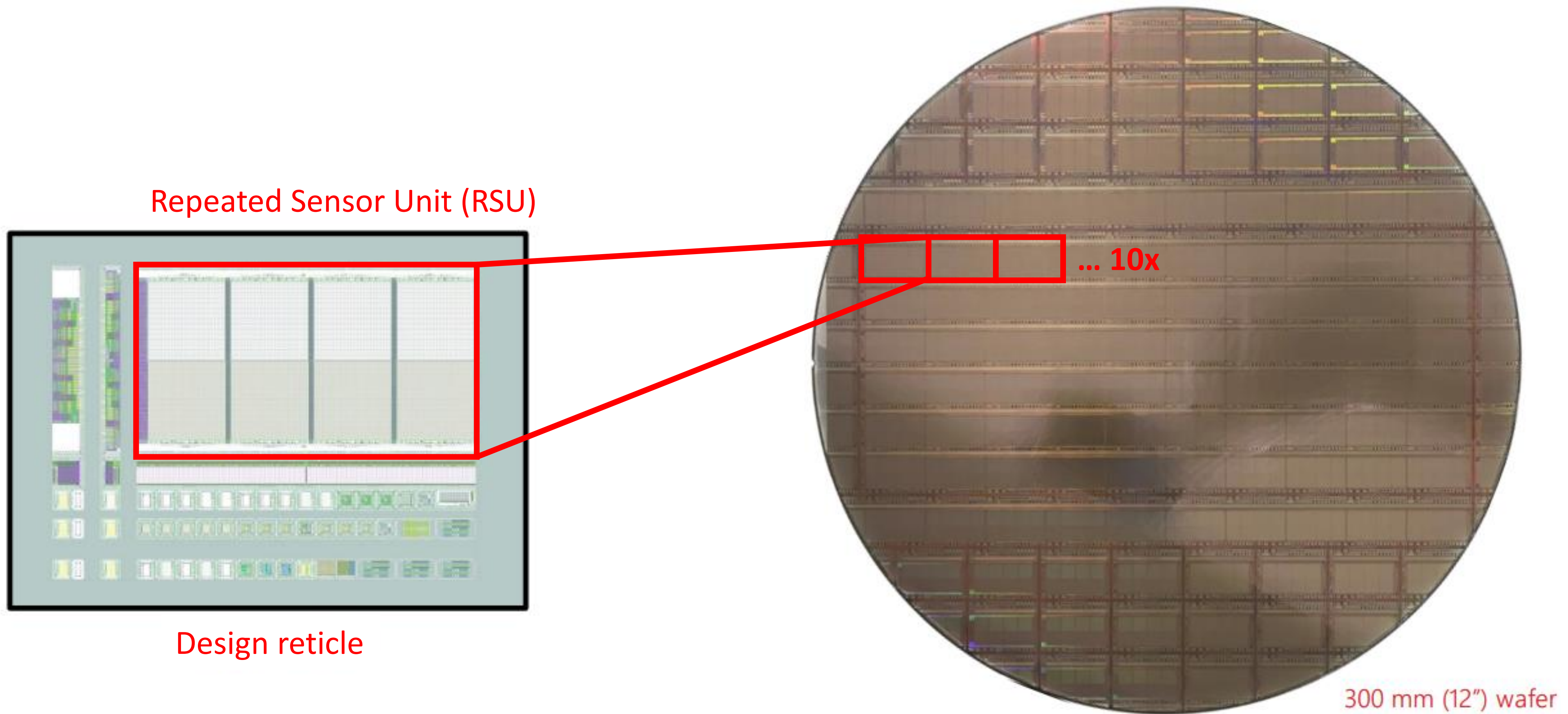
ER1 wafer layout + stitching



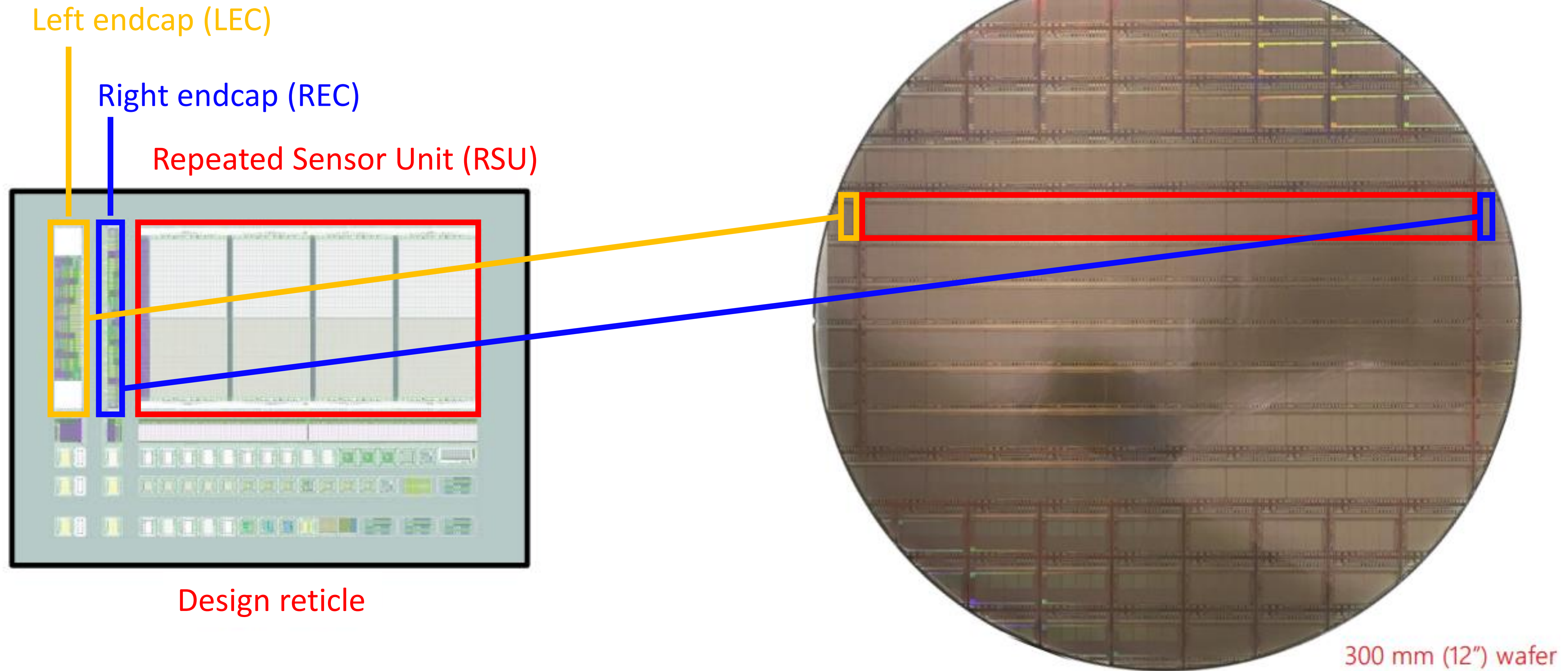
ER1 wafer layout + stitching



ER1 wafer layout + stitching

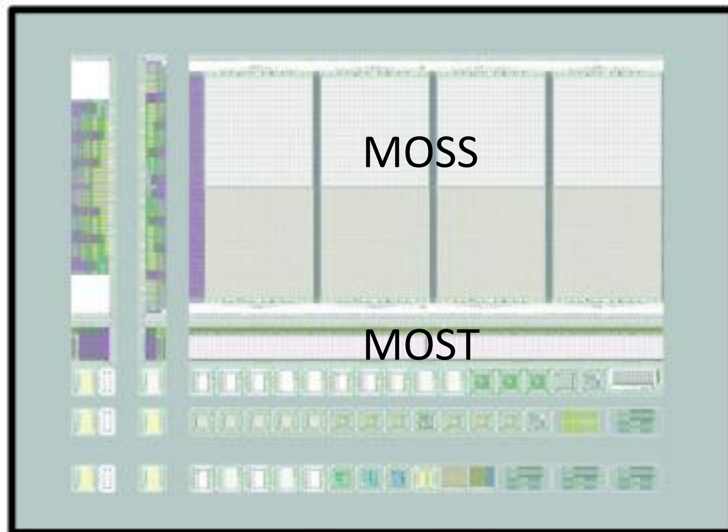


ER1 wafer layout + stitching

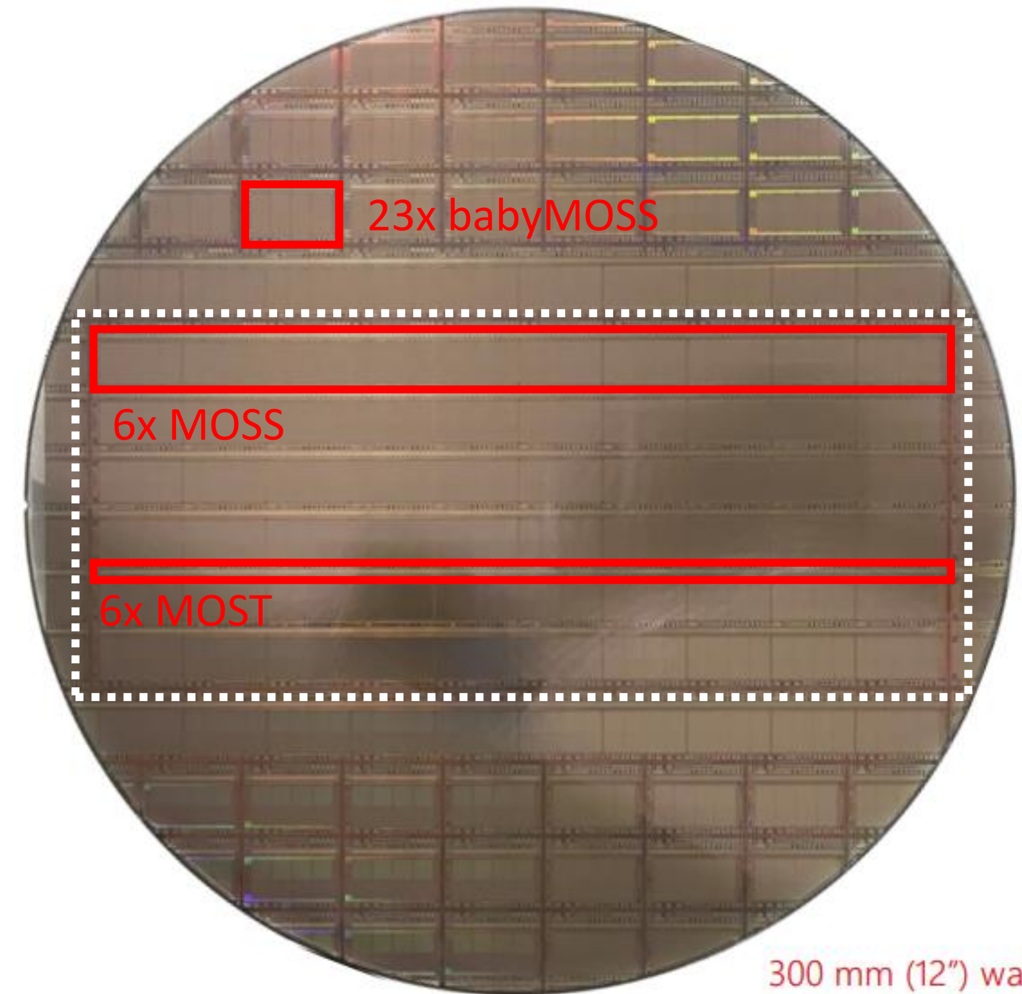


ER1 wafer layout + stitching

- Bonus chips: **babyMOSS**
- A single RSU with both endcaps



Design reticle



300 mm (12") wafer

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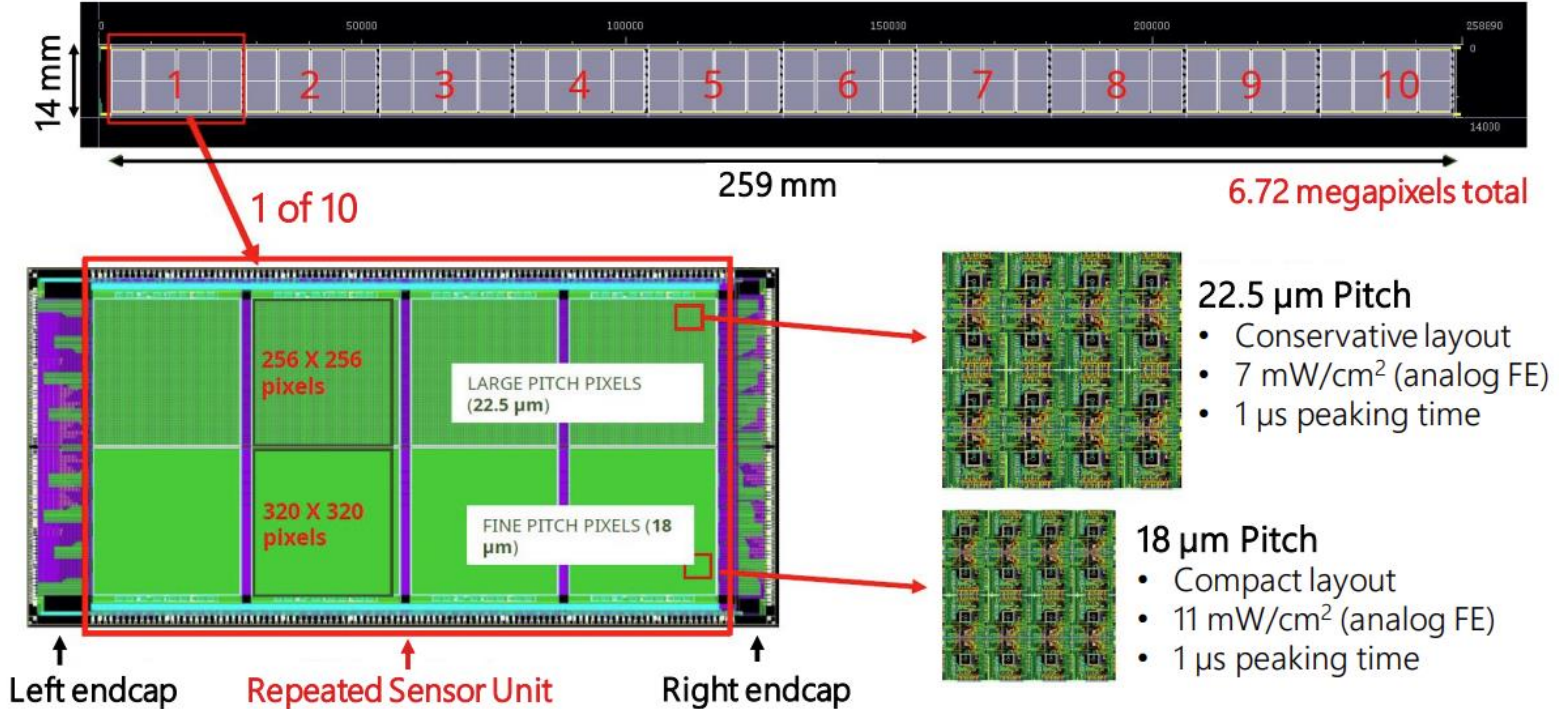
Monolithic Stitched Sensor



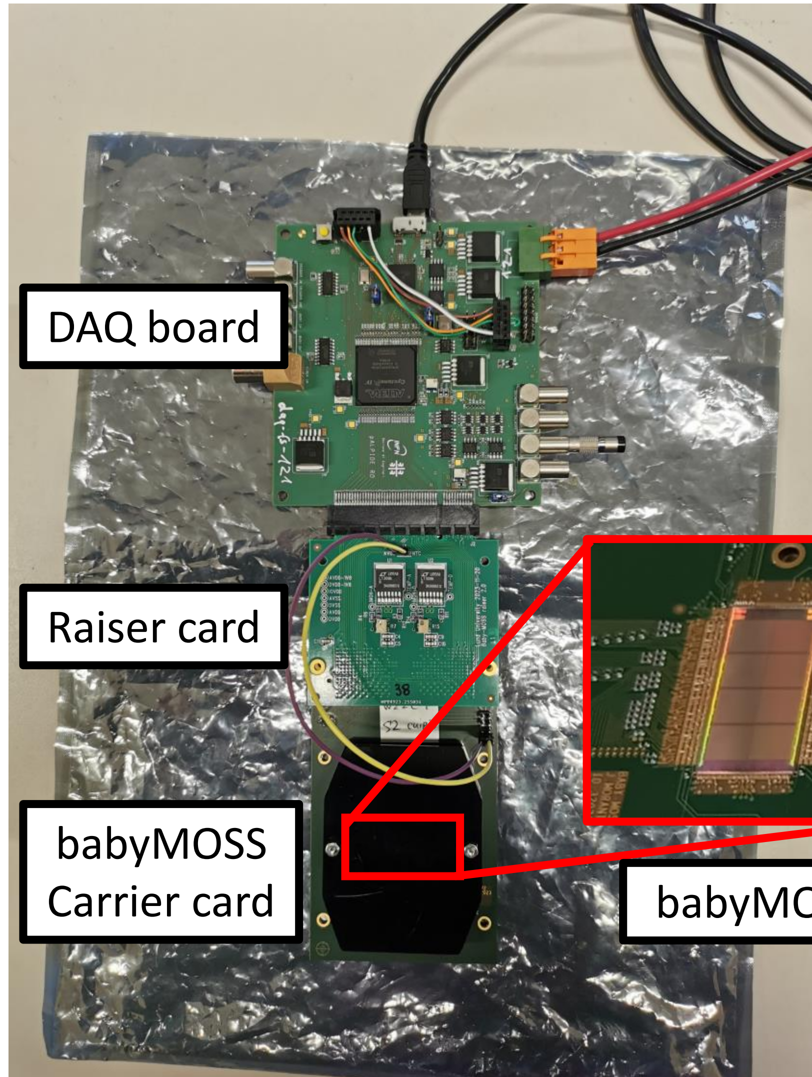
22.5 µm Pitch

- Conservative layout
- 7 mW/cm^2 (analog FE)
- 1 µs peaking time

18 µm Pitch

- Compact layout
- 11 mW/cm^2 (analog FE)
- 1 µs peaking time

babyMOSS test system



DAQ-raiser
test system

Power
supply

DAQ
computer

babyMOSS test system

Test system:

- The DAQ board controls and reads out the chip.
- The Raiser board is an interface board between the DAQ board and the Carrier board
- The Carrier board hosts the babyMOSS chip, which is glued and wire-bonded to the board

- DAQ board has firmware that needs to be programmed
- There is software that is used to control the test system, perform scans and analyse the data
- When using the software 2 config files are needed:
  - ts_config.json5: used to define the test system
  - scan_config.json5: used to control the scan properties (which units to power, DAC settings, masks etc)

babyMOSS list of scans

- Impedance and power testing (performed at CERN with a special setup):
  - 1st impedance measurement: pre-powering.
  - power ramp without PSUB.
  - power ramp with PSUB.
  - 2nd impedance measurement: post powering.
- Functional testing:
  - **power on scan**: powers and configures the chip and measures the currents at each stage
  - **register scan**: for each register, write certain patterns and check the read out
  - **shift register scan**: same as register scan but for the row shift register that controls pulsing and masking
  - **DAC scan**: scans all the DACs used for the chip biasing
- Readout and pixel matrix testing:
  - **digital scan**: pulses the digital circuit for each pixel and measures the hits
  - **analogue scan**: pulses the analogue circuit for each pixel and measures the hits
  - **FHR scan**: read out 100k triggers and measure the noise hits, gives the fake-hit rate of the chip
  - **threshold scan**: uses the analogue pulsing to measure the threshold of each pixel

babyMOSS stability scan

- After familiarisation with the test system, software, scan and analysis, I was tasked with adapting a scan used for the MOSS for the babyMOSS
- This was the stability scan
- The goal of the scan is to measure the reference current (IREF) and voltage (VREF) and the chip analogue currents as a function of each DAC parameter (IBIAS, IDB, IRESET, VCASB, VCASN, VSHIFT)
- This would confirm if the test system was stable over the chip parameter space
- Performed the scan and the results were good

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Summary

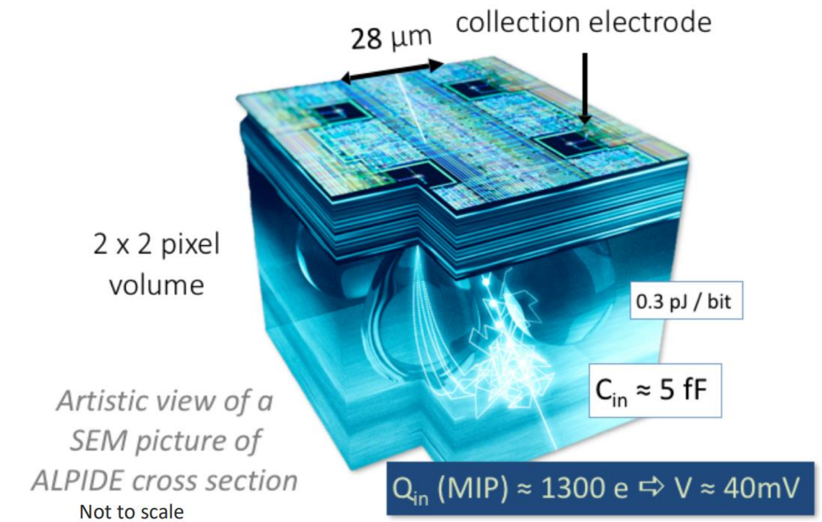
- babyMOSS is a single sensor unit of the MOSS chip
- Received training at CERN and will soon contribute to the testing of the chip

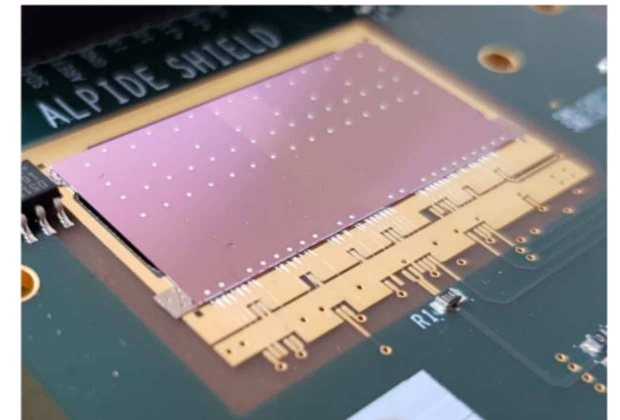
- Next steps:
    - Receive a test system and babyMOSS chip at DL
    - Decide with CERN a testing plan for DL
    - Polish stability scan code and commit to repository

Backup

Sensor choice

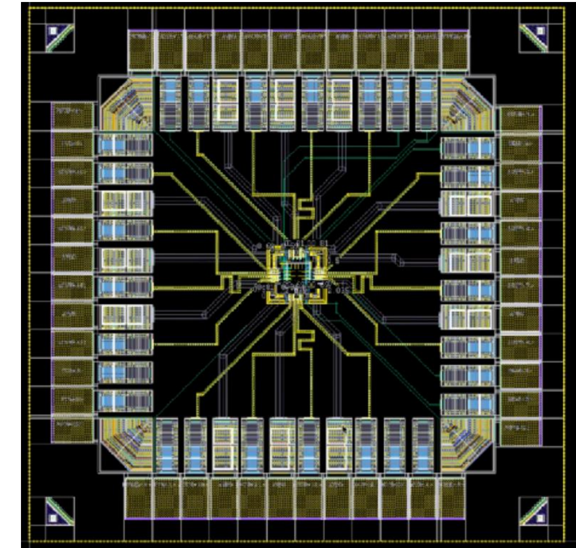
- The ITS3 design leads to many cutting-edge developments in sensor performance, mechanics and design
- With the success of ALPIDE (180 nm) for the ITS2, this chip is a good starting point for ITS3
- ALPIDE:
  - Fully efficient
  - Very low noise
  - Good power-density (esp. in-matrix)
- But for ITS3:
  - Not large enough (only 200 mm wafers)
  - Power consumption is too high for air cooling





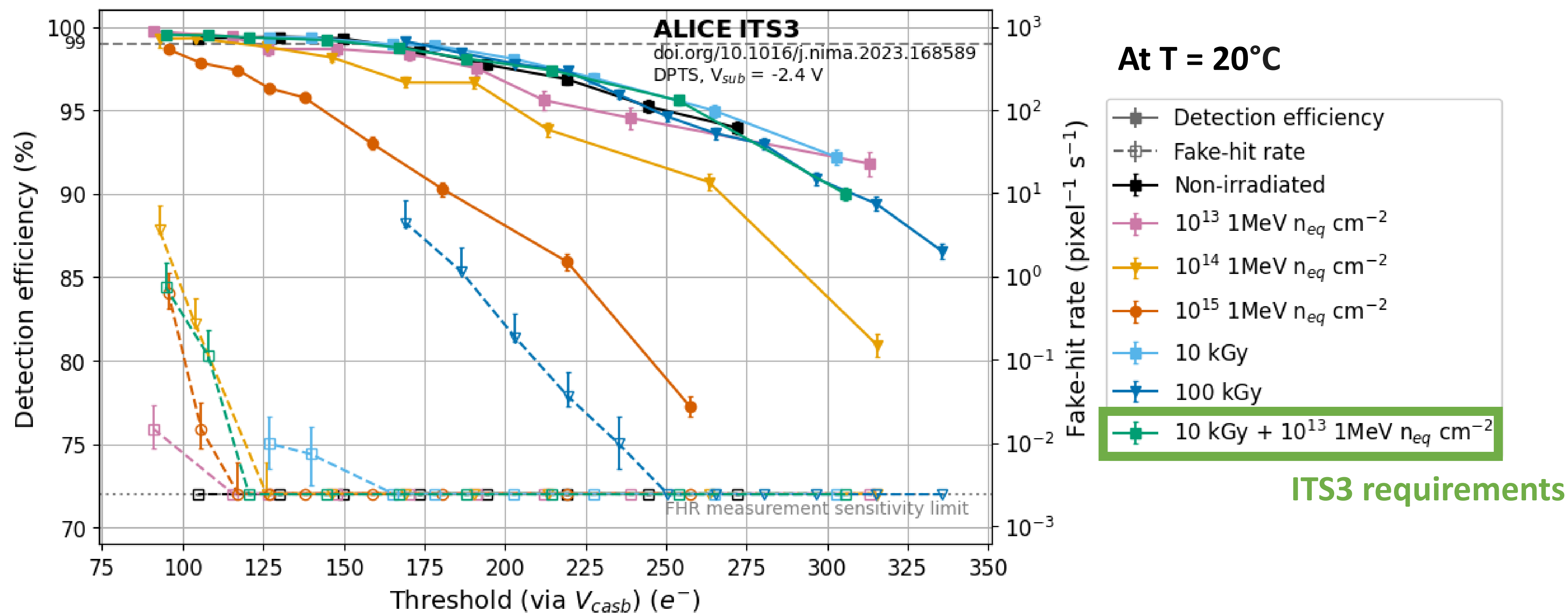
Moving to 65 nm TPSCo process

- Using a smaller technology, 65 nm, will open more possibilities:
  - Produced on 300 mm wafers, allows for complete z-coverage in the detector (ITS3 active area 270 mm)
  - Possibility to use stitching to reach wafer scale sensors
  - Lower power consumption when moving to deeper sub-micron
- Challenges:
  - Optimise sensor design for yield
  - Charge collection to be optimised due to thinner epi layer
  - Radiation hardness needs testing, moderate levels are foreseen (NIEL: $1\text{x}10^{13}$ 1 MeV $n_{eq}cm^{-2}$ and TID: 10 MRad)
- New technology will need extensive characterisation and qualification



65 nm pixel test structure

DPTS results: efficiency



- Results from the DPTS validated the technology in terms of detection efficiency, spatial resolution, fake-hit rate and radiation hardness

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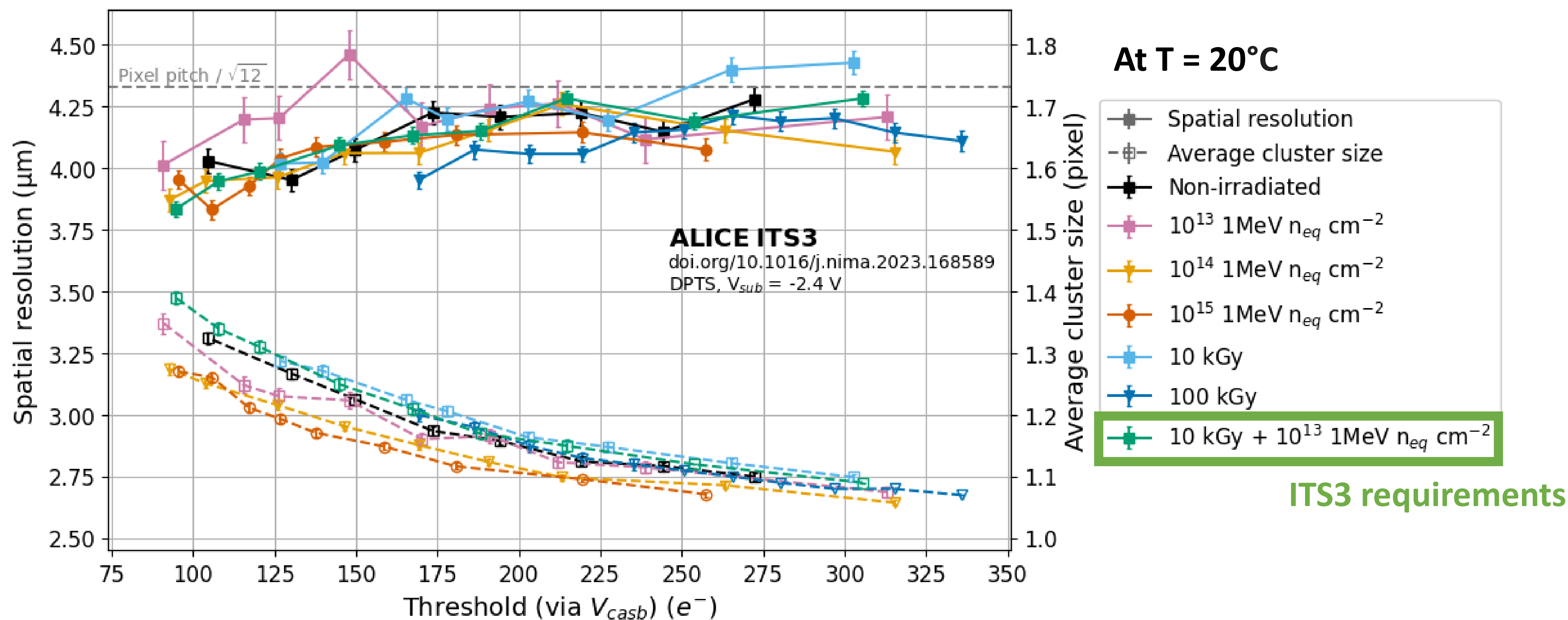
DPTS results: spatial resolution



- Results are published: https://doi.org/10.1016/j.nima.2023.168589