Summary of work @ORNL
:Astropix Sync-up

2024. 11. 26

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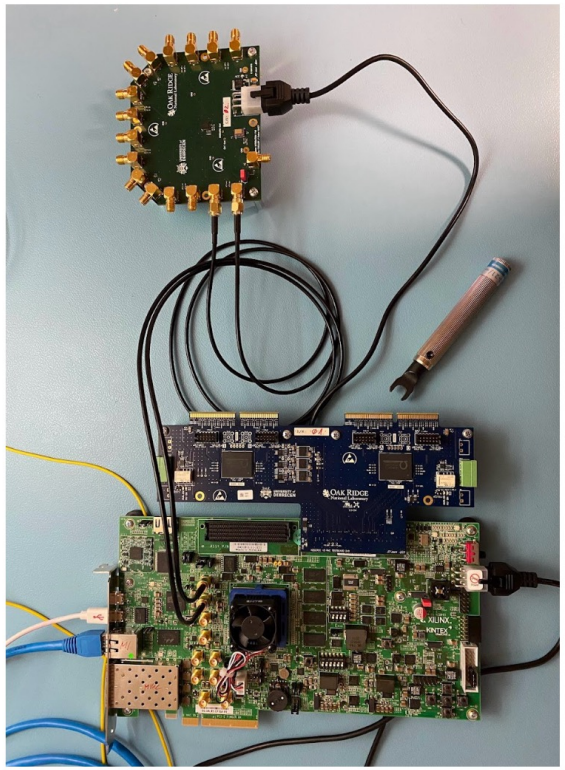
Summary @ORNL

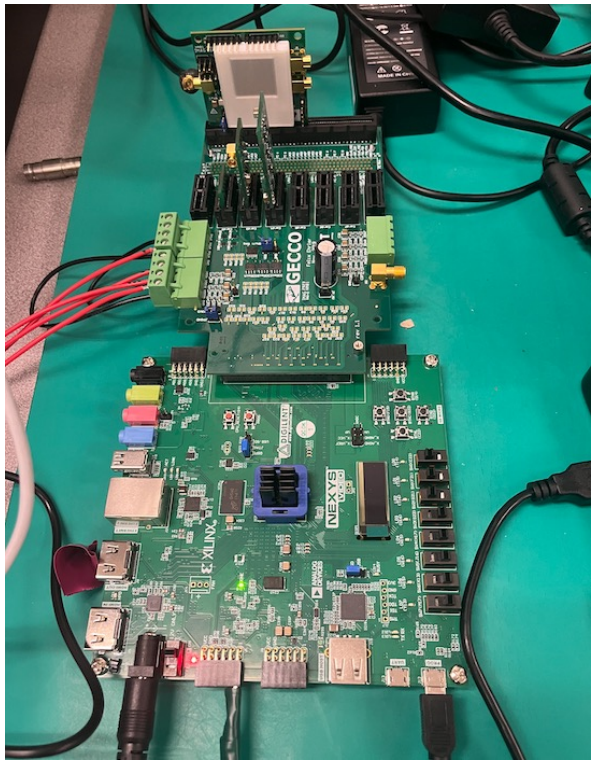
- Synchronize two different system (astropix + baby bcal)
  - So, want to feed them the same clock and track coincidence event by timestamp
- Enabled with the use of external clock on the current astropix readout system
  - Based on the firmware that we used in beam test at FANL in last June
- First try to use one of the PMOD on the nexys board to input a 10MHz clock
- Next visit (Jan. 2025?), try with common clock for H2GCROC and discuss further details

Common clock

Protoboard 2.0 with two H2GROC3A

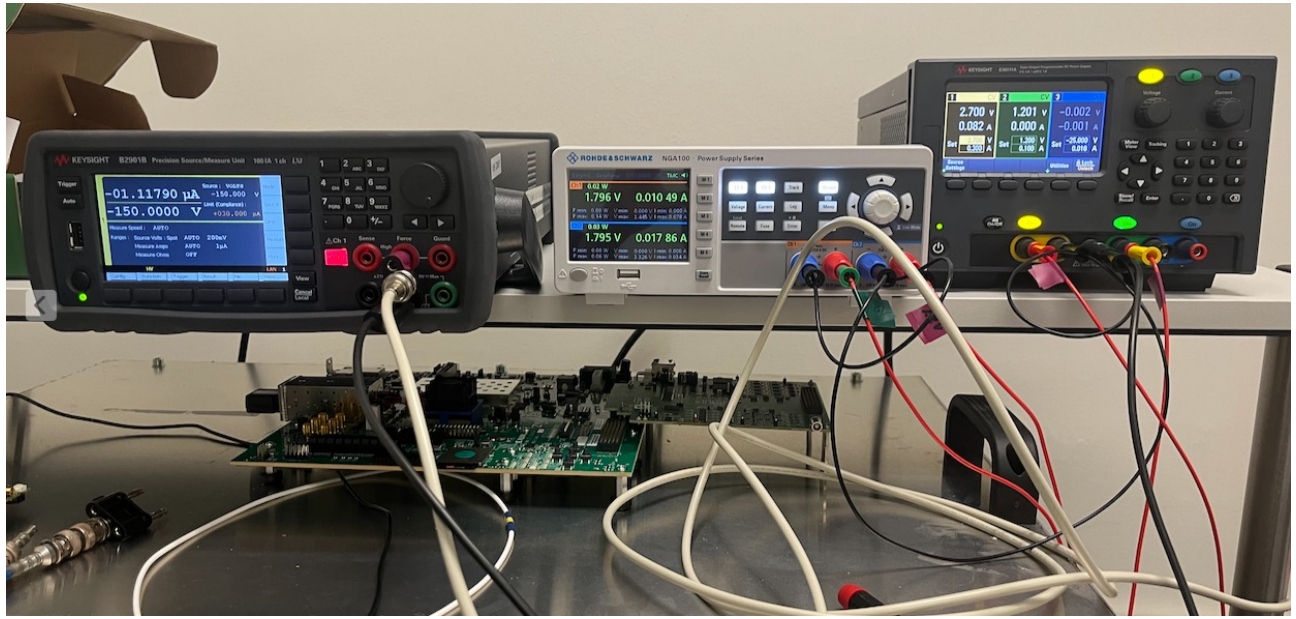
Xilinx KCU

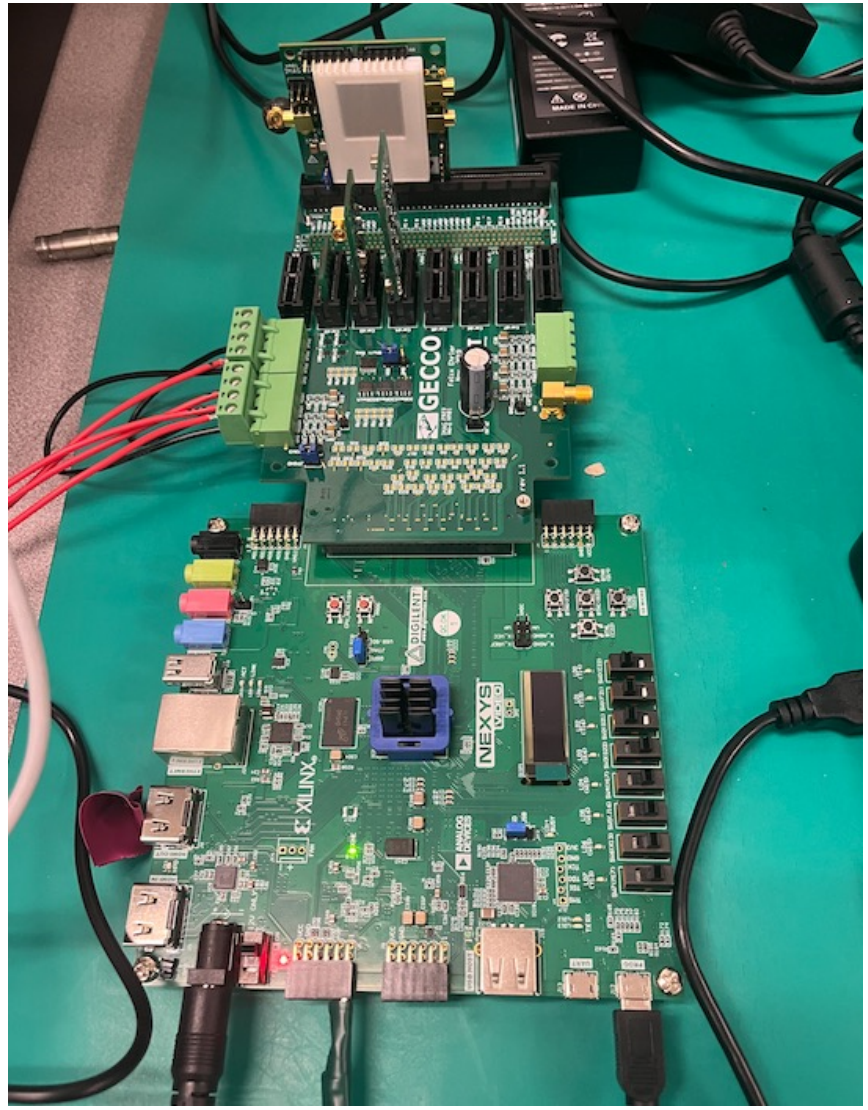




Work @ORNL

- First try to use one of the PMOD on the nexys board to input a 10 MHz clock
  - Test 10 MHz external clock from function generator





10. Pmod Ports

The Pmod ports are arranged in a 2×6 right-angle, 100-mil female connectors that mate with standard 2×6 pin headers. Each 12-pin Pmod connector provides two power pins (6 and 12), two ground pins (5 and 11), and eight logic signals, as shown in Fig. 20. The VCC and Ground pins can deliver up to 1A of current. Pin assignments for the Pmod I/O connected to the FPGA are shown in Fig. 12.

Warning: *Since the Pmod pins are connected to Artix-7 FPGA pins using a 3.3V logic standard, care should be taken not to drive these pins over 3.4V.*

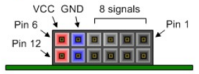
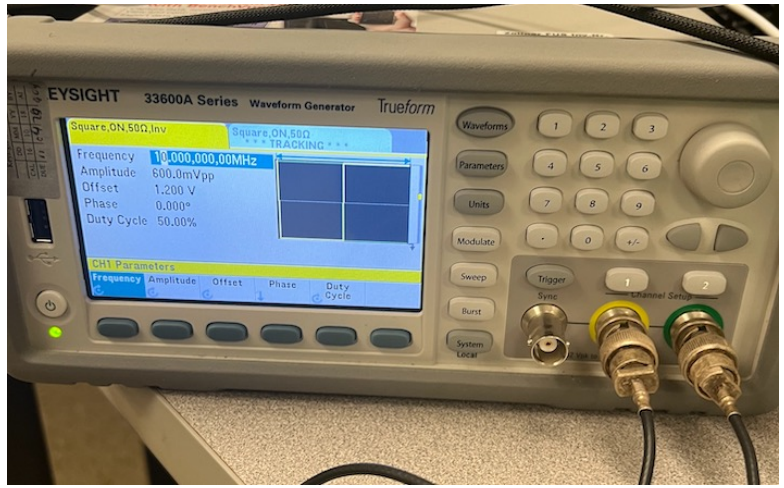


Figure 12. PMOD Ports: Front view as loaded on PCB.

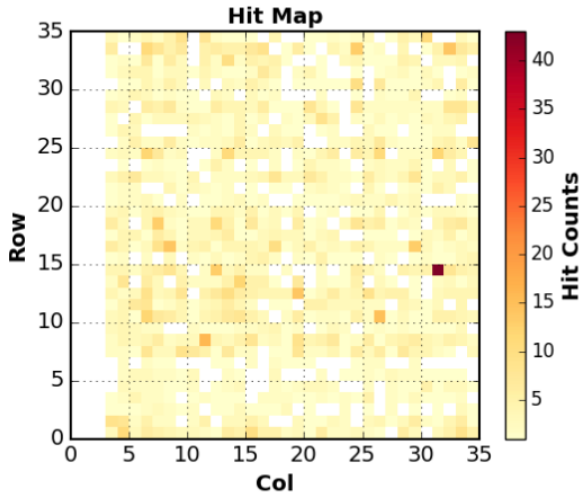
The Nexys Video features four Pmod ports of different "styles" with subtle differences between them. Table 9 summarizes these differences.

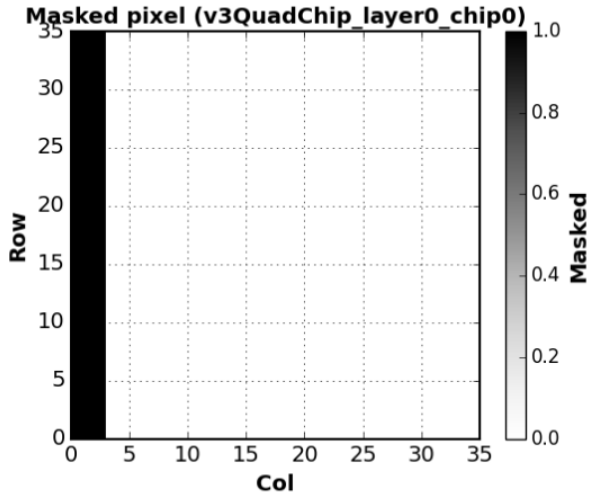
Pmod connector	Power	Analog/Digital	Routing	Series protection	Recommended usage
JXADC	VADJ	Dual	Differential; Pairs: 1-7,2-8,3-9,4-10	100 ohm	Analog inputs; input/output (VADJ=2.5V)
JA	3.3 V	Digital-only	Single-ended	200 ohm	<10 MHz, LVCMOS33
JB, JC	3.3 V	Digital-only	Differential; Pairs: 1-2,3-4,7-8,9-10	0 ohm	>=10MHz; LVDS_25 input only, or TMDS_33 input/output

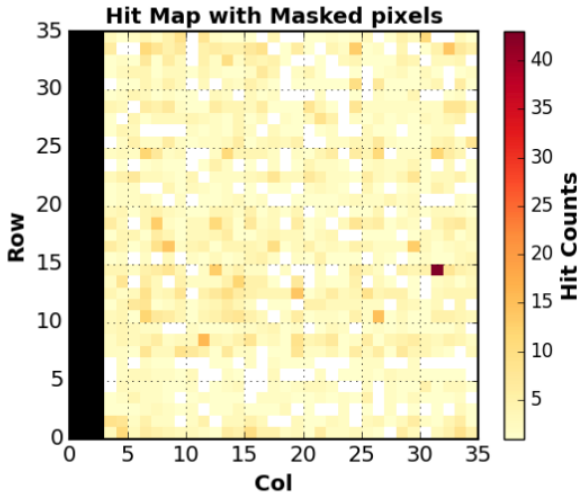


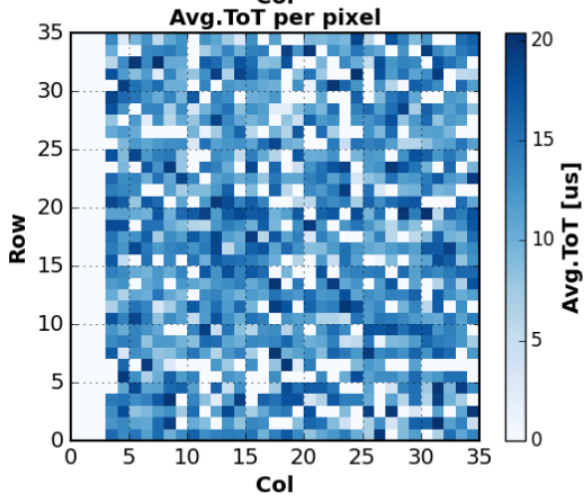
Test result (1) @ORNL

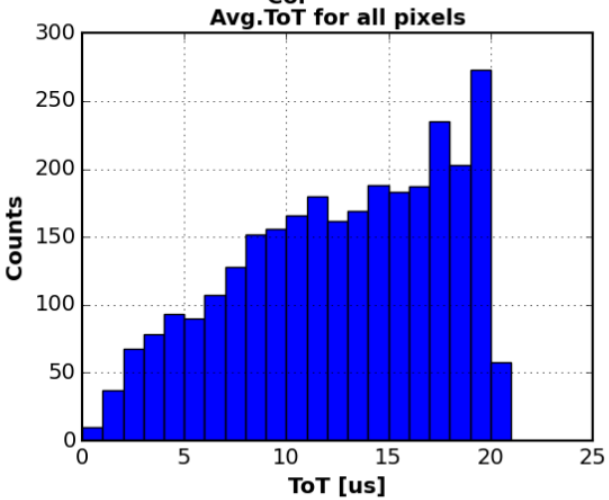
- w101s07 chip
- HV: -150 V
- Threshold: 100 mV
- w.ExternalClockCable
  - 10 MHz, 600 mV_{pp}
- w.source Fe55
  - 5.89 keV, 6.49 keV
- 10m data taking









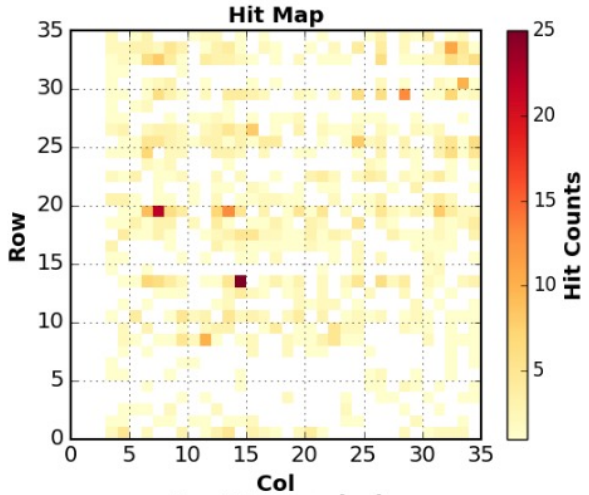


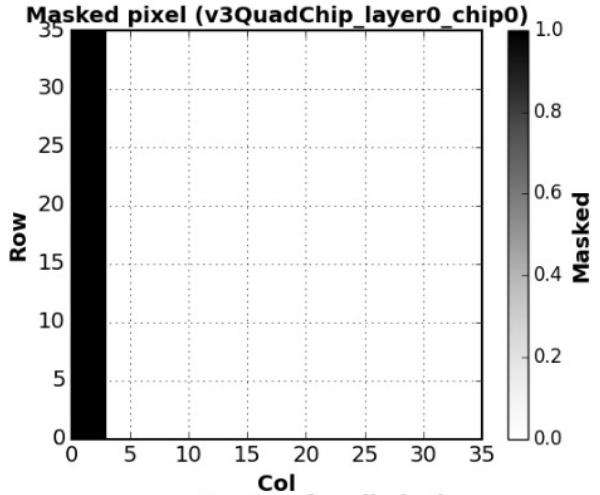
Events: 13562

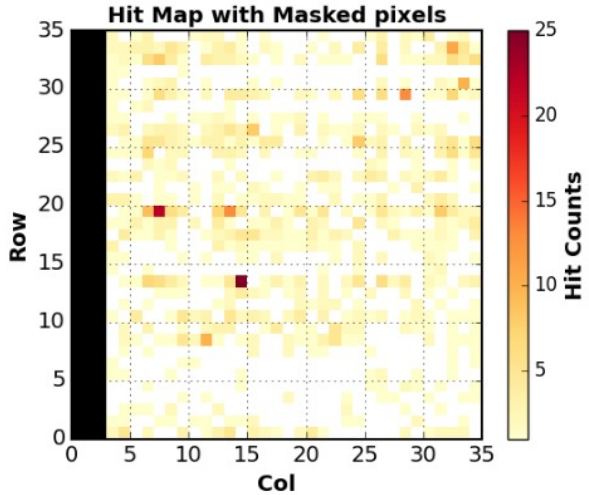
Processed below
conditions: <2 timestamp and <10% in ToT
nevents: 100.00%
nhits: 2923
Available Pixels: 91.43%

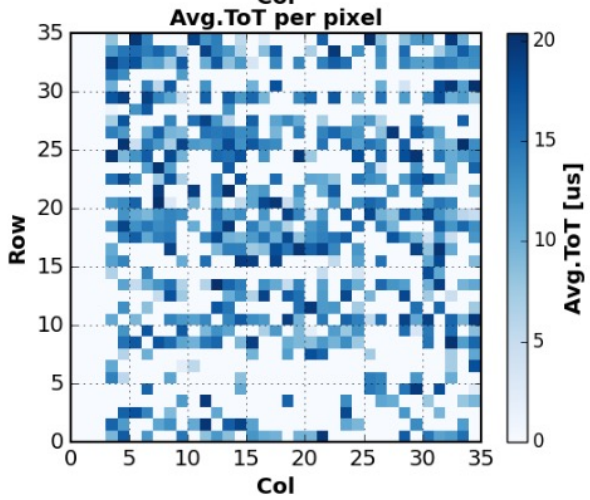
Test result (2) @ORNL

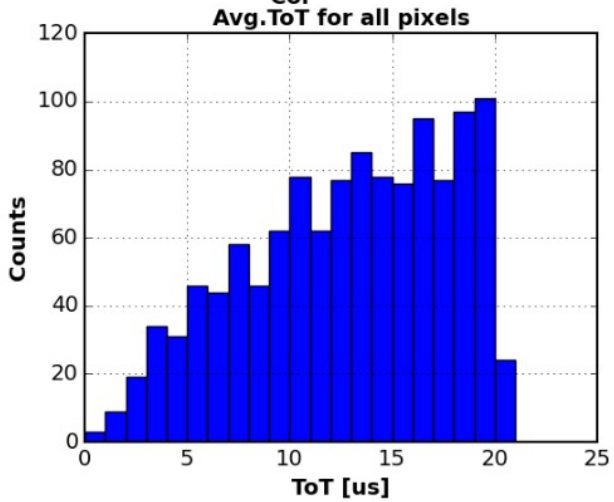
- w101s07 chip
- HV: -150 V
- Threshold: 100 mV
- w.ExternalClockCable
  - 10 MHz, 600 mV_{pp}
- w.source Ba133
- 1m data taking











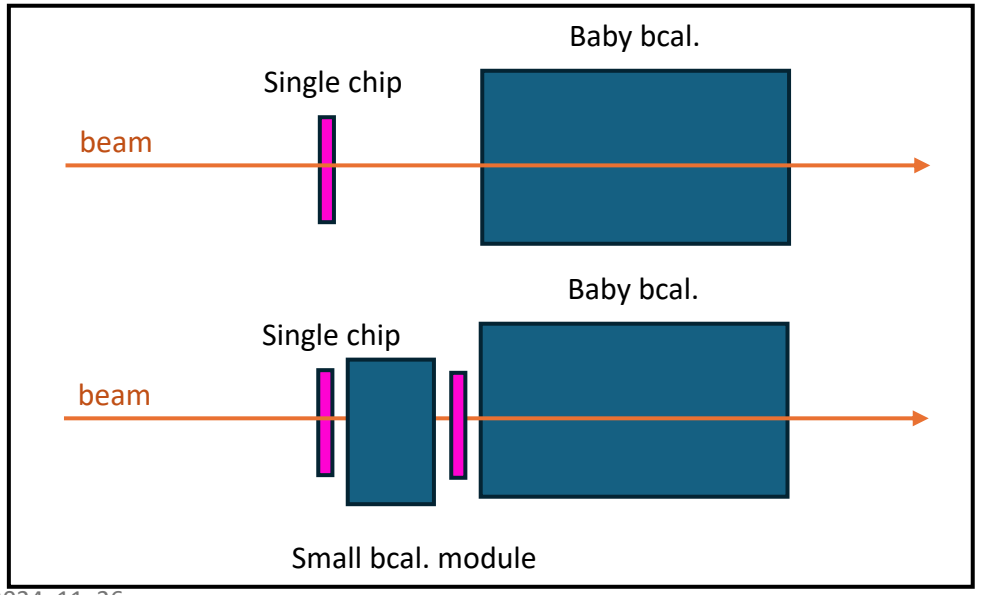
Events: 6140

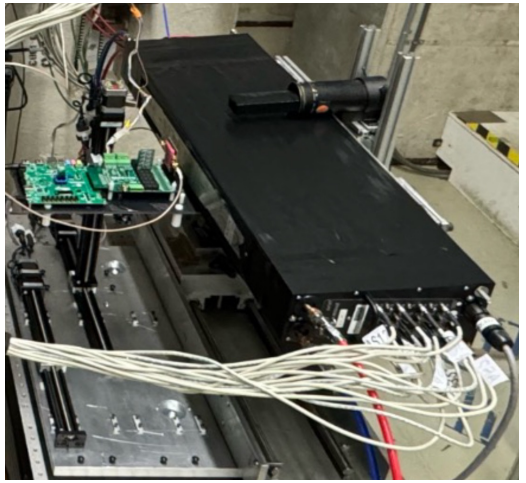
Processed below
conditions: <2 timestamp and <10% in ToT
nevents: 100.00%
nhits: 1202
Available Pixels: 91.43%

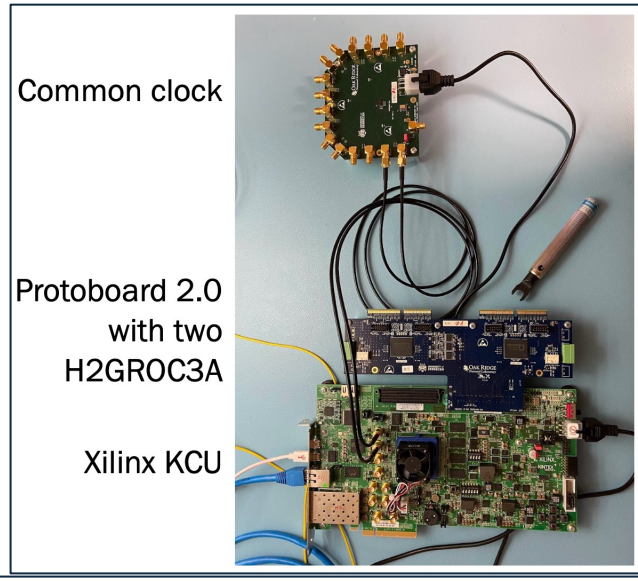
For upcoming beam test?

- Visiting ORNL from Nov. 11 for 1 week
  ✅ Enabled with the use of external clock on the current astropix readout system

- Plan A: if **H2GCROC is available** and it is confirmed to work well
  - Prior work must be completed:
    - External clock on astropix v3 single chips
    - Test H2GCROC with baby bcal → design of readout box ongoing?
- Plan B: **H2GCROC is not available?**
  - Prior work must be completed:
    - External clock on astropix v3 single chips
    - Enabled with the use of external clock on the current babyBCal DAQ system?
- 2025 beam test for BIC by Korean group
  - considering to submit beam request at KEK beam-test facility for March 2025
  - Target to use CERN PS T9 or T10 for 1 week during August







- H2GCROC features front end for SiPM readout
- Measures ADC, Time of Arrival (ToA), and Time over Threshold (ToT) with large dynamic range
- Adapted to sampled mode for ePIC streaming readout
- EIC-specific CALOROC variant in development

- Common clock: 40 MHz